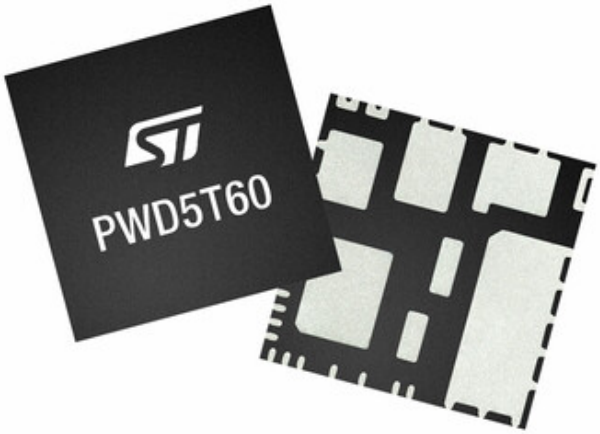
Manufacturing and layout guidelines for SiP embedding MOSFETs

Introduction

System-in-package – named SiP in the rest of the document – is increasingly gaining market share in power electronics and is widely recognized as a BOM and space saving solution. STMicroelectronics leads this trend with a wide offer of SiP and a continuous focus on improving this technology.

When it comes to layout design and PCB assembly, especially for those devices embedding power MOSFETs, SiP presents challenges that may need to be addressed with successive optimizations. The aim of this document is to provide some guidelines to ease SiP board manufacturing and layout by providing some recommendations and tips.

Figure 1. PWD5T60 is an example of SiP embedding MOSFETs.



1 Manufacturing considerations

The Quad Flat No-lead (QFN) package technology is widely used due to its excellent thermal and electrical performance, compact size, and cost-effectiveness. QFN packages are leadless packages with terminals located at the bottom of the package. They provide a small footprint and low profile, making them ideal for high-density applications. The key features include:

- **Thermal pads**: enhance heat dissipation
- **Peripheral pads**: ensure electrical connectivity
- **Moisture sensitivity**: requires proper handling to prevent damage

Proper soldering techniques are crucial to ensure reliable electrical connections and mechanical stability with this type of package.

This section of the document provides detailed guidance on the solderability process for SiP in QFN packages.

STMicroelectronics' SiP, for example PWD13F60, PWD5F60, PWD5T60, and POWERSTEP01 have a Thermally Enhanced Plastic Very Thin Fine Pitch QFN package (VFQFPN, QFN category).

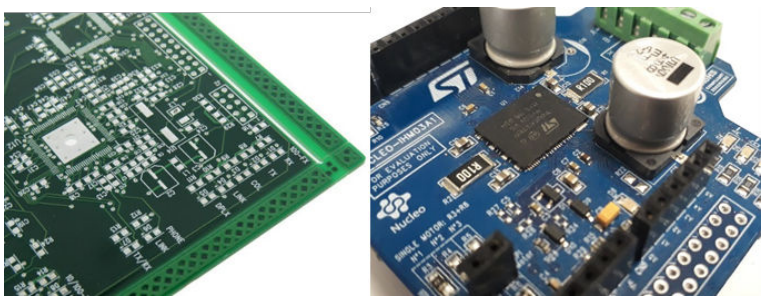
1.1 QFN packages and PCB finishing

QFN packages have been on the market since the early 2000s and are commonly soldered on a variety of PCB surface finishings.

Almost all PCB finishings are compatible with VFQFPN:

- Hot Air Soldering Levelling (HASL - HAL)
- Organic Soldering Preservative (OSP)
- Immersion Tin
- Immersion Silver
- Electroless Nickel Immersion Gold (ENIG)

Figure 2. Examples of PCB surface finishing



The main purpose of surface finishing is to preserve the PCB copper surface prior to soldering.

Each finishing has its own pros and cons: the selection of finishing is mainly based on process manufacturing requirements and specific experience of each PCB manufacturer.

1.2 SMD soldering

VFQFPN packages are soldered with the standard SMD process used for QFN devices.

There are several steps to follow to achieve a good quality soldering of QFN devices: the main aspects are described hereinafter.

1.2.1 Preparation for soldering

1.2.1.1 Storage and handling

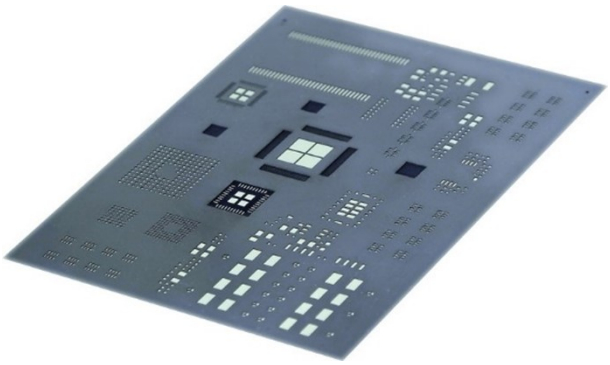
Two key aspects must be considered when QFN packages are stored and handled on the PCB manufacturing site:

- **Moisture sensitivity**: store QFN packages in moisture barrier bags with desiccant.
- **ESD protection**: use ESD-safe workstations, equipment, and handling procedures.

1.2.1.2 Stencil design

To depose the solder paste on the PCB prior to soldering, a stencil with proper thickness and aperture (that is, holes where solder is deposed) has to be designed and used, as per the usual SMD process. Based on STMicroelectronics' experience, it is possible to achieve positive results with a stencil thickness from 80 µm (3 mils) to 125 µm (5 mils). The thickness can be further increased up to 150 µm (6 mils) in case of pitch greater than 0.5 mm.

Figure 3. Example of stencil



Stencil selection and design may also depend on other components mounted on the PCB and it is based on the equipment and process experience of the PCB manufacturer. It is recommended to adjust the stencil's characteristics to fulfill specific production environments after initial soldering tests.

1.2.1.3 Solder paste type

STMicroelectronics recommends using a standard solder paste type 3 or higher (type 4 is often used). Solder paste type indicates the average solder sphere diameter: the lower the type, the larger the average solder sphere diameter. It is recommended that the stencil aperture be at least 5 times the average solder sphere diameter.

Type 3 solder paste has an average solder sphere of 36 µm, while for type 4 it is 30 µm. For this reason, any aperture smaller than 180 µm (7 mils) should use type 4 solder paste.

It is recommended to store solder paste in a controlled environment to maintain its properties.

1.2.2 Reflow soldering process

1.2.2.1 Reflow profile

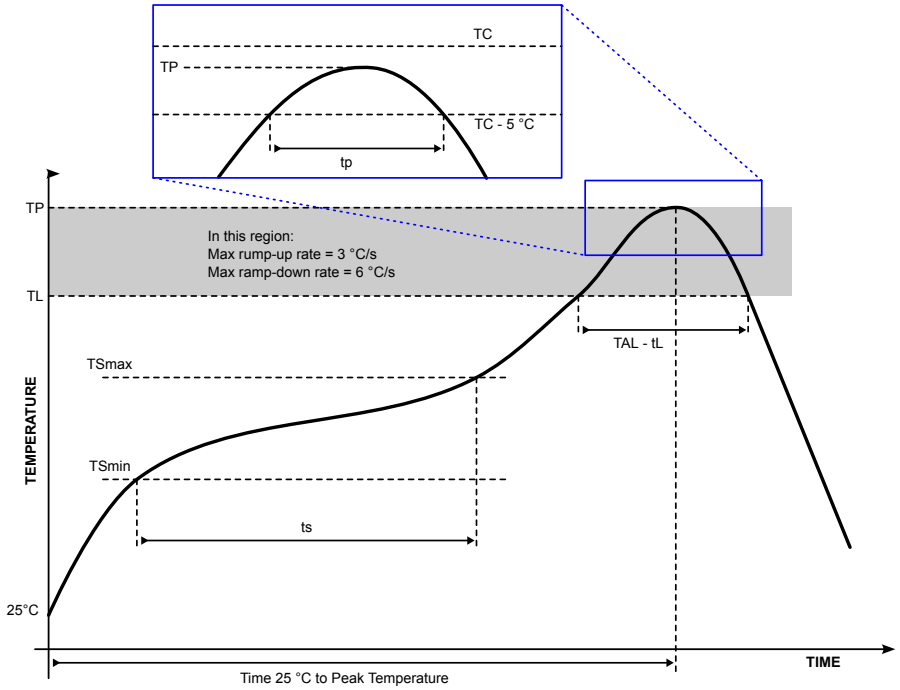
The reflow soldering process involves heating the assembly in a controlled manner to melt the solder paste and form solder joints. The reflow profile consists of several stages:

- **Preheat stage**: gradually heat the assembly to avoid thermal shock. The temperature should increase at a rate of 1-3 °C per second until it reaches the soak stage.
- **Soak stage**: maintain a stable temperature to activate the flux and remove any volatiles. The temperature range is usually between 150 °C and 200 °C, and the typical duration is 60-120 seconds.
- **Reflow stage**: heat to peak temperature to melt the solder paste (see examples in Section 4). The peak temperature is generally between 230 °C and 250 °C for lead-free solder. The time the solder is above its melting point (Time Above Liquidus, TAL) is typically 60 to 150 seconds. Paste manufacturers specify precise parameters.
- **Cooling stage**: cool down the assembly at a controlled rate to solidify the solder joints and prevent thermal shock. The cooling rate is typically 3-5 °C per second.

Table 1. Classification profiles (according to IPC/JEDEC J-STD-020F)

Profile feature	Pb-free assembly (SAC Alloys)
Temperature min. (Tsmin)	150 °C
Temperature max. (Tsmax)	200 °C
Soak time (Tsmin to Tsmax) (tS)	60 seconds – 120 seconds
Ramp-up rate (TL to TP)	3°C/second max.
Time 25 °C to peak temperature (Device supplier maximum)	8 minutes max.
Liquidus temperature (TL)	217 °C
Time Above Liquidus (TAL - tL)	60 seconds – 150 seconds
Peak package body temperature (TP)	TP shall not exceed TC
Time (tP) within 5 °C of the specified (TC), (see Figure 4)	30 seconds
Ramp-down rate (TP to TL)	6 °C/second max.
Classification temperature (TC)	260 °C for package thickness < 1.6 mm See material declaration of the part number for details

Figure 4. Pb-free reflow profile (IPC/JEDEC J-STD-020F)



1.2.2.2 *Nitrogen atmosphere*

Inert atmosphere: Using a nitrogen atmosphere during reflow soldering can reduce oxidation and improve the quality of solder joints. Nitrogen displaces oxygen, minimizing the formation of oxides on the solder and component leads.

1.2.3 Common issues and troubleshooting

The table below lists some of the most common issues related to soldering procedure, the typical root cause, and possible solutions:

Table 2. Common issues and troubleshooting

Issue	Cause	Solution
Solder bridging	Excessive solder paste or misalignment.	Adjust stencil design and improve placement accuracy.
Insufficient solder	Inadequate solder paste deposition.	Optimize stencil thickness and aperture design.
Voiding	Trapped gases during reflow.	Use a proper reflow profile and consider vacuum reflow processes. Other tips to reduce voids' formation are described in Section 1.3.

1.3 General guidelines for solder voids mitigation

There is consensus in the electronics assembly industry that solder joints with a low level of voids are more resistant to mechanical stress and more electrically and thermally conductive.

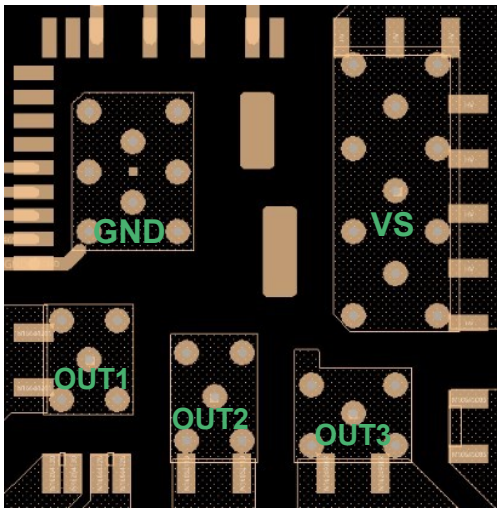
There are general guidelines, such as from the IPC (Global Association for Electronics Manufacturing), which recommend in QFN a level of voids under exposed pads below 50%.

Achieving low voiding in a solder joint requires the use of specially designed soldering materials in combination with carefully controlled process conditions. This section of the document provides general guidelines to reduce the occurrence of voids.

1.3.1 Use of vias

The presence of vias (standard, not filled), under exposed pads, can help reduce the number and size of voids. An example of a PCB with vias placed below exposed pads is shown in Figure 5; the diameter of vias is typically 0.25 mm (10 mils). Larger vias could draw too much solder from the pad; smaller vias are more expensive and must be placed in a higher quantity to be effective. It is recommended to place vias uniformly under the exposed pad and keep a safety margin from via to pad edge. As explained in Section 2.1, add as many vias as possible, keeping a distance of 1 mm (39 mils) typical between vias and at least 0.15 mm (6 mils) between the via and pad edge. Here below an example of PCBs with uniformly distributed vias below exposed pads.

Figure 5. PWD5T60 top layer PCB with highlighted vias



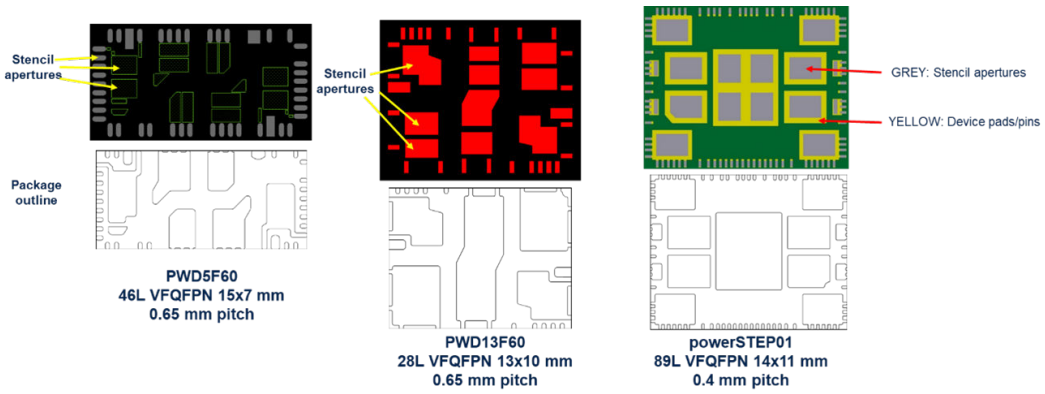
1.3.2 Stencil pattern and aperture

A second aspect to consider to limit voids is the stencil.

As a general guideline for QFNs, if the exposed pad is a square above 4 x 4 mm, stencil apertures shall be divided into smaller apertures with a covering between 50% and 70% of the pad area, depending on vias, stencil thickness, paste, etc., as seen in Figure 6.

Small pins use an aperture of 85-90% of the pin area. This design recommendation allows the component to settle to the pad better, rather than floating on top of the solder paste.

Figure 6. Example of stencil apertures and package outline correspondence



In many cases incorrectly designed stencils (full opening or too large apertures) resulted in an excessive number of solder voids. These issues have been fixed by small modifications of the stencil design.

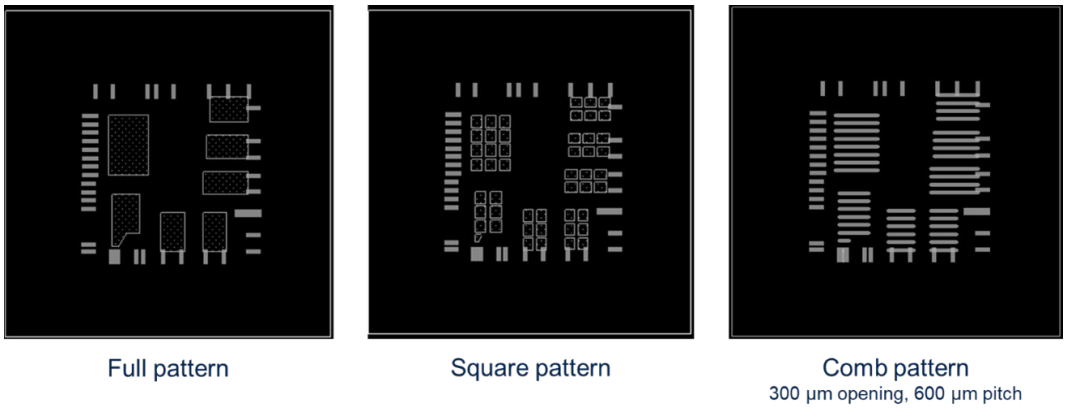
PCB manufacturers usually adjust these parameters based on the experience of their soldering equipment.

ST performed some soldering trials to identify possible optimizations to further improve stencil design if an excessive amount of voids is observed. The stencil pattern was one of the variables considered in these trials. Possible types of stencil patterns are depicted in Figure 7.

The “default” pattern typically used by board manufacturers is the ‘square’ pattern.

According to STMicroelectronics experiments, the stencil using a ‘comb’ pattern is better in reducing the formation of voids. The ‘comb’ pattern has been used to improve void amount when results with the ‘square’ one were not satisfactory.

Figure 7. Possible types of stencil patterns



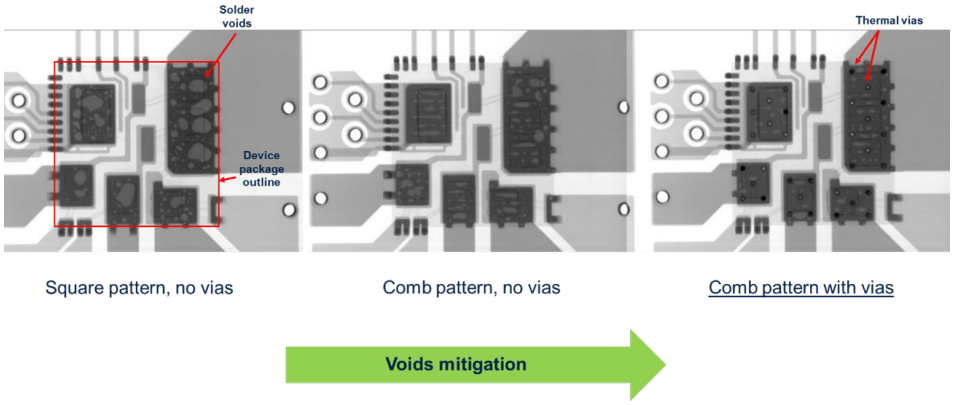
1.3.3 Other recommendations

Another method that can help reduce the presence of voids is to extend the duration and reduce the slope of the reflow profile as much as possible, in compliance with solder paste manufacturer’s guidelines, while keeping a low peak temperature (for example, 240 °C instead of 250 °C).

1.3.4 X-ray solder voids results vs. type of stencil pattern and use of PCB vias

Figure 8 contains X-rays of the same device soldered on the PCB using different stencil patterns and the addition of vias.

Figure 8. Voids presence vs. stencil pattern



As explained above, the use of a comb pattern combined with vias is the solution that ensures the best result in terms of voids.

2 Layout considerations

This section of the document provides comprehensive guidelines for designing the layout of System-in-Packages (SiP) in Quad Flat No-lead (QFN) packages. Proper PCB layout is crucial for ensuring optimal performance, reliability, and manufacturability of QFN packages. This document covers key considerations and best practices for layout design.

2.1 PCB design considerations

- **Footprint**: footprints depict the land pattern of a component on a bare PCB. It is the region in which the component is soldered. It is basically the physical interface between the board and the component.
- **Pad design**: footprint rules specify how pads should be arranged and distanced from other pads in a board layout. They also demarcate the spacing between other components, drill holes, and the board edge. An inaccurate pad layout is responsible for wrong component locations, leading to assembly issues. The pad dimension and spacing between pads are essential items that need to be checked. Ensure symmetry in the component pads; it avoids tombstoning, a footprint defect in which the components are completely or partially lifted from the PCB pad. Pad size and shape: ensure that the opposite pads of the same component are in the same size and shape. Maintain minimum clearance between footprint pads and board edge. This practice supports depanelization. It is common to have around 50-75 µm (2-3 mils) of clearance between the pad and the mask.
- **Solder mask**: use a non-solder mask defined (NSMD) pad design for better solder joint reliability. Solder mask bridge: This is the solder mask between two pins. It is typically 100 µm to 200 µm (4 mils to 8 mils). If it is less than this value, it leads to shorts between the pins. It is recommended the use of rounded finger pads to prevent solder bridging.
- **Thermal vias**: implement thermal vias under the thermal pads for efficient heat dissipation, to transfer effectively the heat from the top copper layer of the PCB to the inner or bottom copper layers. Add vias uniformly under the exposed pads, bearing in mind constraints due to underlying tracks clearance. The recommended via diameter is 0.25 mm (10 mils) or less. Although more thermal vias improve the package thermal performance, there is a point of diminishing returns, therefore the recommended via spacing is 1 mm (39 mils) (see Figure 5).
- **Copper areas**: copper areas on the same layer of the SiP and in the inner layers act as heat sinks for the QFN device. Assuming the device is mounted on the top layer, top copper areas should be made as large as possible. Inner or bottom layer copper planes can also can be connected to exposed pad using vias and should be made as large as possible (see Figure 11).

2.2 Ground connection

A typical application using SiP embedding MOSFETs (for example, PWD5T60) has an MCU driving the power stage located inside the SiP. This is also the most comprehensive case since there are typically four types of ground connections:

1. **MCU ground** (VSS and VSSA): It is the ground reference for the MCU, operational amplifiers, comparators, and analog-to-digital converters.
2. **Driver signal ground** (GND and EPAD): It is the signal ground of the internal gate driver.
3. **Driver power ground** (PGND): It is the power ground of the internal gate driver and brings the gate current of the low-side drivers.
4. **Power stage ground**: It is the grounding point for the currents flowing into the power stage (that is, the MOSFETs embedded into the SiP).

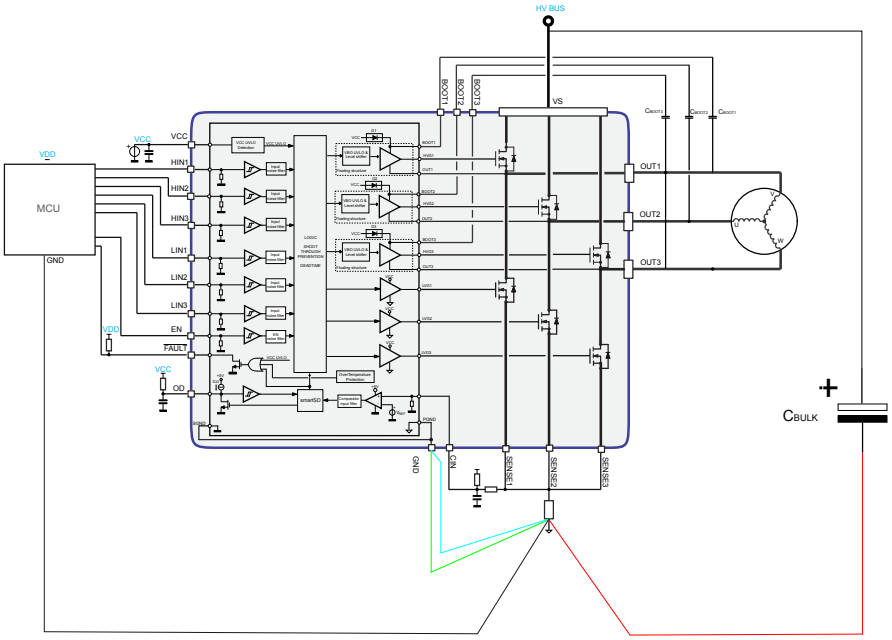
Often, as in the PWD5T60 SiP shown in Figure 9, signal and power grounds of the driver are joined internally on the package frame.

The preferred connection point of the grounds is on the shunt resistors.

This connection is recommended to reduce the effect of parasitic inductances that create voltage spikes on the paths carrying large current or high di/dt current signals, such as the paths including MOSFETs, shunt resistors, and bulk capacitors.

Ensure all ground pads, including exposed pads, are connected to a solid ground plane that offers the advantage to act as a shield for sensitive signal traces to minimize electromagnetic interference (EMI).

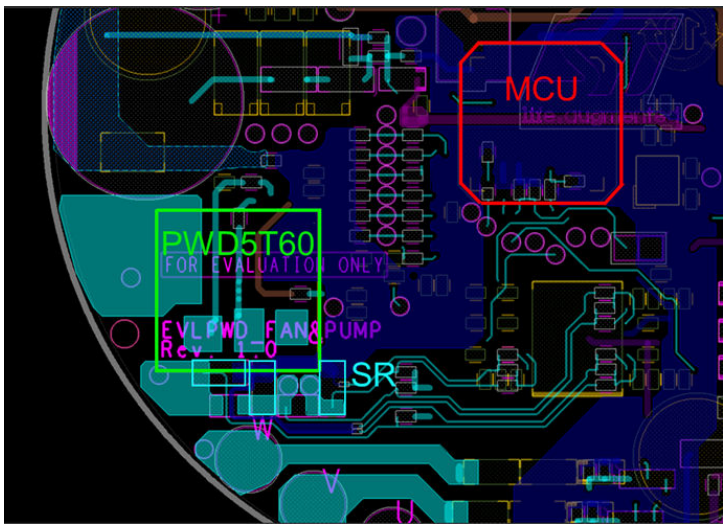
Figure 9. **Ground connection of EVLPWD5T60 board**



2.2.1 Example of ground connection

It is recommended to connect all VSS pins of the MCU together by the shortest possible path to reduce the risk of creating voltage difference between the VSS pins above the absolute maximum ratings stated in the device datasheet, due to the current induced by external disturbance and to reduce the impedance of ground return path. The best practice is to connect the VSS lines to the ground plane through the vias placed as close as possible to the device VSS pins. The ground plane should be solid without slots or holes which may cause an increase of the ground plane impedance. Splitting analog and digital ground is not recommended. While it may have a questionable impact on noise distribution from the digital to analog domain, it always shows a worse EMC performance (AN1709 - EMC design guide for STM8, STM32, and legacy MCUs). In Figure 10 there is an example of ground connection between an MCU and SiP embedding MOSFETs in a 2-layer PCB. The blue shape is the connection of SiP and MCU ground near the shunt resistor to minimize noise and avoid unbalanced ground references.

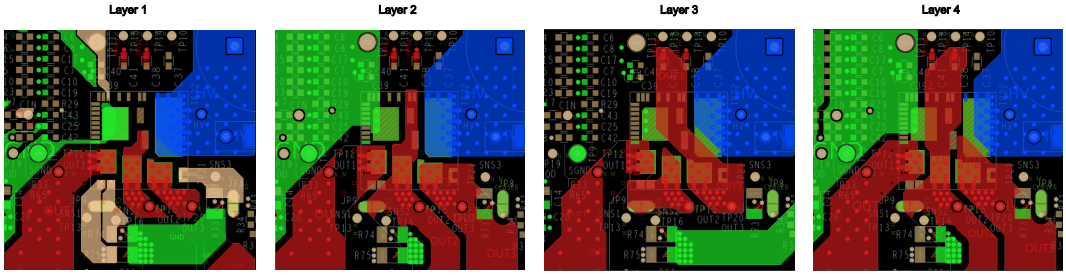
Figure 10. **Example of ground connection of PWD5T60 EVL FAN&PUMP design (2L-PCB)**



2.3 Power dissipation through exposed pads

To ease power dissipation as much as possible, which is a major concern for all SiP embedding MOSFETs, it is recommended to insert a large copper area around the exposed pads (such as DRAIN of embedded MOSFETs) on the same layer as the component and, if possible, to add such copper areas on the remaining layers too. It is recommended to insert vias below the exposed pads to convey the heat from the component to adjacent layers.

Figure 11. Example of power dissipation through exposed pads and copper areas



The images above show an example of the dissipative area created on 4 layers for both the ‘HV’ and the ‘OUTx’ pads of the PWD5T60 triple half-bridge; vias are inserted uniformly in the exposed pads.

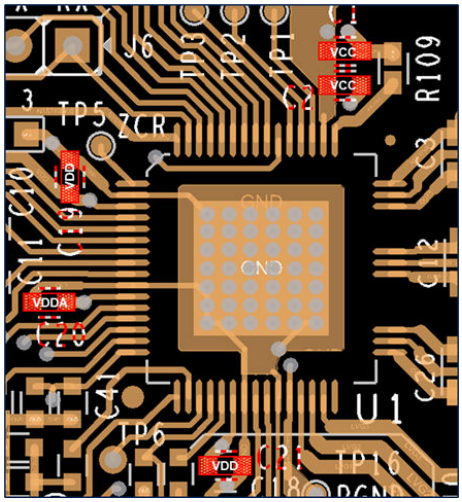
2.4 Decoupling capacitors

To avoid unwanted spikes, place decoupling capacitors near the IC. SMT ceramic capacitors (or different types of low-ESR and low-ESL capacitors) must be placed close to each supply rail pin. A 100 nF decoupling capacitor must be placed next to all MCU and driver supplies, as close as possible to the pins, to filter high-frequency noise and spikes. To provide local storage for pulsed current, a second capacitor with a value in the range between 1 µF and 10 µF should also be placed nearby.

If possible, use a multilayer PCB with a separate layer dedicated to ground and another for the MCU supply. This provides good decoupling and a good shielding effect for the MCU.

As a good practice, it is suggested to add R-C filters – such as 100 Ω / 33 pF – close to logic inputs of the device (driver input pins), especially for fast switching or high-voltage applications. Minimize the number of layer transitions to reduce signal degradation and maintain controlled impedance for high-speed signal traces.

Figure 12. Example of decoupling capacitor placement



2.5 Power section

With reference to Figure 13, the paths circled in green are subject to high currents and high dI/dt but are inside the SiP, as well as the gate driving circuitry; therefore, these paths are already optimized to ensure optimal performance.

While the PCB tracks circled in red should be as short and wide as possible to minimize parasitic inductance and resistance. If possible, use thicker copper traces or planes for high current paths.

The bulk capacitor should be placed as close as possible to the SiP.

Figure 13. Power paths around the SiP embedding MOSFETs

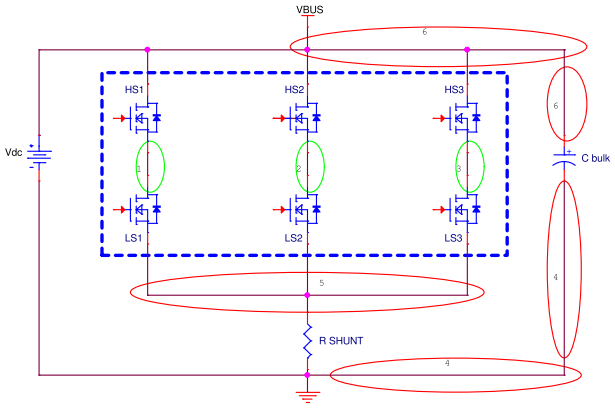
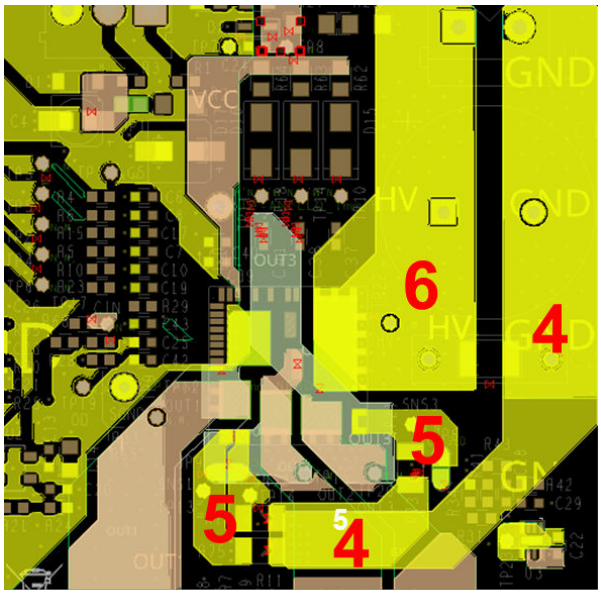


Figure 14. Same critical paths highlighted in a typical layout



Other suggestions include:

- use solid power planes to reduce impedance and improve power delivery.
- implement continuous ground planes to minimize noise and provide a low impedance return path for the currents.

2.6 Current sensing

To optimize shunt resistor reading, use Kelvin sensing with minimal area between tracks to bring the shunt signal to the amplifier (Figure 15).

Figure 15. Optimal sensing of signal across shunt resistor

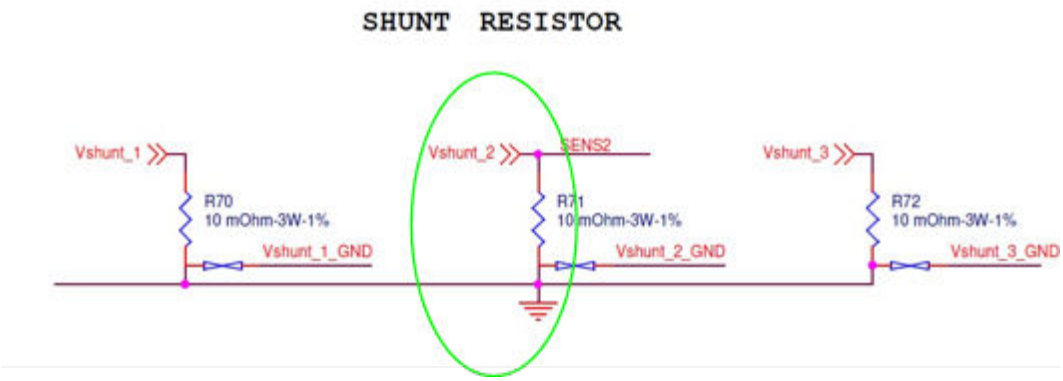
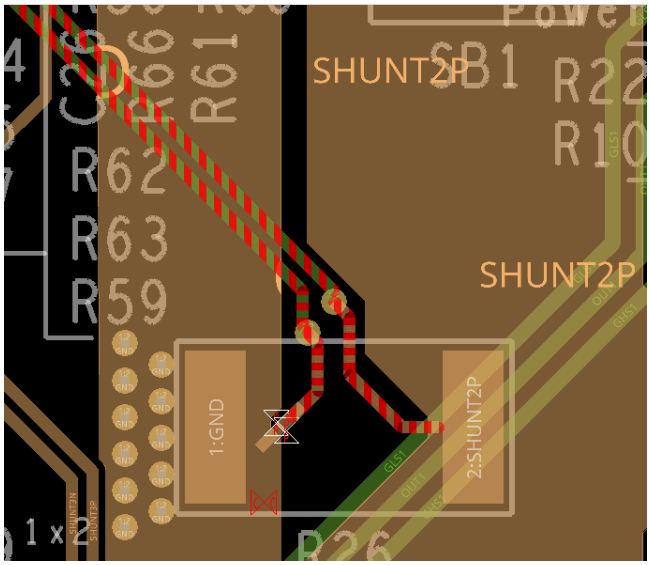


Figure 16. Sensing of current signal in a typical layout



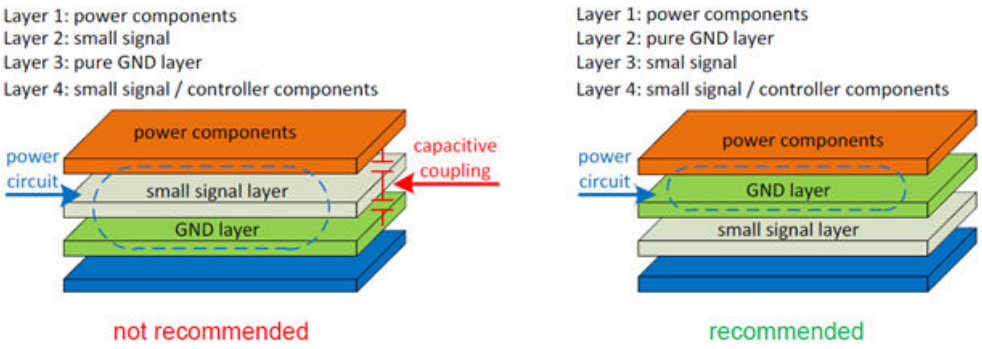
2.7 Radiated noise from PCB tracks

To minimize radiated emission from a PCB hosting power SiP:

- keep power or signal traces as short as possible
- keep power or signal loops as small as possible
- shield signal from power traces
- if possible, route traces above GND plane

Ideally, the PCB design should be structured as depicted in Figure 17. In case of a 2-layer design, signal traces must be kept isolated from power traces and high-frequency signal tracks should be shielded with ground traces or planes around them.

Figure 17. Optimal sensing of signal across shunt resistor



3 Conclusion

The solderability process for SiP in QFN packages requires careful consideration of storage, handling, component placement, PCB design, solder paste application, and reflow soldering.

Proper layout design is essential for the performance, reliability, and manufacturability of this type of device.

By following the guidelines provided in this application note, PCB designers can optimize electrical and thermal performance, and manufacturers can achieve reliable and high-quality solder joints, ensuring the performance and longevity of their electronic assemblies.

For further assistance or specific inquiries, contact the ST technical support team.

4 Appendix: evaluation board examples

Here below some examples of ST evaluation boards and their soldering materials and process.

4.1 EVALPWD5F60

Figure 18. **Picture of EVALPWD5F60 board**

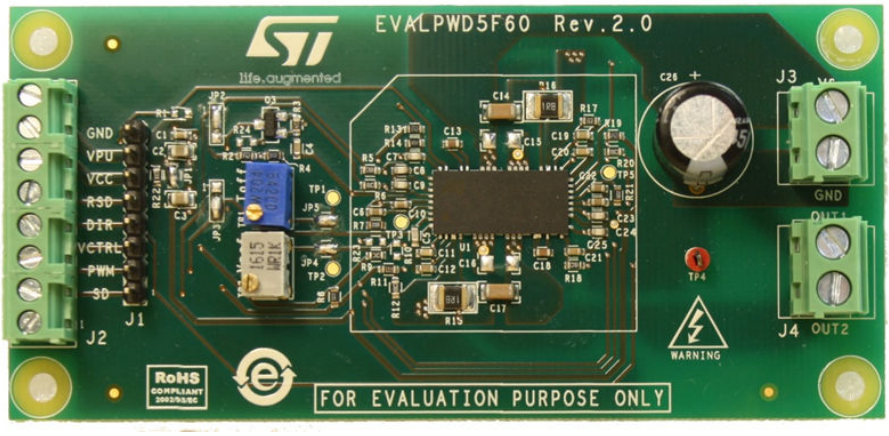
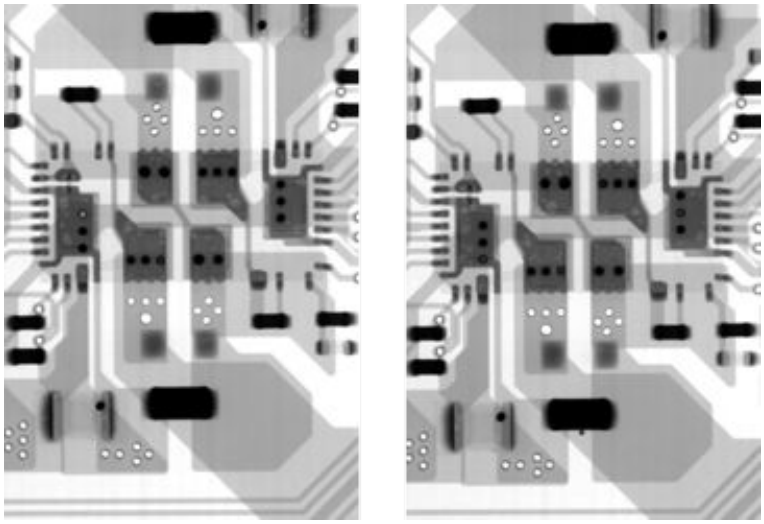


Figure 19. **X-rays of EVALPWD5F60 board**



4.1.1 EVALPWD5F60 soldering process

The exact soldering process is influenced by specific characteristics of the board (dimensions, components density, # of PCB per "panel", etc.) and must be fine-tuned at specific assembly line.

Characteristics of evaluation board and PWD5F60:

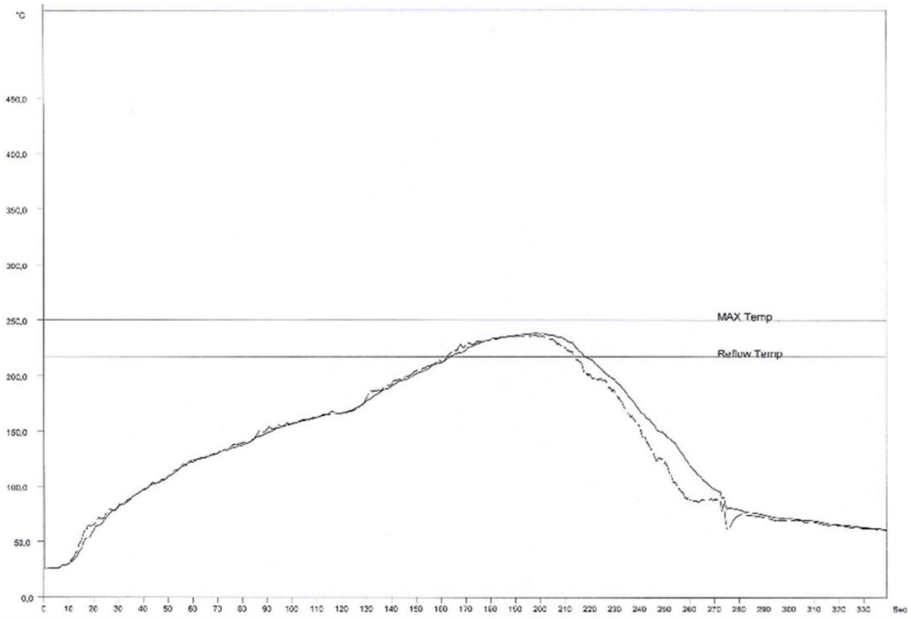
- PCB surface finishing: NiAu. Thickness: 3u<Ni<5u Au>0.05u
- PCB copper thickness 35 µm
- PWD5F60 lead frame finishing is pure Tin

Table 3. **Soldering process for EVALPWD5F60 board**

Parameter	Value
Laminate type	FR4 DE104
Soldering paste	ALPHA® OM-338-T, Type 3
Stencil thickness	100 µm
Stencil design	Square

4.1.2 EVALPWD5F60 reflow profile

Figure 20. **Soldering process for EVALPWD5F60 board**



4.2 EVLPWD5T60

Figure 21. **Picture of EVLPWD5T60 board**

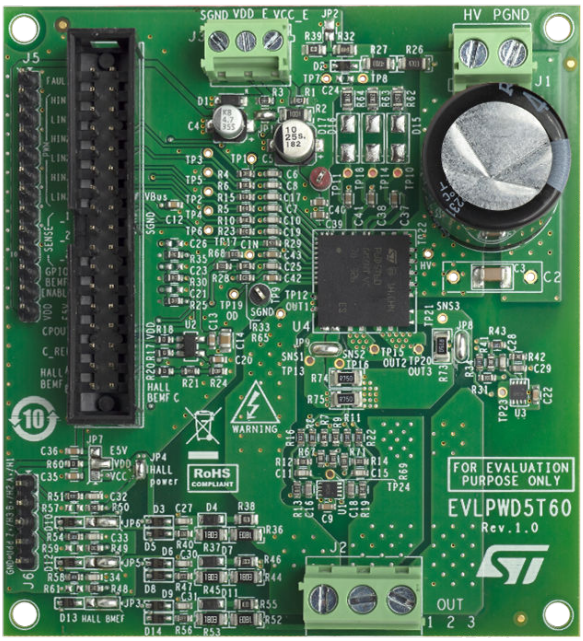
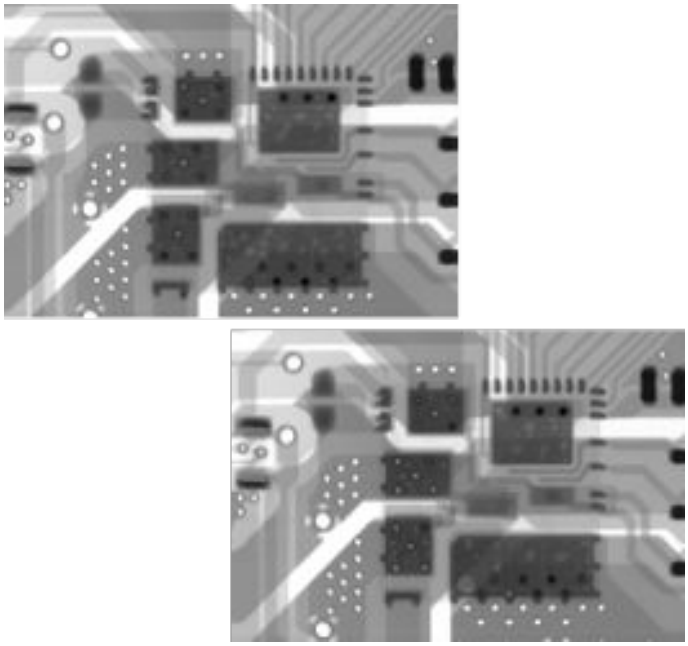


Figure 22. **X-rays of EVLPWD5T60 board**



4.2.1 EVLPWD5T60 soldering process

The exact soldering process is influenced by specific characteristics of the board (dimensions, components density, # of PCB per "panel", etc.) and must be fine-tuned at specific assembly line.

Characteristics of evaluation board and PWD5T60:

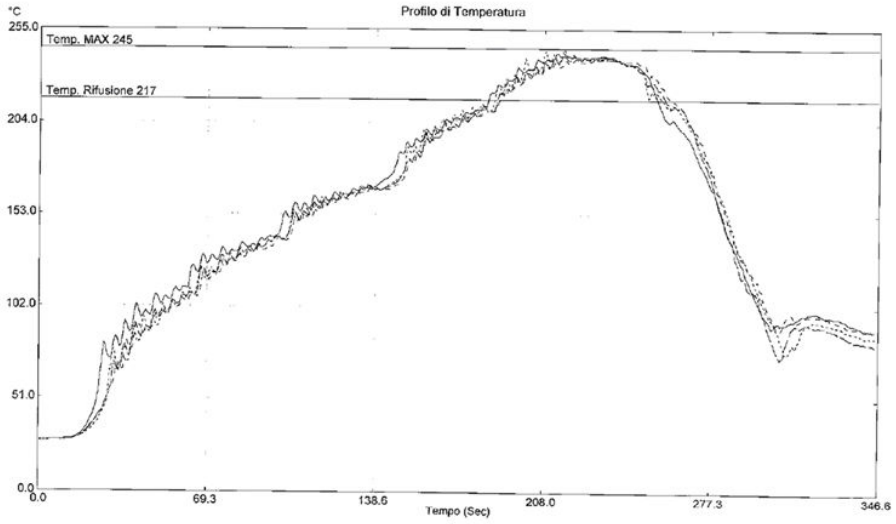
- PCB surface finishing: NiAu. Thickness: 3u<Ni<5u Au>0.05u
- PWD5T60 lead frame finishing is pure Tin

Table 4. **Soldering process for EVALPWD5F60 board**

Parameter	Value
Laminate type	370HR
Soldering paste	ALPHA® OM-338-T
Stencil thickness	127 µm
Stencil design	Comb

4.2.2 EVLPWD5T60 reflow profile

Figure 23. **Soldering process for EVLPWD5T60 board**



Revision history

Table 5. **Document revision history**

Date	Version	Changes
19-Dec-2024	1	Initial release.

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