Guidelines for the proper use of the L99DZ200G in the door zone control applications

Introduction

This document provides guidelines for the proper use of the L99DZ200G in the door zone control applications. It supports the user with the necessary steps to integrate the device into its application. It shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

This document is targeted at automotive system engineers, hardware engineers, software engineers, quality managers and project managers involved in the development of electronic door control units for automotive applications.

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1 Introduction to L99DZ200G device

The L99DZ200G is a door zone system IC providing electronic control modules with enhanced power management power supply functionality, including various standby modes, as well as LIN and CAN physical communication layers. The device has two low drop voltage regulators to supply the system microcontroller and external peripheral loads such as sensors and provides enhanced system standby functionality with programmable local and remote wake-up capability. Moreover, the 7 high-side drivers increase the system integration level; high-side drivers 7, 8 and 9 support the constant current mode for LED module with high input capacitance.

The external MOS transistors in H-bridge configuration can be driven in PWM mode up to 50 kHz. An additional gate driver can control an external MOSFET in high-side configuration to supply a resistive load connected to GND (for example mirror heater). An electrochromic mirror glass can be controlled using the integrated SPI-driven module with an external MOS transistor. All the half bridge and high side output are OC protected and implement an open-load diagnosis, the ST standard SPI interface (4.0) allows control and diagnosis of the device and enables generic software development.

1.1 Application fields and target markets

The L99DZ200G is designed for door zone application.

1.2 Purpose of this document

This document is composed of several components of chipset applicable experiences. It can speed up hardware design at the system level and serves as a guideline as well.

It provides the following contents from several aspects:

- Detailed descriptions of the chip's functions and technical specifications, including its input/output interfaces, clock frequency, and power consumption.
- Guidance on how to properly design and configure systems to use the chip.
- Include circuit diagrams, pin assignments, layout and wiring recommendations, etc.
- Ensure the correct connection and interaction of the chip with other components and peripherals.
- Offer practical application examples and case studies, showcasing the chip's usage in different fields.

If users encounter problems while using the chip, this document typically provides troubleshooting and failure handling guides. These guides list potential issues and their solutions, helping users to quickly solve technical challenges related.

This document also includes information about how to optimize performance, reduce power consumption, and best practice recommendations. It can help designers and engineers fully leverage the functions and performance of the chip.

2 Overview of L99DZ200G chip characteristics

Figure 1. Block diagram
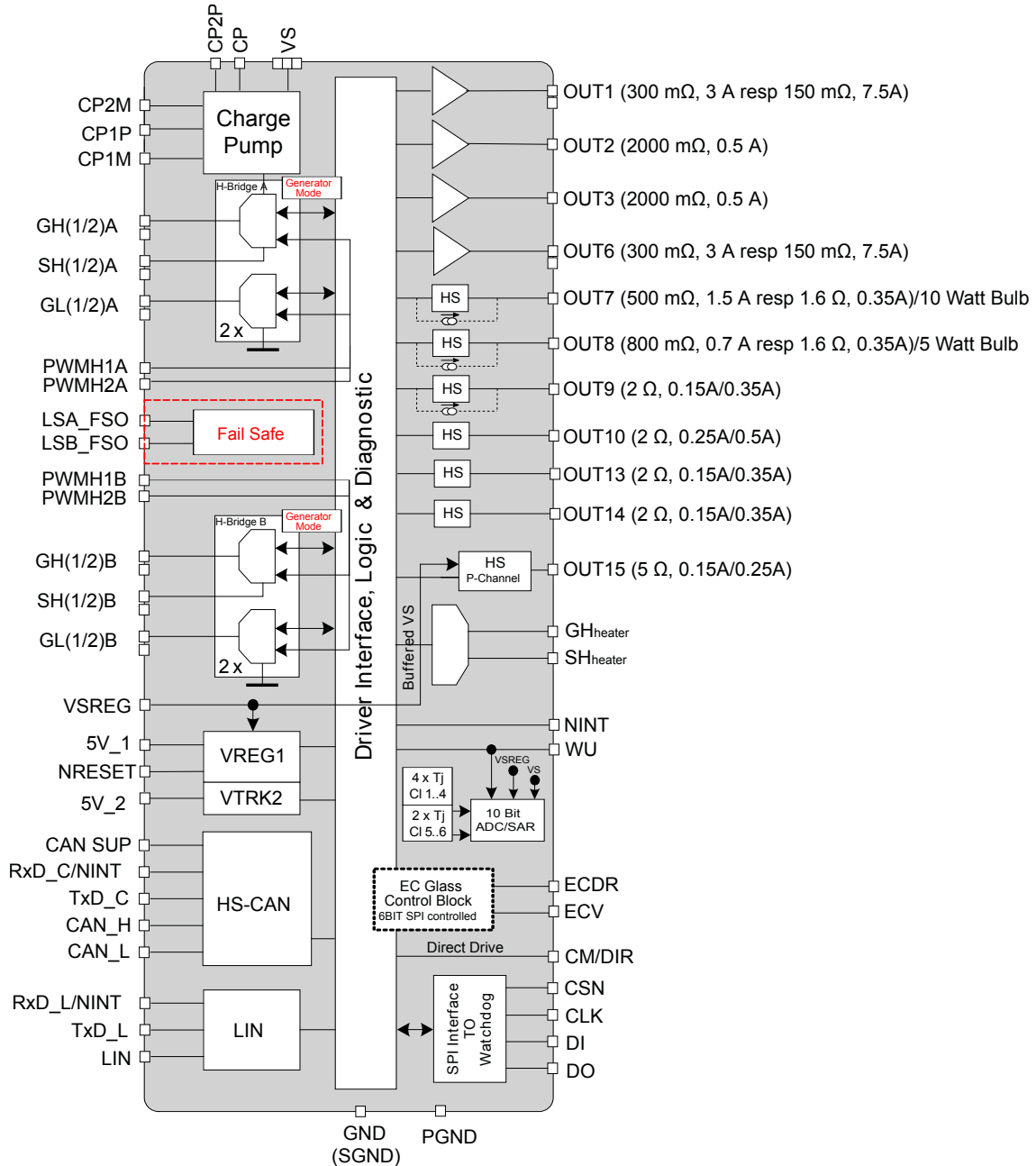
2.1 Packaging and size information

LQFP-64 (10x10x1.4 mm) with exposed pad down.

3 Operating modes
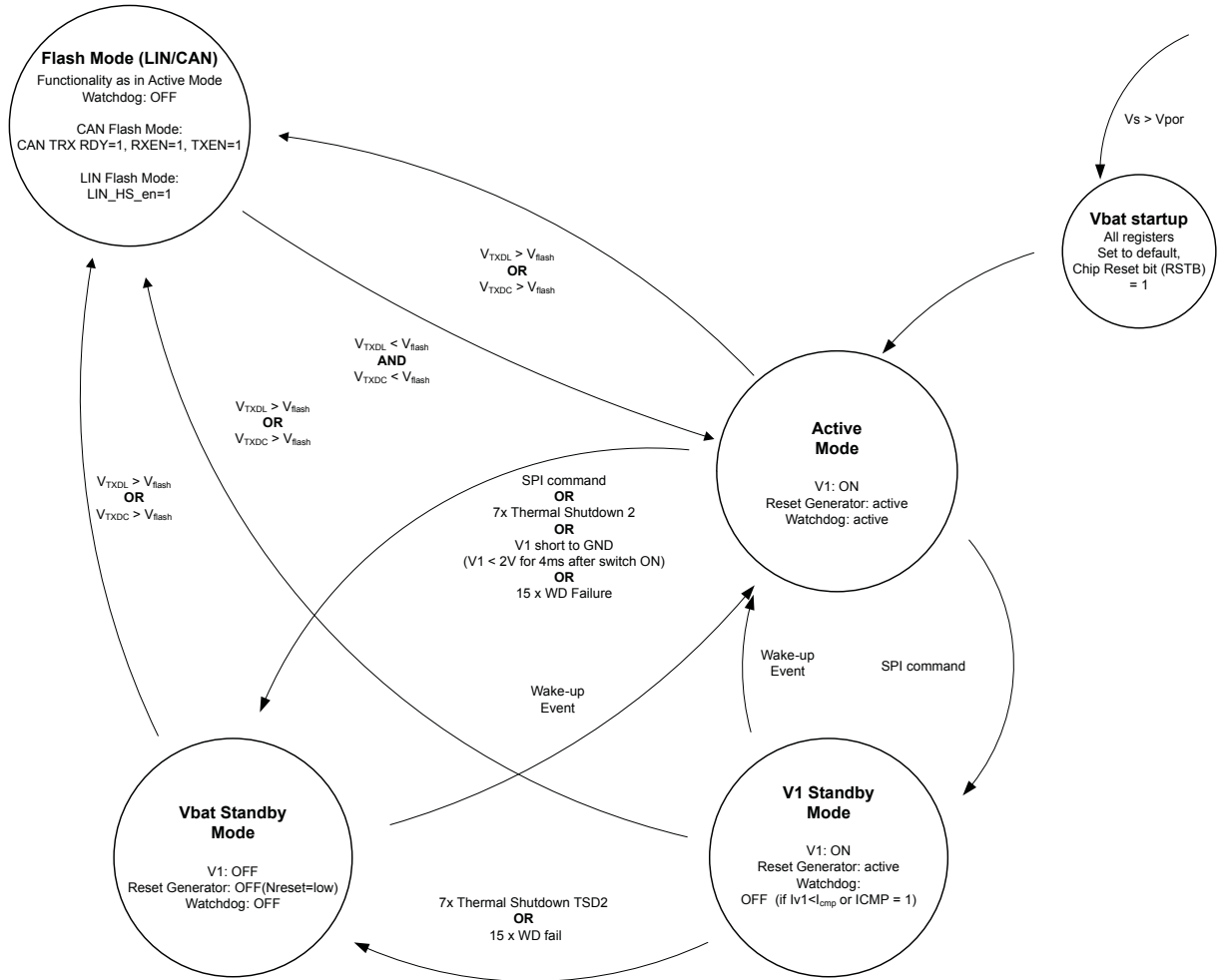
3.1 Main operating modes

Figure 2. Operating mode

Table 1. Operating mode features

Active	Flash/Debug	V1_Standby	VBAT_Standby
All peripherals are ON	All peripherals are ON Watchdog is OFF CAN is enabled by default	5V1 is ON CAN and LIN are OFF Power outputs (except OUT 15) are OFF OUT15 and 5V2 are switched ON or OFF according to SPI configuration. Watchdog is OFF dependent on ICMP setting.	5V1, CAN and LIN are OFF Power outputs (except OUT15) are OFF OUT15 and V2 are switched ON or OFF according to SPI configuration. Watchdog is OFF

3.2 Flash mode

To program the system microcontroller via LIN or HS CAN bus signals (watchdog is disabled).

The flash modes are entered by applying an external voltage at the respective pin:

- $V_{TxDL} \geq V_{flashH}$ (CAN flash mode)
- $V_{TxDC} \geq V_{flashH}$ (LIN flash mode)

In LIN flash mode, the maximum bitrate is automatically increased to 100 Kbit/s (LIN_HS_EN = 1).

A transition from flash modes to V1_Standby or VBAT_Standby mode is not possible.

At exit from flash mode ($V_{TxDL/C} < V_{flashL}$), no NReset pulse is generated, and the watchdog starts with a long open window.

Note: *For more information and operation details, please refer to section 4.3.2 of the device datasheet.*

3.3 Debug mode

To allow software debugging, the L99DZ200G has a debug mode. In debug mode, the watchdog is deactivated, all other functions are able to work, and CAN is enabled by default.

Note: *Making sure properly enter debug mode, it is strongly recommended to connect the PWMH1B pin to the V1 pin.*

To enter in debug mode, follow 2 steps:

1. Apply at power-up a high-level voltage (5 V) on the PWMH1B input pin; this procedure shall be done before the rising edge of the NRESET pin. It is strongly recommended that 5V_1 and PWMH1B pins are tied together by means of a jumper, avoiding configurations in which the 5 V for the PWMH1B pin are externally provided;
2. After a time interval longer than t_{V1R} (typ. 2 ms), remove the jumper between 5V_1 and PWMH1B so the PWMH1B signal goes low thanks to its internal pull-down resistor. Consequently, the NRESET output rises at its highest value and the L99DZ200G is from now on in SW-Debug mode.

Note: *For more information and operation details, please refer to "Figure 20. Sequence to enter in SW-Debug mode" in the datasheet.*

To exit from debug mode, the microcontroller can set the DEBUG_EXIT bit in CR22. The L99DZ200G exits from SW-Debug mode and the watchdog starts a long open window.

3.4 V1_Standby mode

The transition from active mode to V1_stanby is controlled by SPI, writing the bits PARITY, STBY_SEL and GO_STBY (bit3, bit2 and bit1 of CR1 register) as per the Table 2.

Note: *Before going to V1_Standby or VBAT_Standby mode, OL_H1L2_x, OL_H2L1_x and GH_OL_EN bits respectively in CR10, CR21 and CR11 must be set to 0 to achieve the specified current consumption. After woke up from VBAT_Standby or V1_Standby mode, the CR1 Bit1, 2 and 3 do not return to the default value (0b000).*

After the V1 standby command is received (CSN low to high transition), the device enters V1_Standby mode immediately and, considering I_{CMP} bit value, there are two scenarios:

- If I_{CMP} = 0 (default value), L99DZ200G watchdog starts a long open window and, if V1 load current drops below the I_{CMP_fal} (1.5 mA ÷ 6 mA), the watchdog is deactivated.
- If I_{CMP} = 1, the watchdog is deactivated upon transition into V1_Standby mode without monitoring the V1 load current.

Note: *The procedure to set the ICMP value is made by two consecutive SPI commands. In other words, writing ICMP (CR 22) = 1 is only possible if ICMP_CONFIG_EN (CFR) is set to 1 in the previous SPI message. The ICMP_CONFIG_EN bit is reset to 0 automatically with the next SPI command.*

After entering V1 standby mode, 5V1 remains active to supply the microcontroller in a low-power mode. Power outputs (except OUT 15), as well as the LIN and CAN transmitters are switched OFF.

The OUT 15 and 5V2 remain in the configuration programmed before the standby command.

The interrupt signal (NINT) indicates a wake-up event from V1_Standby mode. The RxD_L/NINT pin is pulled low for 56 µs, after a reaction time t_{Int_react} from the wake-up event.

3.5 VBAT_Standby mode

The transition from active mode to VBAT_Stanby is controlled by SPI [2], writing the bits PARITY, STBY_SEL and GO_STBY (bit3, bit2 and bit1 of CR1 register) as per the Table 2.

Note: *Before going to V1_Standby or VBAT_Standby mode, OL_H1L2_x, OL_H2L1_x and GH_OL_EN bits respectively in CR10, CR21 and CR11 must be set to 0 to achieve the specified current consumption. After woke up from VBAT_Standby or V1_Standby mode, the CR1 Bit1, 2 and 3 do not return to the default value (0b000).*

In VBAT_Standby mode, the voltage regulators 5V1 and 5V2, the power outputs (except OUT15) as well as LIN and CAN transmitters are switched off.

The OUT15 remains in the configuration programmed before the standby command to enable supply (static or cyclic) of external contacts.

A NReset pulse is generated upon wake-up from VBAT_Standby mode.

Table 2. STBY_SEL and GO_STBY bits

PARITY	STBY_SEL	GO_STBY	
0	1	1	Go to V1_Standby
1	0	1	Go to VBAT_Standby
0	0	0	No transition to standby
1	1	0	No transition to standby

4 Wake-up

A wake-up event turns the L99DZ200G from standby mode (V1_Standby or VBAT_Standby) back into active mode.

Note: *At wake-up from VBAT_Standby mode the NRESET signal (with 2 ms timing) is generated, otherwise, an interrupt signal in RXDL/NINT pin is generated.*

To prevent the system from a deadlock condition (no wake-up from standby possible), it is not allowed to disabling both CAN wake-up and LIN wake-up (bits LIN_WU_EN and CAN_WU_EN in CR1). In case the user tries to disable CAN and LIN wake-up at the same time (writing LIN_WU_EN = CAN_WU_EN = 0), the device rejects the command. All wake-up sources are configured to default values and the SPI error bit (SPIE) in the global status byte is set.

In case of wake-up from VBAT_Standby the NRESET signal (with 2 ms timing) is generated, while for wake-up from V1_Standby the RXDL/NINT (interrupt) signal is generated.

The Table 3 shows all wake-up sources with related description.

Table 3. Wake-up events functions

Wake up source	Description
LIN bus activity	Can be disabled by SPI
CAN bus activity	Can be disabled by SPI
Level change of WU	Can be configured or disabled by SPI
I_{V1} > Icmp	The device remains in V1_Standby mode but watchdog is enabled (If I_{CMP} = 0) No interrupt is generated
Timer interrupt / Wake-up of µC by TIMER	Programmable by SPI: - V1_Standby mode: the device wakes up and Interrupt signal is generated at RxDL/NINT when the programmable time-out has elapsed - VBAT_Standby mode: the device wakes up after programmable timer expiration. The 5v1 regulator is turned on and the NReset signal is generated when the programmable time-out has elapsed
SPI access	Always active (except in VBAT_Standby mode) Wake-up event: CSN falling on edge
V_S overvolatge	Only when generator mode is enabled (GENERATOR_MODE_EN = 1 in CR22)

4.1 LIN wake-up

The device wake-up from LIN occurs only if the LIN_WU_EN bit in CR1 is set.

Two types of signals (configurable by bit LIN_WU_CONFIG in CFR at address 0x3F) on the LIN bus are able to wake-up the device:

- If LIN_WU_CONFIG = 0 (default value) a Recessive-Dominant-Recessive pattern (according to LIN 2.2a) with dominant state duration higher than t_{dom_LIN} is requested to wake up L99DZ200G (see the Figure 3).

NB: A dominant time of at least 150 µs must be identified as a wake-up pattern according to LIN 2.2a, even if shorter dominant times may wake-up the device since $t_{dom\_LIN\_min}$ = 28 µs.

- If LIN_WU_CONFIG = 1 a state change recessive to dominant or dominant to recessive (according to LIN 2.1) is requested to wake-up L99DZ200G.

Note: *An unwanted wake-up can occur if, when the device is set in standby mode with LIN in recessive (dominant) state, there is a dominant (recessive) level at LIN for a time longer than t_{LINBUS} (typ. 64 µs).*

Figure 3. **Wake-up behavior according to LIN 2.2a**

Voltage at LIN-Pin of LIN Physical Layer device
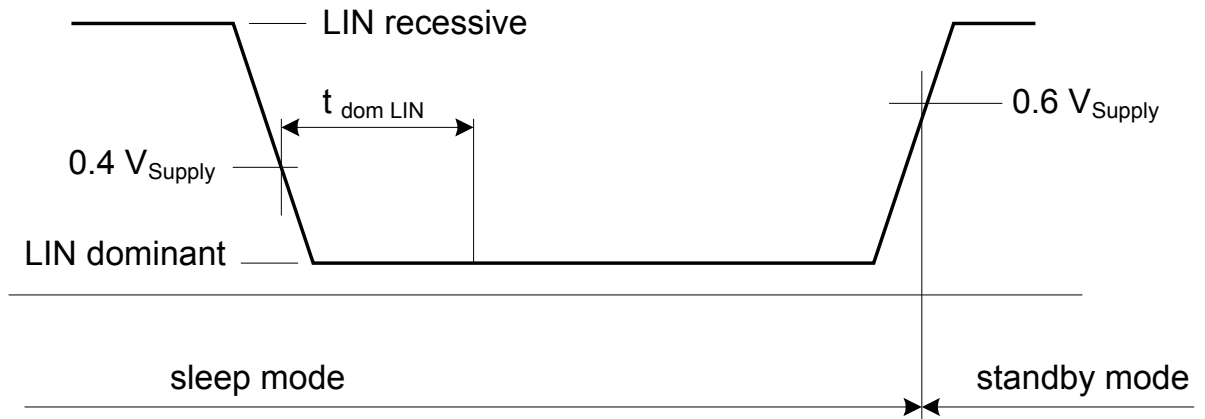
Important: *If LIN wake-up is not used (LIN_WU_EN bit in CR1 is not set), it is highly recommended to set LIN_WU_CONFIG = 1 (bit22 in CFR). This avoids an extra current consumption in standby mode (both in V1_Standby mode and in VBAT_Standby mode) that occurs if LIN bus or TxD_L pin are stuck to GND during transition from active mode to stanby mode.*

4.2 CAN wake-up

The device wakes up from CAN occurs only if the CAN_WU_EN bit in CR1 is set.

The device can be woken up by a pattern on CAN bus that satisfies the following requirements:

- The CAN interface wake-up receiver must receive a series of two consecutive valid dominant pulses (each one longer than t_{filter}) separated by a recessive one (longer than t_{filter}).

Note: *Please keep in mind that the t_{filter} range specified in the datasheet (0.5~5 µs) is not a safety range. To make sure wake up the device, the pulses should be longer than 5 µs.*

- The two pulses must occur within a time frame not longer than t_{wake}.

Note: *Please keep in mind that the t_{wake} range specified in the datasheet (0.5~5 ms) is not a safety range. To make sure wake up the device, the pulses should be shorter than 0.5 ms.*

- Wake-up occurs when the duration of the second pulse becomes longer than t_{filter}.

Independently on device mode (ACTIVE or STANDBY), the t_{wake} starts from BUS transition recessive to dominant (see the Figure 4).

In CAN TRX STBY mode, the CAN transmitter is disabled and the RXDC pin is kept at high (recessive) level. CAN receiver can detect a wake-up pattern (WUP).

Figure 4. CAN wake-up patterns

CAN pattern wakeup

CAN pattern wake-up with dominant state before Standby
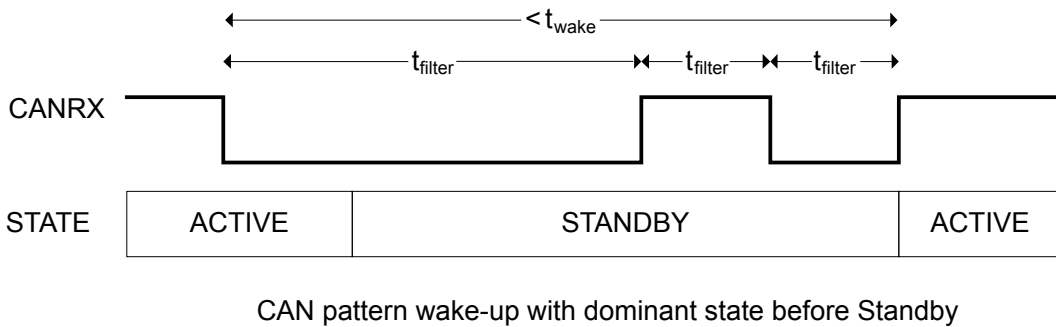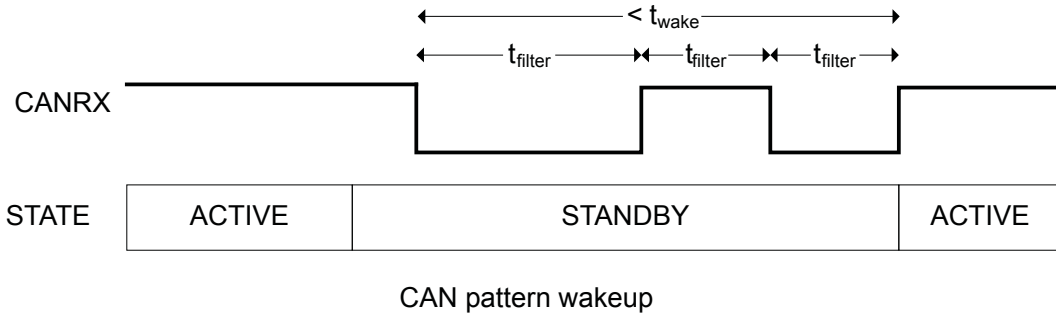
4.3 WU input WU

The WU pin (configured by default for input voltage measurement) can be configured as a wake-up source (WU_CONFIG bit in CFR at 0x3F address). When configured as a wake-up input it is sensitive to any level transition (either positive or negative edge).

Wake up mode can be configured for static or cyclic monitoring of the WU input voltage level (WU_FILT_1 and WU_FILT_0 in CR1).

To minimize current consumption in standby mode, follow these recommendations:

- Set the current source configuration (WU_PU = 1 in CR1) for active low contacts.
- Set the current sink configuration (WU_PU = 0 in CR1) for active high contacts.
- Keep $V_{WU} < 1$ V or $V_{WU} > V_{Sreg} - 1.5$ V.

If WU pin is unused, it is recommended to connect it to ground.

Figure 5. Internal scheme of WU input
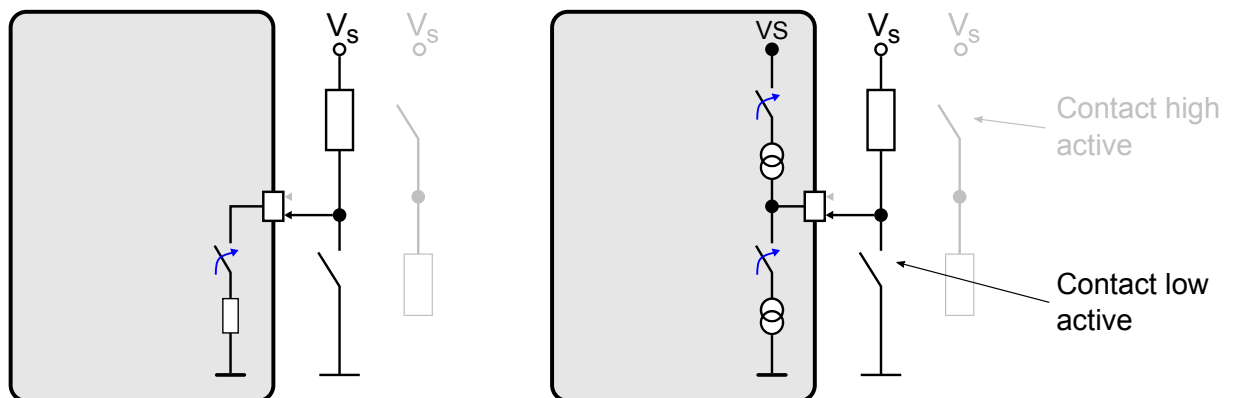
4.3.1 Static wake-up monitoring

In case of static monitoring, a filter time of t_{wu_stat} (64 µs) is implemented. The filter is started when the input voltage passes the specified threshold V_{WUthx} (typically 0.45 V_{Sreg} for negative edge and 0.55 V_{Sreg} for positive edge) as shown in the Figure 6 and Figure 7.

Wake-up status bit (WU_STATE bit in SR1) is set only if the threshold is passed for more than t_{wu_stat}.

To reduce current consumption in standby mode, R_{WU_act} is activated just after the external interrupt request (as soon as $V_{WU} > 1$ V or $V_{WU} < V_{Sreg} - 1.5$ V as shown in the Figure 6 and Figure 7, so it is highly recommended to dimension external resistors to make sure that $V_{WU} < 1$ V or $V_{WU} > V_{Sreg} - 1.5$ V, when the contact is open, otherwise, the quiescent current will be higher than the specified value on datasheet (I_{WU_stdby}).

Figure 6. Wake-up request for active high contact
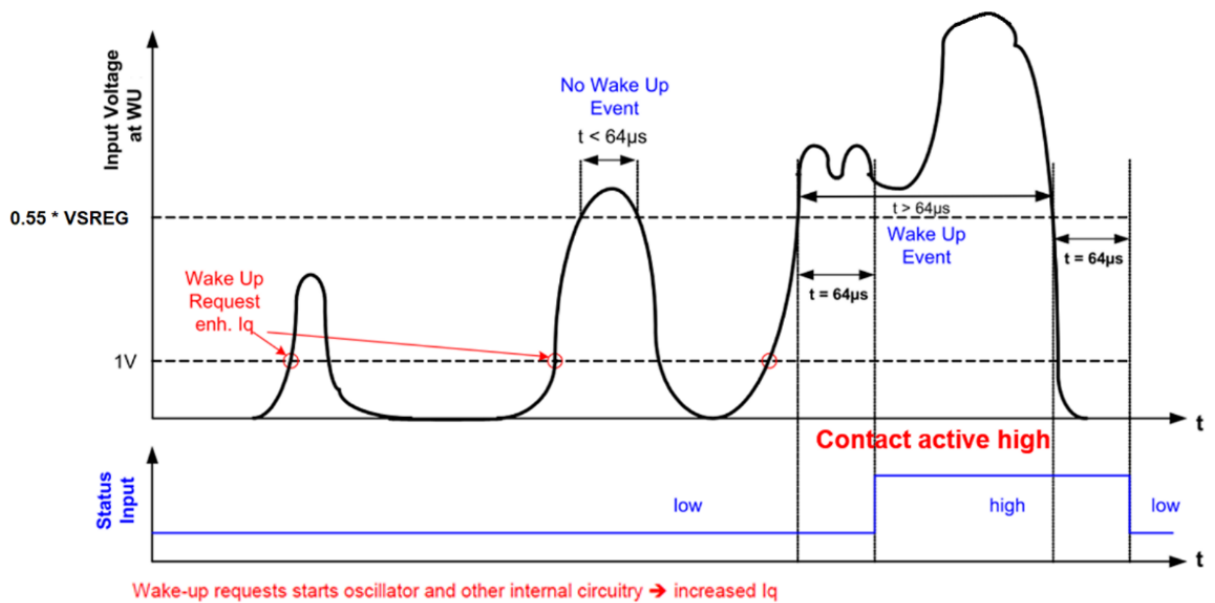
Figure 7. Wake-up request for active low contact
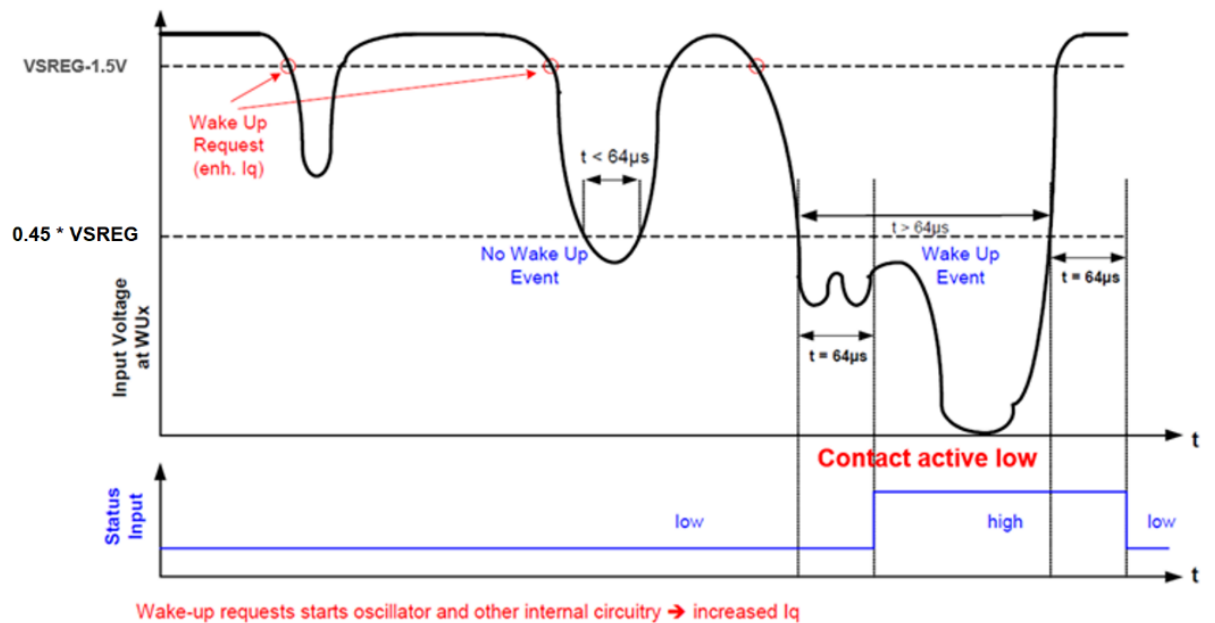
4.3.2 Cyclic wake-up monitoring

Cyclic contact monitoring conceived to reduce the quiescent current of the device, allows periodical activation of the wake-up input to read the status of the external contact. The periodical activation is driven by timer 1 or timer 2 whose settings (on-time and period) can be configured through bits Tx_PER_y and Tx_ON_y in CR2.

Moreover, in case of cyclic sensing, the internal pull-down resistor (R_{WU_act}) is periodically activated on each rising edge of the TIMER_ON.

The input signal is filtered with a filter time of t_{WU_CYC} after a delay (80% of the configured timer on-time) as showed in the Figure 8. A wake-up is processed if the status has changed versus the previous cycle, therefore wake-up by WU status bit (WU_WAKE bit in SR1) is set only if the status of two consecutive ON-time pulses is different.

Figure 8. Cyclic wake-up monitoring
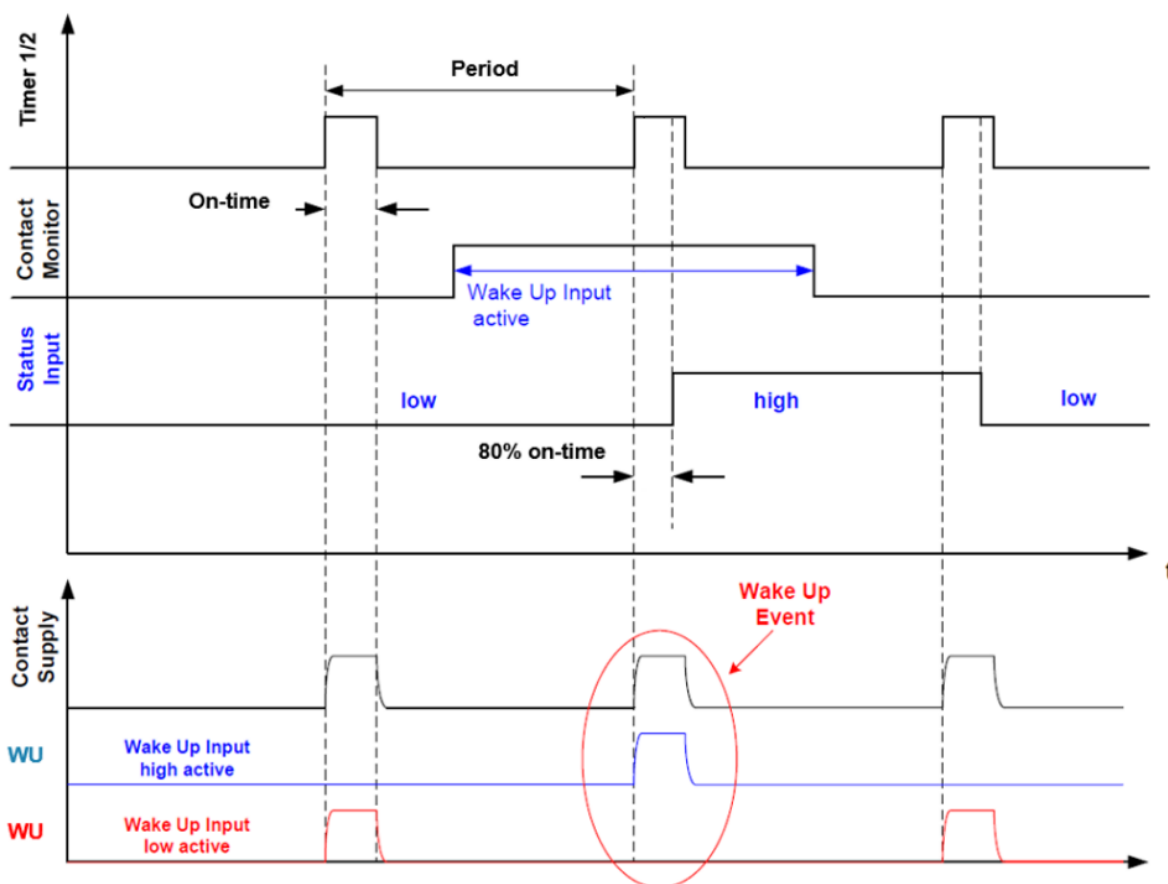
The output OUT15, configured to be driven with timer1 or timer2 (bits OUT15_y in CR6), with the same timer setting (timer1 or timer2) used for cyclic monitoring of the wake-up input, can be used to supply the external contact (see the Figure 9).

Figure 9. External contact supplied periodically by the internal timer through OUT15
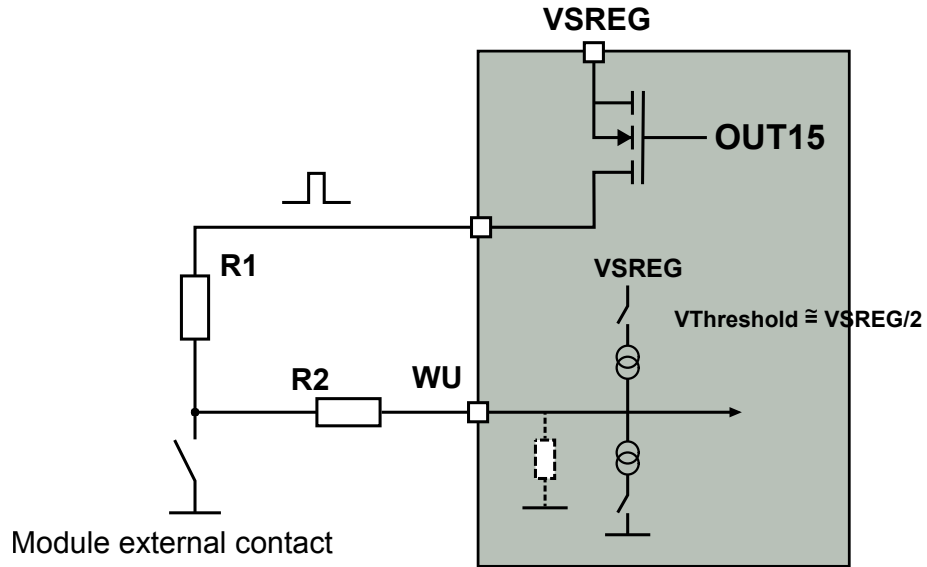
The following is a practical example of external resistor dimensioning in the case of OUT15 (configured in low current mode) being used to supply the external contact (active low).

The external resistors R1 and R2 should be dimensioned according to the following recommendation:

- If contact is closed;

$$\frac{V_{Sreg,max}}{R1} < I_{OC15\_min} \tag{1}$$

This condition must be satisfied to avoid OUT15 over current protection intervention when contact is closed.

- If contact is open;

$$V_{Sreg,max}\frac{R_{WU\_act\_min}}{R1 + R2 + R_{WU\_act\_min}} > V_{Sreg,max} - 1.5 \tag{2}$$

This condition guarantees the minimum current consumption in standby mode when contact is open.

Resolving the Eq. (1) and Eq. (2):

$$R1 > \frac{V_{Sreg,max}}{I_{oc15\_min}} \tag{3}$$

$$R1 + R2 < \frac{3R_{WU\_act\_min}}{2V_{Sreg,max} - 3} \tag{4}$$

Considering the value on datasheet (I_{OC15_min} = 150 mA and $R_{wu\_act\_min}$ = 80 kΩ) and supposing $V_{Sreg,max}$ = 18 V:

$$R1 > 18\,V/0.15\,A \approx 120\,\Omega \tag{5}$$

$$R1 + R2 < \frac{3*80\,k}{2*18 - 3} \approx 7.2\,k\Omega \tag{6}$$

A possible combination that satisfies the two previous requirements could be R1 = R2 = 1 kΩ (see the Figure 10).

Figure 10. Example of R1 and R2 dimensioning
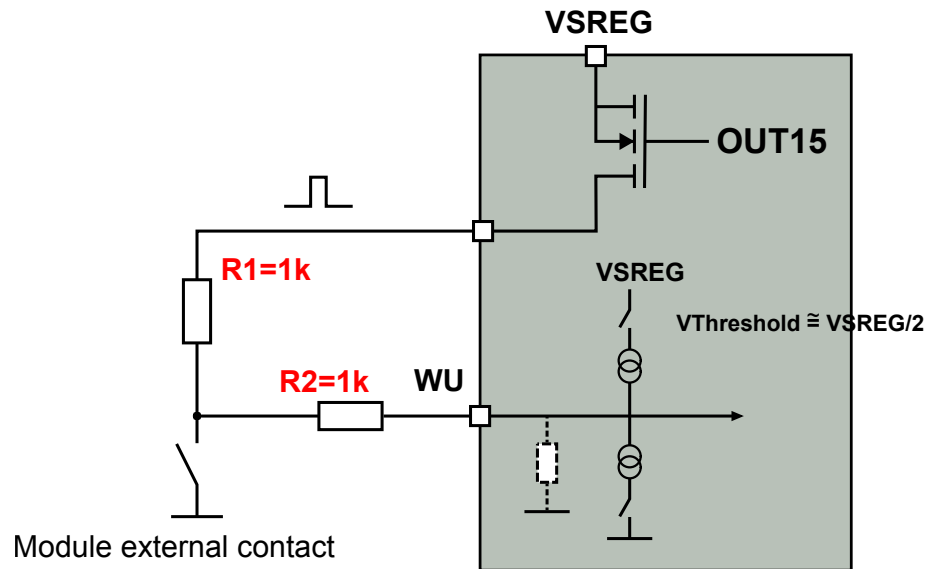
5 Watchdog

5.1 Startup or wake-up from VBAT/V1 standby

After power-ON or after wake-up from V1/VBAT standby mode, the watchdog starts with a timeout (long open window, $t_{LW,min}$ = 160 ms). This timeout allows the microcontroller to run its own setup before starting the window watchdog by setting the trigger bit (TRIG in CR1 or CFR).

The Long open window starts also in the following cases:

- After entering V1_Standby mode (if I_{V1} > Icmp and WD enable)
- Exit from debug mode

5.2 Watchdog normal operation

After the long open window (t_{LW}) MCU must serve the watchdog by alternating the watchdog trigger bit (TRIG in CR1 or CFR) within a time inside the safe trigger area defined by T_{SWx_max} - T_{SWx_min} (configurable, default 7.5 ÷ 12 ms), as showed in the Figure 11.

Figure 11. Watchdog safe trigger area
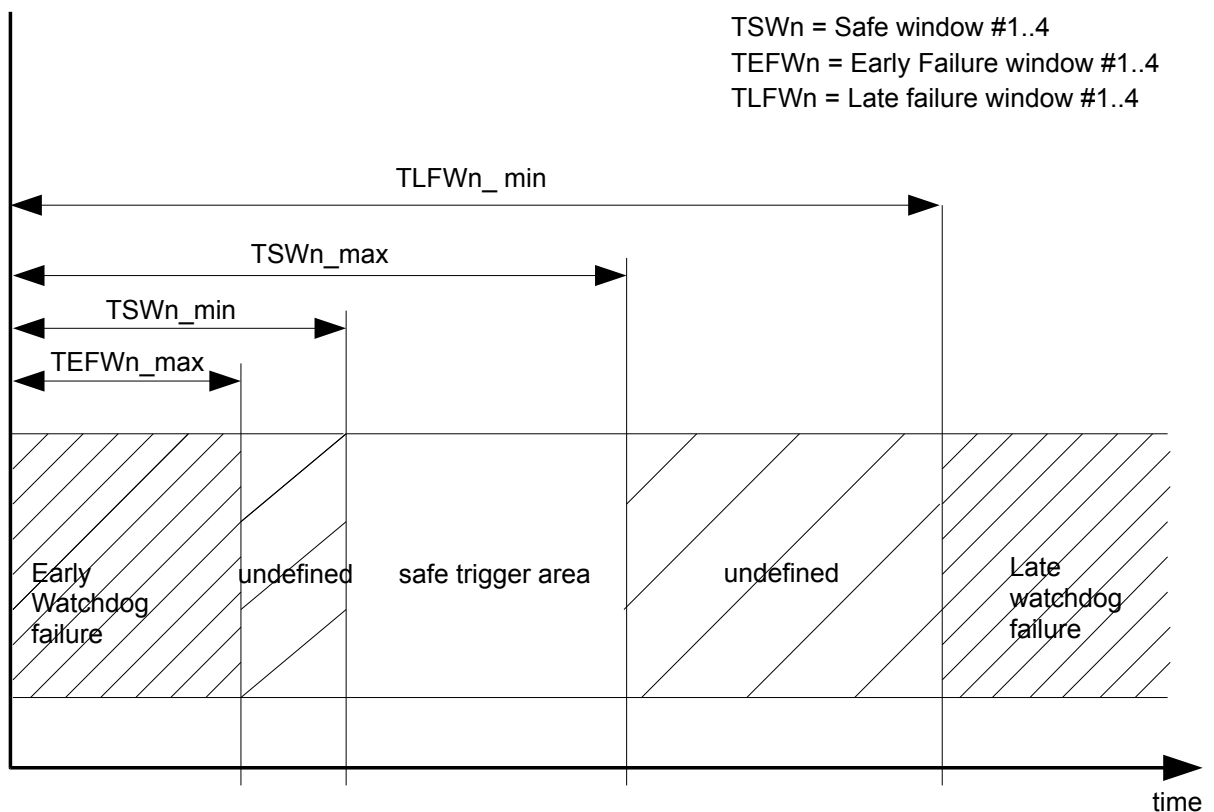
The recommended way to serve the watchdog is the following one:

- Read the status of TRIG bit in CR1 (or CFR if CFR is used as the watchdog trigger register);

Note: *The WD trigger bit in CR1 and CFR are internally synchronized.*

- Serve the watchdog with the inverted trigger bit read back from the previous step;
- Repeat the previous steps in a time inside the safe trigger area (T_{SWX_min} < t < T_{SWX_max}).

In case the trigger bit is not updated inside the safe trigger area (shorter or longer time) a NRESET pulse is generated and the watchdog restarts with a long open window (t_{LW}). Details on the Figure 12.

### Figure 12. Watchdog timing
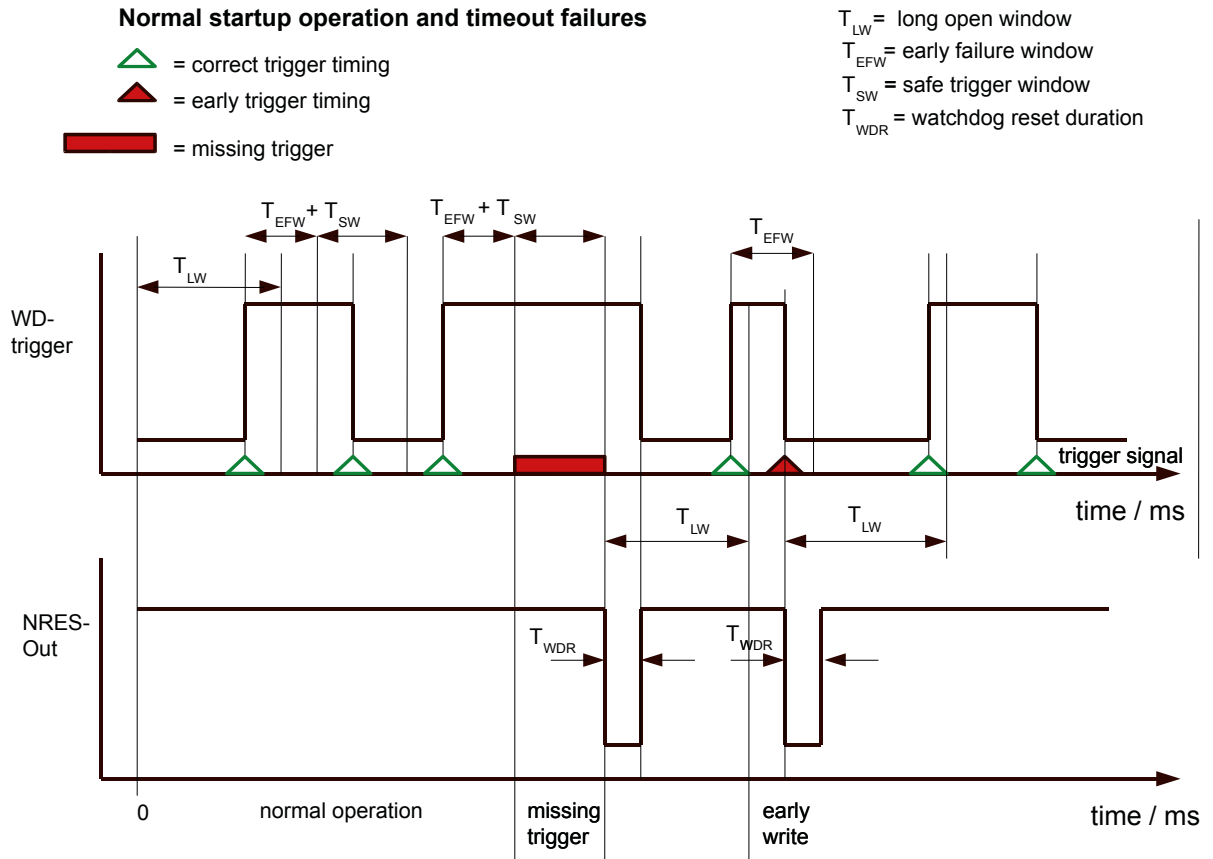
Window watchdog trigger time can be configured with 4 values: T_{SW1} (7.5 ÷ 12 ms, default after power ON), T_{SW2} (37.5 ÷ 60 ms), T_{SW3} (75 ÷ 120 ms) and T_{SW4} (150÷240 ms).

The SPI command needed to change watchdog timing is protected; two consecutive SPI write commands are requested as described below:

1. Set to 1 the bit WD_CONFIG_EN in CFR, first;
2. Set WD_TIME_x bits in CR2 to the desired value.

As showed in the Figure 13, the new timing (T_{SW2}) gets active immediately, and the next TRIG refresh cycle must be sent within the new timing (T_{SW2}).

Figure 13. WDC time change from 10 ms to 50 ms
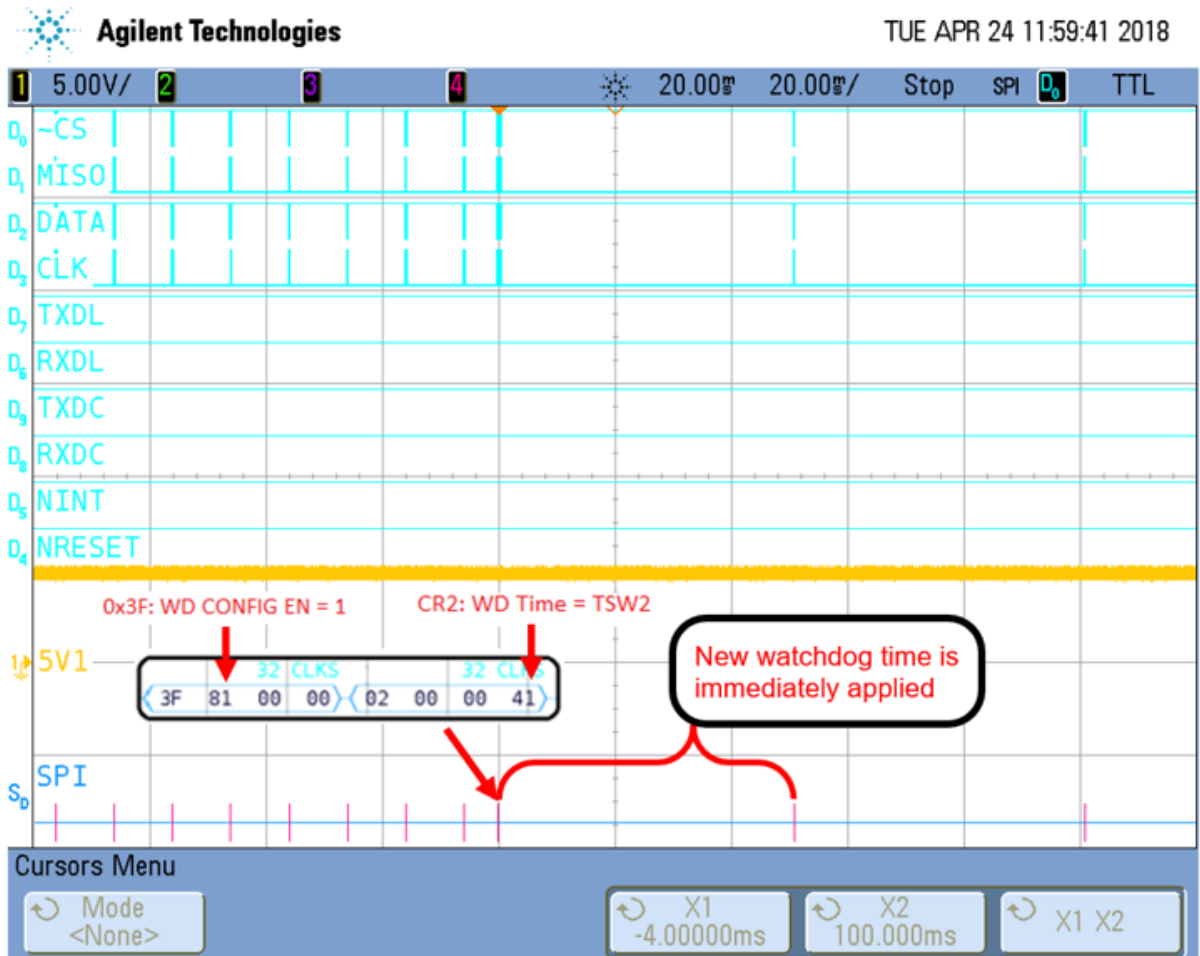
Following there are two examples on how to feed the watchdog at device startup:

Example 1: default configuration with T_{SW1}

- At device startup the NRESET is released, and the watchdog starts a long open window (t_{LW}).
- Before t_{LW} expiration the MCU must write the TRIG bit to 1, then the watchdog leaves a long open window and the MCU must feed the watchdog within the safe window time.
- After about 10 ms (value inside the safe window 1) there should be another write operation on CFR, and the TRIG bit must be written to 0. And so on.

Example 2: T_{SW2} set at device startup

There is the possibility to set timing T_{SW2} at device startup:

- At device startup, before t_{LW} expiration, the two commands to change watchdog timing are sent, as previously described. The new timing (T_{SW2}) is set.
- Then the MCU writes the TRIG bit to 1 (before t_{LW} expiration).
- After about 50 ms (value inside the safe window 2), the TRIG bit must be written to 0. And so on.

5.3 WD in standby mode/Debug mode

In VBAT standby mode and in debug mode, the watchdog is disabled.

5.4 WD in V1 standby mode

In V1 standby mode, depending on ICMP bit (CR22) value, there are two possible scenarios:

• Watchdog is disabled as soon as I_{V1} < Icmp. (ICMP = 0, I_{V1} current supervisor enabled).

• Watchdog is disabled upon transition into V1_standby mode. (ICMP = 1, I_{V1} current supervisor disabled).

5.5 WD failure

In case of watchdog fail, the reset output (NReset pin) will be pulled down for 4 ms (t_{WDR}), and L99DZ200G enter fail-safe mode. The watchdog fail bit (WDFAIL in SR1) is latched and, after NRESET is released, L99DZ200G starts a long open window to allow the MCU do the startup procedure,

As showed in the Figure 14, if after the first WD failure there are 7 additional watchdog failures in sequence, the regulator 5V1 is turned-off for t_{V1OFF} (typ. 200 ms). Then, after 7 additional consecutive watchdog failures, the 5V1 regulator is turned off permanently, the device goes into forced VBAT_standby mode, and the status bit FORCED_SLEEP_WD in SR1 is set.

Figure 14. Consecutive watchdog failures
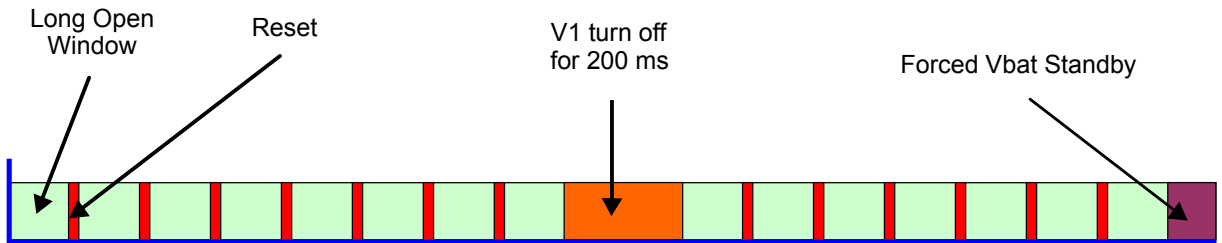
From forced VBAT_standby mode a wake-up is possible by any activated wake-up source.

After waking up, if the watchdog trigger is still not serviced in a watchdog long open window, the device enters forced VBAT standby mode again at the first WD failure, since the internal failure counter has been NOT cleared, keeping the maximum number of 15 failures. This sequence is repeated until a valid watchdog trigger event is performed by writing bit TRIG = 1.

6 Fail-safe

The fail-safe (FS) circuitry is a completely independent mechanism that allows the device to react to critical conditions by immediately switching OFF all outputs.

Specifically, in fail-safe mode, the device behaves as follows:

- All outputs besides LSA_FSO and LSB_FSO are turned off
- All control registers are set to default values except the GENERATOR_MODE_EN bit
- LIN and SPI remain ON (transmitters are deactivated in case of thermal shutdown TSD1 (TSD1 cluster 5 or 6 in cluster mode)
- FS bit (global status byte) and corresponding failure bits in status registers are set
- LSA_FSO and LSB_FSO will be turned on
- The charge pump is switched off
- Write operations to control registers are blocked. Only the following bits are not WRITE protected:
  - CR13~CR16:
    - PWMx_DC_y
  - CR12:
    - PWMx_freq_y
  - CR6:
    - OUT15_x
  - CR2:
    - Timer1 and Timer2 settings
  - CR1:
    - V2_x
    - CAN_GO_TRX_RDY
    - TRIG

There could be different sources of failure:

- Watchdog failure due to a microcontroller failure
- 5V1 regulator failure due to an overload or a short to GND
- Thermal shutdown (TSD2)

Failures can be categorized in two types:

- Temporary failures: failure that can automatically recover after a while.
- Non-recoverable failures: failure that remains stable till external failure removal action

In case of temporary failures the device enters immediately in FS mode and then it can recover with the actions reported in the Table 4.

Depending on the different root cause of entering the fail-safe, the action to exit fail safe mode is different as shown in the Table 4.

In case of non-recoverable failures, L99DZ200G, after different retry tentative, enters in forced VBAT standby mode and all control registers are set to default value. After the device wake up, as soon as the fault has been removed, the cause of the forced VBAT standby mode is indicated in the SPI status registers. In the Table 5 all possible non recoverable failures with relevant diagnosis flags are reported.

Table 4. Temporary failures conditions

Fail source	Failure condition	Diagnosis	Exit from fail-safe mode
Microcontroller (oscillator)	Watchdog early writes failure or expired window	FS (global status byte) = 1 WDFAIL (SR1) = 1 WDFAIL_CNT_x (SR1) = n + 1	TRIG (CR1) = 1 during long open window Read and clear SR1
V1	Undervoltage	FS (global status byte) = 1 V1UV (SR1) = 1 V1fail (SR2) = 1[1]	$V1 > V_{RTrisinng}$ Read and clear SR1
Temperature	$T_j > T_{SD2}$	FS (global status byte) = 1 TW (SR2) = 1 TSD1 (SR1) = 1 TSD2 (SR1) = 1	$T_j < T_{SD2}$ Read and clear SR1

1. If V1 < V1fail (for t > t_{Vfail}). The fail-safe bit is located in the global status register.

Table 5. Non recoverable failures conditions

Fail source	Failure condition	Diagnosis	Exit from fail-safe mode
Microcontroller (oscillator)	15 consecutive watchdog failures	FS (global status byte) = 1 WDFAIL (SR1) = 1 FORCED_SLEEP_WD (SR1) = 1	Wake-up TRIG (CR1) = 1 during long open window Read and clear SR1
V1	Short at turn-on	FS (global status byte) = 1 FORCED_SLEEP_TSD2/V1SC (SR1) = 1	Wake-up Read and clear SR1
Temperature	7 times TSD2	FS (global status byte) = 1 TW (SR2) = 1 TSD1 (SR1) = 1 TSD2 (SR1) = 1 FORCED_SLEEP_TSD2/V1SC (SR1) = 1	Wake-up Read and clear SR1
SGND loss	Ground loss at pin SGND	FS (global status byte) = 1 SGND_LOSS (SR1) = 1	Wake-up Read and clear SR1

7   Reset output - NReset

The NReset pin is a device output pin that should be connected to the MCU reset input pin.

At the 5V1 regulator turns ON (V_{SReg} power on or wake-up from VBAT_Standby mode), NReset is kept low for t_{V1R} (2 ms typical) to keep the microcontroller in reset until 5V1 supply voltage is stable. After the NReset is released, the watchdog starts with a long open window (t_{LW}) to allow the microcontroller to run its own setup before starting the window watchdog.

Apart of behavior at device startup, a reset pulse on NReset pin is generated in case of:

- V1 drops below V_{rth} (configurable by SPI) for t > t_{UV1}

Note: *The V1 reset threshold can be configured (using bits V1_RESET_x in CR2) with four values: 4.3 V (default value at power ON), 4 V, 3.8 V and 3.5 V.*

- Watchdog failure

As soon as the NRESET is released, the watchdog timing starts with a long open window.

Figure 15. NRESET pin
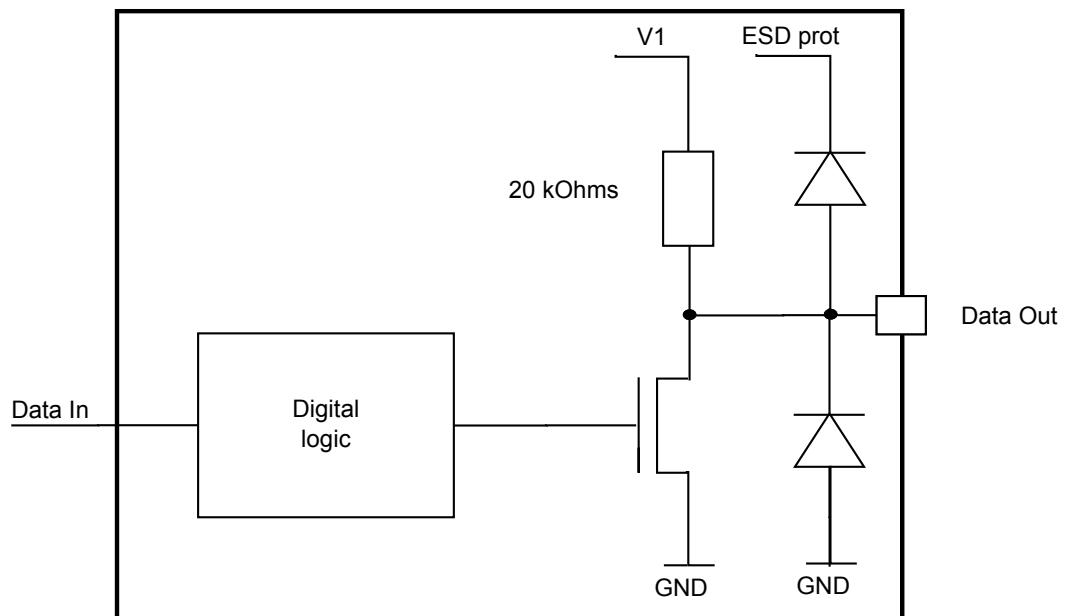
Although there is a 5V1 weak internal pull-up, the external 5V1 pull-up is recommended.

Since the NReset output is realized with an open-drain output, it is also possible to connect other external open-drain structures in parallel to control the MCU reset pin. In other words, the MCU can be reset by a different device, even if this can eventually trigger a watchdog failure error on the L99DZ200G since the MCU is no longer able to serve the watchdog as soon as it has been reset.

8   Interrupt (NINT)

The interrupt pins (RxD_L/NINT RxD_C/NINT and NINT) are device output pins that should be connected to corresponding MCU pins.

RxD_L/NINT, RxD_C/NINT and NINT indicate different events.

RxD_L/NINT indicates:

•   The MCU a wake-up event from V1_Standby mode (except wake-up by CAN).

RxD_C/NINT indicates:

•   Mode transitions of the CAN transceiver

•   CAN communication timeout. The CANTO flag is set (no CAN communication for t > tSilence). This interrupt can be masked by SPI (CR1: CANTO_IRQ_EN).

NINT indicates:

•   In active mode:

    –   VSREG dropped below the programmed early warning threshold (VSREG_EW_TH_x in CR3). The feature is deactivated if VSREG_EW_TH is set to 0 V

•   In V1_Standby mode:

    –   Programmable timer interrupt: a NINT pulse is generated at the beginning of the timer on-time (Timer1 or Timer2)

    –   CAN communication timeout

    –   Wake-up from V1_Standby mode by any wake-up source

In all the previous cases the interrupt pin is pulled low for 56 µs.

The interrupt signal is generated in all wake-up events from V1_Standby, apart the case of Iv1 > Icmp during V1_Standby mode (Iv1 > Icmp). In this specific case the device remains in standby mode while the watchdog starts with a long open window and no interrupt signal is generated.

9 Outputs

9.1 High side output

All high side outputs can be configured to be driven by:

- Internal DC input (ON/OFF activation)
- 7 internally generated PWM signal (PWM1 to PWM7)
- 2 internal timer (Timer1 or Timer2)
- 1 external pin (DIR) which can be connected to an MCU output pin

The configuration can be chosen using the 4-bits OUTx_y (x: channel number; y: 0~3) in CR5 and CR6, as showed in the Table 6.

Furthermore, the RDSON for OUT7 and OUT8 is configurable (bits OUT7_RDSON and OUT8_RDSON in CR9).

Table 6. Power output settings

OUTx_3	OUTx_2	OUTx_1	OUTx_0	Description
0	0	0	0	Off (default)
0	0	0	1	On
0	0	1	0	Timer1
0	0	1	1	Timer2
0	1	0	0	PWM1
0	1	0	1	PWM2
0	1	1	0	PWM3
0	1	1	1	PWM4
1	0	0	0	PWM5
1	0	0	1	PWM6
1	0	1	0	PWM7
1	0	1	1	Not applicable

The available high side outputs are:

- OUT 7 to OUT 10, OUT 13 and OUT 14 (supplied by VS)
- OUT 15 (supplied by VSREG)

All high-side outputs are protected and are switched OFF in case of:

- VS/VSREG overvoltage and undervoltage (depending on SPI configuration, see datasheet "Power supply fail" section for details)
- Overcurrent in case $I_{OUT} > I_{OCX}$ (with OCR mode only for OUTs having this feature)
- Over temperature in case $T_j >$ TSD1 (behavior depends on TSD_CLUSTER_EN bit value)
- Fail-safe event
- Loss of GND at SGND pin

9.2 Half-bridge output

All high side and low side of half bridge outputs can be configured ON or OFF.

Furthermore, the RDSON for both OUT 1 and OUT 6 is configurable (bit OUT1_6_RDSON in CR9).

9.3 Overcurrent recovery and CCM mode

L99DZ200G integrates the CCM (constant current mode) mode for OUT 7, 8 and 9, and the OCR (overcurrent recovery) mode for all half-bridge and some high side outputs (OUT 7, 8 and 15), to fit respectively motors or incandescent bulbs (inrush current) and LED modules with high capacitor at input.

9.4 Constant current mode

CCM mode is available for OUT 7 ~ OUT 9. This function can be set only if the related driver is in OFF state, and it temporarily disables channel overcurrent and short-circuit detection (open-load detection remains enabled).

The CCM mode is not available with internal PWM and timer. If the CCM bit is set, an SPI write command to configure OUT to be driven by PWM or timer is rejected, and the SPI invalid command error flag is set.

The default value for CCM bit is OFF.

For correct channel enable in CCM mode, the following sequence has to be used:

•   Set OUTx_CCM_EN bit (x = 7, 8, 9) in CR9

•   Set OUTx_0 bit to turn ON the driver in DC mode (PWM or timer are ignored)

The driver starts with a constant current of typical 175 mA (ICCM) for 10 ms (t$_{CCMtimeout}$); during this phase channel overcurrent and short-circuit detection are disabled. When t$_{CCMtimeout}$ has elapsed, the channel switches to ON mode, while the OUTx_CCM_EN bit is automatically cleared.

The Figure 16 and Figure 17 show an example of an RC load (10 µF with 68 Ω in parallel) driven by OUT8 with CCM disabled and with CCM enabled. With CCM disabled the current needed to charge the output capacitor is higher than the OC threshold (IOC8) and the channel is immediately switched OFF. If CCM is enabled the load voltage increases linearly (with a constant current) during t$_{CCMtimeout}$ and charges the capacitor, then the device is switched fully ON.

Figure 16. OUT 8 with an RC as load, with CCM disabled
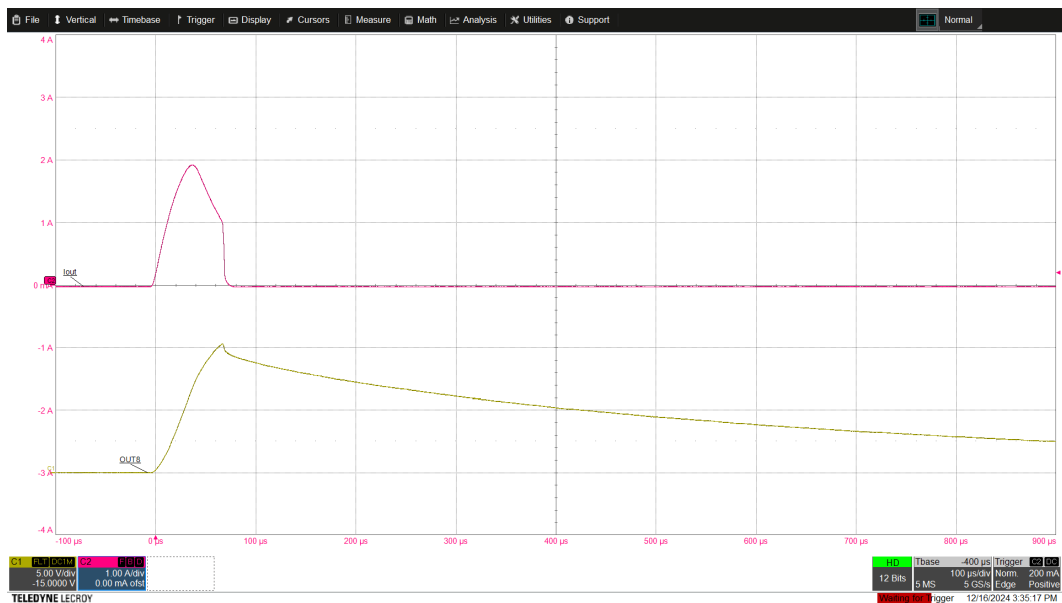
Figure 17. **OUT 8 with an RC as load, with CCM enabled**
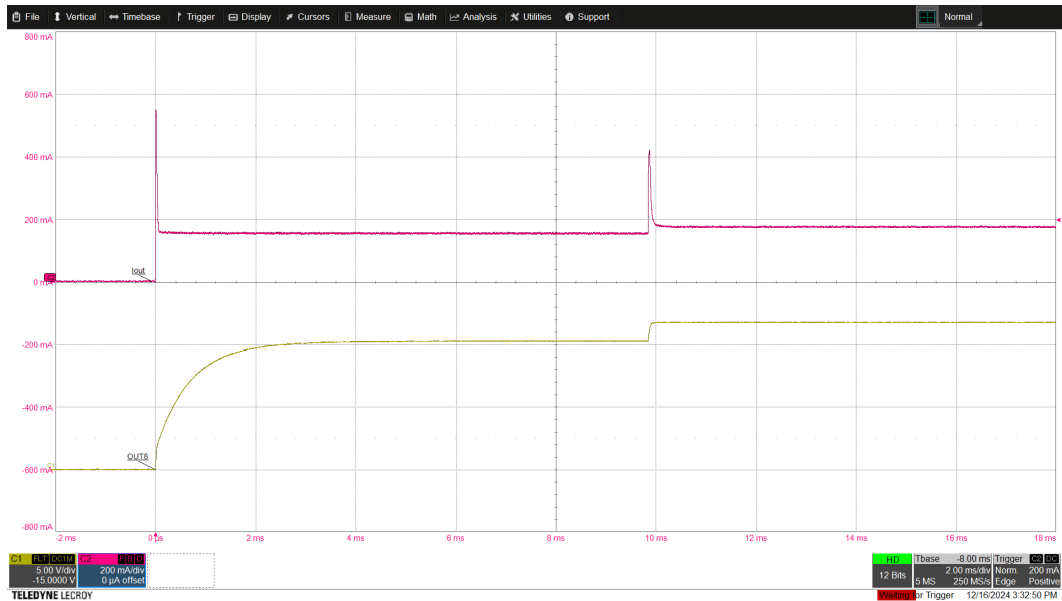
9.5 Overcurrent recovery mode

OCR function is available for all HB and some high side outputs.

The overcurrent recovery feature can be enabled by setting the OUTx_OCR bit in CR7.

If OCR mode is enabled, the corresponding output is turned OFF when the overcurrent threshold is reached, and then it turns automatically ON after a programmable recovery time. The PWM modulated current provides sufficient average current to power up the load (for example: heat up an incandescent bulb or a motor inrush current) until the load current reaches a stable condition (is not suggested to enable the OCR function for too long time. Based on the load information, the OCR function should last for a limited time.).

In the Figure 18 it is shown an example of OCR mode in case of inductive load (like a motor) and in case of incandescent bulb load.

Figure 18. **OCR function with inductive loads and incandescent bulbs**
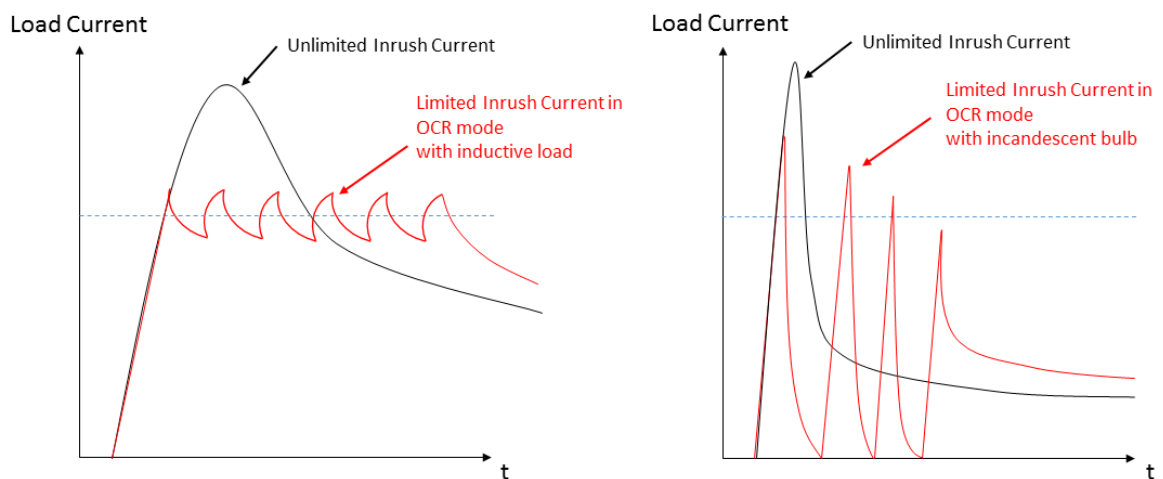
9.6 Short circuit protection

Only integrated half-bridge drivers have another protection against hard short circuits. This feature is enabled by default, and it can be disabled through bit OUTx_SHORT_DIS in CR7.

In case of hard short circuits (short circuit faster than t_{OCR} or occurring during t_{BLK}), another threshold higher than over current threshold (I_{OCX}) is implemented. In case the output current is higher than the short circuit threshold (I_{SC_OUTX}) for more than the filter time (t_{FSC}), the channel is switched OFF (see red trace in the Figure 19), the status bit OUTx_xS_SHORT in SR4 is set and the channel can be reactivated only after the related flag is cleared.

Figure 19. Short circuit detection (red trace)
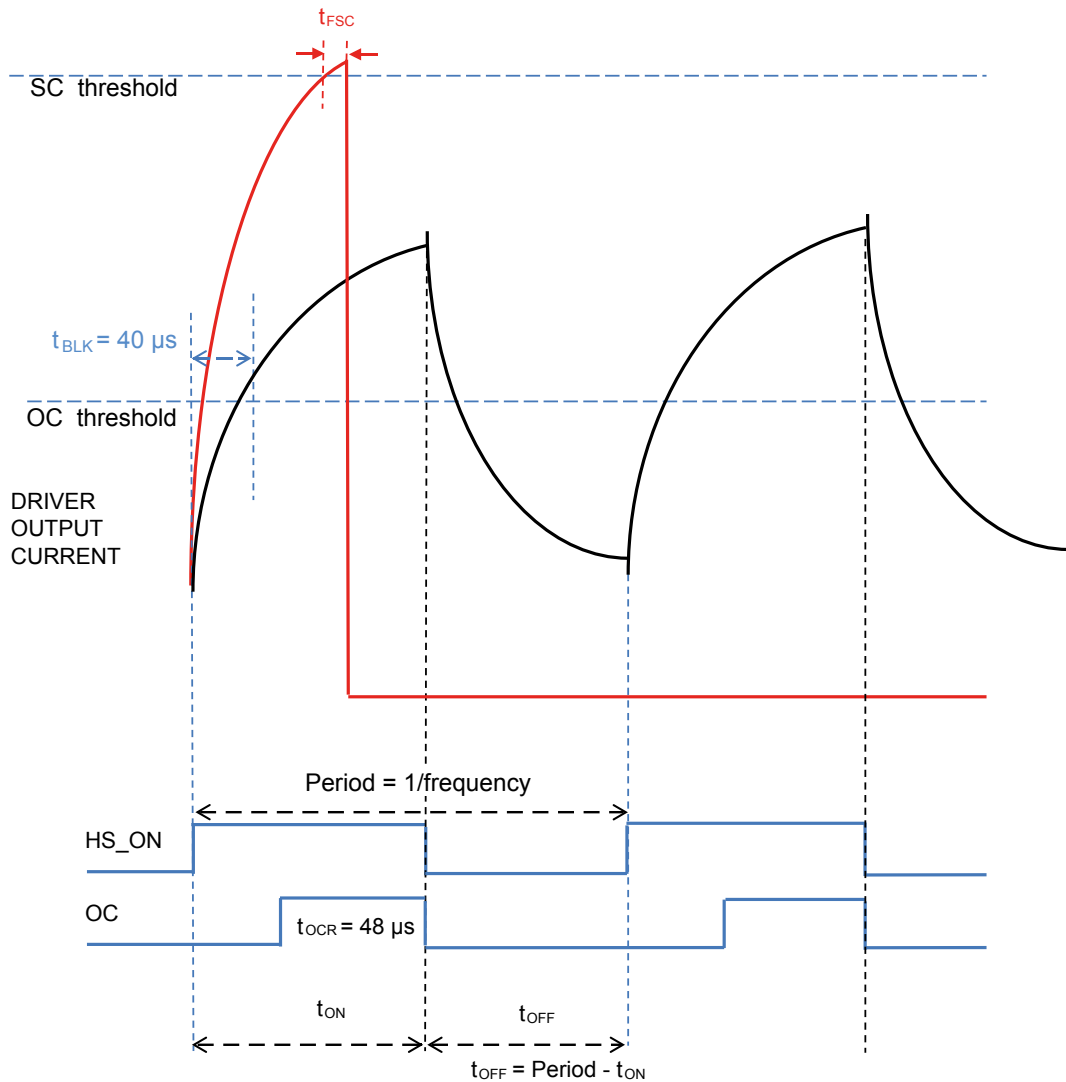
Red peak Current: device shutoff as per SC threshold
Black peak Current: device cycling as per auto-recovery setting

9.7 Thermal expiration feature

The OUT1, 2, 3, 6, 7, 8, and 15, have thermal expiration feature that provides a robust protection against possible microcontroller malfunction, switching off a given channel if continuously driven in auto-recovery (OUTx_OCR_THX_EN (CR8). If the temperature of the related cluster increases by more than 30 °C after reaching the auto-recovery time t_{AR}, the channel is switched off. The thermal expiration status bit OUTx_TH_EX (SR3) is set.

Figure 20. Short circuit detection (red trace)
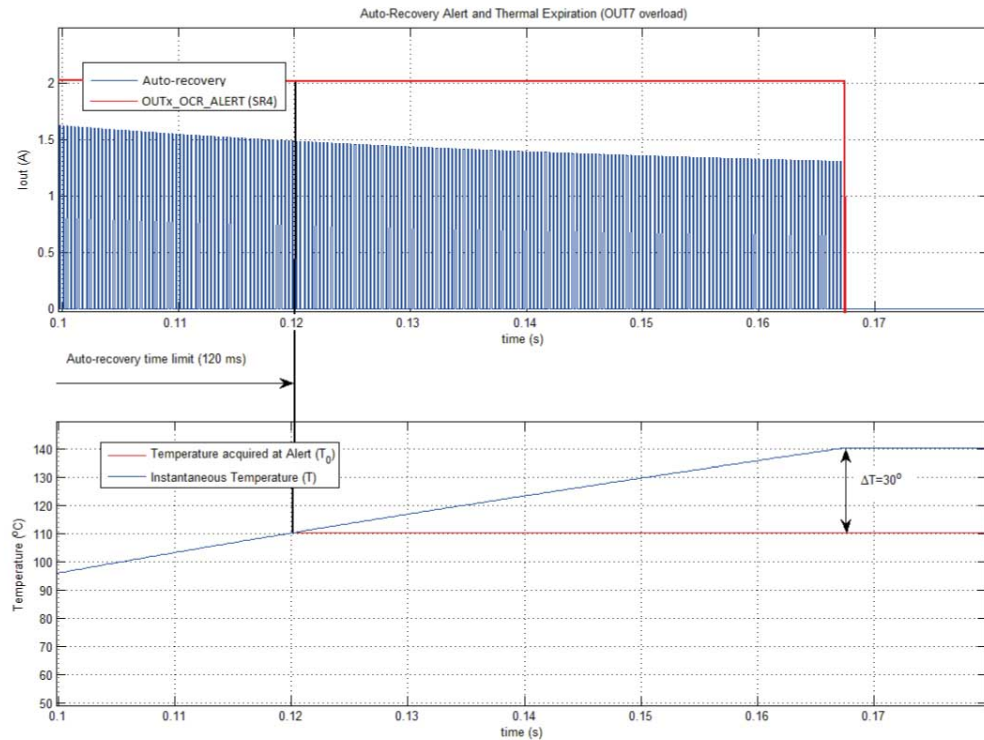
Note: *Temperature acquisition starts after t_{AR} thermal expiration occurs after a ΔT = 30º.*

9.8 Duty cycle adjustment

All standalone high side outputs can be programmed to calculate some internal duty cycle adjustment to adapt the duty cycle to a changing supply voltage at VS. This feature is aimed to avoid LED brightness flickering in case of alternating supply voltage. Auto compensation features can be activated for all HS outputs each by setting OUTx_AUTOCOMP_EN (CR 17 to CR 20).

The formula below explains how the control is realized.

$$DutyCycle = \frac{V_{th} - Vled}{V_{bat} - Vled} \times DutyCycleNom \tag{7}$$

Where:

- Vth → Duty cycle reference voltage (fixed at 10 V)
- Vbat → Voltage at VS pin
- Vled → Voltage drop on the external LED (To be compatible to different LED load characteristics the value for VLED can be programmed for each output by a dedicated control register, the voltage must be < Vth (10 V)
- Duty Cycle Nom → Nominal duty cycle programmed by SPI< PWMx DCx>

10 Heater power MOSFET driver

L99DZ200G embeds a gate driver stage for N-channel power MOSFET in high-side configuration to control an external heater as shown in the Figure 21. The heater driver is controlled by the control bit GH in the CR5.

Figure 21. MOSFET driver for external heater
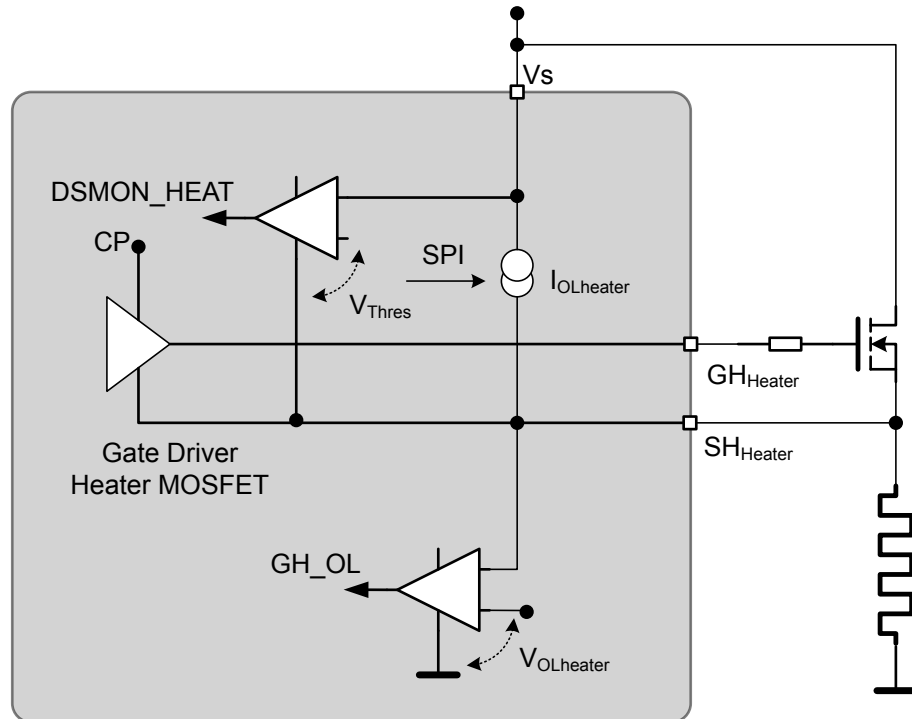
The driver also contains internal circuitry for OL detection in OFF state and V_{DS} monitoring in ON state.
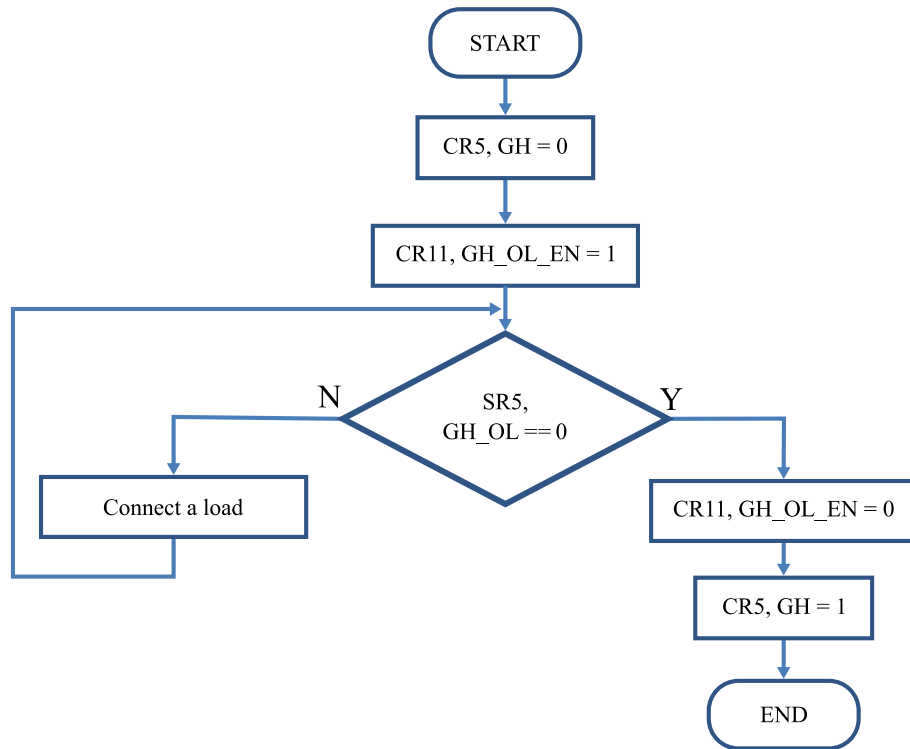
The V_{DS} monitoring function protects the external MOSFET in case of short-circuit to GND only when the driver is active (GH = 1). If the DS voltage exceeds the programmed threshold voltage V_{SCdx_HE} (configurable in the range 200 mV~550 mV through the 3-bits GH_TH_x in CR11) for a time higher than filter time t_{SCd_HE} (6 μs typ), the gate driver switches off the external MOSFET and the corresponding drain source monitoring flag (DSMON_HEAT bit in SR5) is set. The DSMON_HEAT bit must be cleared by SPI to reactivate the gate driver.

Open-load detection in off state is realized by monitoring the voltage difference between SH heater and GND and supplying SHheater by a pull-up current source that can be controlled via SPI with GH_OL_EN bit in CR11. If no load is connected to the external MOSFET source, the voltage is pulled to VS and if the voltage exceeding the threshold $V_{OLheater}$ for a time longer than the open-load filter time (t_{OL_HE}) the open-load bit GH_OL in SR5 will be set.

The recommended heater activation procedure is the following (see the flow chart in the Figure 22):

- Put the gate driver in OFF state (CR5, GH = 0)
- Active the open-load detection in the OFF state, by setting GH_OL_EN bit (CR11, GH_OL_EN = 1):
  - If no load is connected to the external MOSFET source, the MOSFET source voltage is charged to VS and the open-load bit GH_OL (SR5, GH_OL = 1) will be set
  - If the load is connected to the output, no GH_OL flag is set (SR5, GH_OL = 0)
- If the OL diagnosis does not report any issue (SR5, GH_OL = 0), it is necessary to disable the open-load detection stage (CR11, GH_OL_EN = 0) and then the MOSFET can be turn ON (CR5, GH = 1)

Figure 22. Flow chart diagram for heater activation procedure


```
                    START
                      │
                      ▼
              ┌──────────────┐
              │  CR5, GH = 0 │
              └──────────────┘
                      │
                      ▼
          ┌──────────────────────┐
          │ CR11, GH_OL_EN = 1   │
          └──────────────────────┘
                      │
          ┌───────────┴──────────┐
          │          ◇           │
     N    │      SR5,             │    Y
     ◄────┤   GH_OL == 0          ├────►
          │          ◇           │
          ▼                       ▼
  ┌──────────────┐       ┌──────────────────────┐
  │ Connect a load│      │ CR11, GH_OL_EN = 0   │
  └──────────────┘       └──────────────────────┘
                                  │
                                  ▼
                         ┌──────────────┐
                         │  CR5, GH = 1 │
                         └──────────────┘
                                  │
                                  ▼
                                END
```

11 Electrochromic glass control

L99DZ200G can control an electrochromic (EC) mirror glass using the integrated SPI-driven module with an external MOS transistor (see the Figure 23).

The function can be enabled through the bit ECON in CR11. When ECON = 1, OUT10 is automatically turned ON and OUT10 settings (CCM, OCR, PWMx, DIRx, TIMERx) are ignored. OUT10 settings are recovered as soon as ECON bit is set to '0'.

The ECV pin voltage can be set to a target value using the 6-bits EC_x in CR11. The target voltage is binary coded with a full-scale range of 1.5 V (0V with bits '000000' and 1.5 V with bits '111111').

An internal low side switch can be enabled (ECV_LS bit in CR11) for ECV fast discharge. In this case, the ECV pin is pulled to ground by 1.6 Ω low-side switch to reach faster the target voltage. The internal ECV MOSFET is also protected in case of overcurrent (ECV_OC flag) and embeds the OL circuitry (ECV_OL flag).

For loop-stability and EMS reasons, all the relevant external components must be placed as close as possible to device pins. A capacitor of at least 5 nF must be placed between pin ECDR and GND, and a capacitor of at least 200 nF must be placed between pin ECV and GND.

Figure 23. Electro-chrome control block
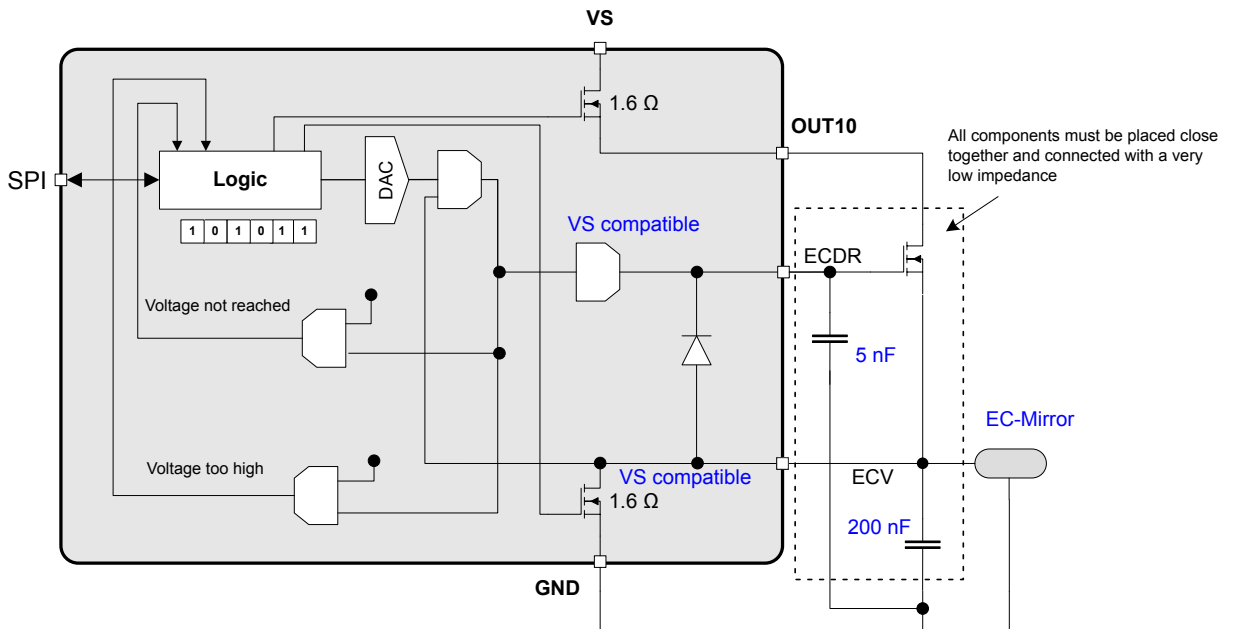
ECV settings:

- In electro-chrome mode, (ECON = 1), the drain of the external power MOSFET transistor (the recommended one is STL19N3LLH6AG) is supplied by OUT10, which maintains its integrated diagnoses in case of overload or open load conditions (OUT10_OC and OUT10_OL)
- If ECV_HV = 0 (default value): the maximum electro chrome controller target value is clamped to 1.2 V
- If ECV_HV = 1: the maximum electro chrome controller target value is set to 1.5 V
- The resolution of EC output is constant: $1.5\ V/(2^6 - 1)$, independently by ECV_HV setting
- Internal ECV MOSFET overcurrent and open load failures can be monitored respectively through ECV_OC and ECV_OL bits in SR5

Through SPI it is possible to check if the desired voltage has been correctly reached through two live status bits:

- ECV_VHI bit in SR6 is set in case of $V_{ECV} - V_{target} > d_{VECVhi}$
- ECV_VNR bit in SR6 is set in case of $V_{ECV} - V_{target} < d_{VECVnr}$

The voltage is at the desired value when these bits are both at '0'.

In case of failure (overcurrent, VS/VSREG overvoltage /undervoltage, TSD1, CP_LOW), EC glass control block is disabled (the only exception is VS undervoltage failure with VS_UV_SD_ENA bit set to '0'):

- OUT 10 is turned OFF

- EC_x bits (CR11) are reset to default value '000000'
- ECDR pin is pulled to GND.
- ECON (CR11) bit remains set to '1'
- ECV_LS (CR11) maintains its configuration

The procedure to restart EC control after a failure, supposing that the cause of failure has been removed, is the following:

- Read and Clear of the related error flag (not necessary in case of VS/VSREG overvoltage/undervoltage if CR3 VS/VSREG_LOCK_EN bit is set to '0', since the error flag is automatically cleared)
- Set the desired value on bits EC_x (CR11)

Consider the following points about the internal ECV low side switch:

- Even if ECV_LS = 1, the low side is turned ON only if the ECV_VHI bit is set, otherwise it is maintained in the OFF state.
- If ECV_OC is set, the low side is turned OFF and it is necessary to clear the ECV_OC bit to re-enable the low side driver.
- To discharge a significant out capacitance load via the internal low side it could be necessary to set ECV_OCR (CR11) = 1. With this configuration, ECV_OC will not be set, and, in case of ECV short to VBATT, device internal temperature could rise. **So, it is strongly recommended to enable the ECV_OCR feature for a limited time**.

12 H-bridge pre-driver

L99DZ200G embeds 2 pre-drivers to control 8 external MOS transistors in H-bridge configuration that can be driven in PWM mode up to 50 kHz. This is particularly suitable for door power window lift motor.

The H-bridge drivers are disabled by default. They are enabled setting the bit HEN_x in CR1.

The MOSFET activation can be controlled by input pins (PWMHNy), and DIRHy bits according to SPI setting.

There are two modes available, selectable by the DMy bit in CFR:

• Single mode (bit DMy = 0, default): 4 MOSFET in full bridge configuration to drive a single motor
• Dual mode (bit DMy = 1): two independent half bridges can be used for two separated motors

Additionally, with the 2-bits SDxy and SDSxy (CR10 register) four different slow decay modes (via drivers and via diode) can be selected using the high-side or the low-side transistors.

All possible input combinations of the previous signal are listed in Table 68 and in Table 69 (H-bridge control truth table in Single and Dual Mode) of datasheet.

H-bridge driver block integrates several customization and protection features:

• Slew rate control: it allows to enable current source driving instead of a low impedance driving
• Resistive output mode: it forces MOSFET OFF during standby mode or in case of failure
• Drain source monitoring: for overload short-circuit detection/protection (for each external MOSFET)
• OFF state diagnosis
• Programmable freewheeling strategy (with SDxy and SDSxy bits)
• Cross current protection with configurable dead time
• Two LS switches (LSA_FSO and LSB_FSO) to switch OFF the MOSFETs if a fatal error happens
• Generator mode: it allows a brake to GND of both the DC motors connected to the 2 external full bridges when an overvoltage on the VS line is detected. It is performed by the switch ON of the external LS MOSFETs of both h-bridges (A and B)

Each of these features is described in the datasheet (see sections 4.26 to 4.33).

13   LDO diagnosis

L99DZ200G embeds two 5 V LDO voltage regulators:

- 5V1 for MCU and the integrated CAN transceiver supply, with up to 250 mA load current
- 5V2 (configurable in tracker mode) for additional loads, with up to 50 mA load current

For both LDO, to guarantee the output voltage stability, a ceramic load capacitor higher than 220 nF is needed. It is recommended to use a 2.2 µF capacitor.

Both LDOs are protected against overload (like short circuit to GND) and overtemperature. They are protected both at startup and when they are already switched ON.

Short to GND protection at LDO turn ON:

- If V1 < V_{1fail} for t > $t_{V1short}$, 5V1 is switched OFF and the device enters immediately in forced VBAT standby mode (bit FORCED_SLEEP_TSD2/V1SC in SR1 and bit V1FAIL in SR2 are set). The 5V1 LDO is automatically re-enabled after the device is woken up
- If V2 < V_{2fail} for t > $t_{V2short}$, 5V2 is switched OFF (bit V2SC and bit V2FAIL in SR2 are set). To re-enable the 5V2 LDO the V2SC bit must be cleared

Overload protection with LDO already turned ON:

- If V1 < V_{1fail} for t > t_{V1fail}, the status bit V1FAIL in SR2 is set but 5V1 is not switched OFF; its current is limited (I_{CCmax1}), and, if the chip temperature exceeds TSD2, it is switched OFF for about 1 s (t_{TSD}). Then it is automatically reactivated. If the restart fails 7 times within one minute the L99DZ200G enters the forced VBAT-standby mode, and the status bit FORCED_SLEEP_TSD2/V1SC in SR1 is set. The 5V1 LDO is automatically re-enabled after the device wake up
- If V2 < V_{2fail} for t > t_{V2fail}, the status bit V2FAIL in SR2 is set; its current is limited (I_{CCmax2}), and, if the chip temperature exceeds TSD1 (bit TSD1 in SR1 is set), it is switched OFF. To re-enable the 5V2 LDO the TSD1 bit must be cleared

In case of overvoltage on LDO output, no diagnosis is implemented, and depending on LDO:

- 5V1 cannot withstand a voltage higher than 6.5 V
- 5V2 is protected up to 28 V (only in case VSREG is supplied)

14 Thermal clusters

The device temperature is controlled; the power outputs and LDOs are grouped into six clusters (5 clusters related to a specific device part as shown in the Figure 24, and one global cluster), each one with dedicated thermal sensors.

The cluster temperatures can be calculated from the binary coded register value using the following formula:

$$Decimal\ code = \frac{(350 - Temp)}{0.488}$$
(8)

Example: T = 25 °C → Decimal code is 666 (0x29A)

Figure 24. Thermal clusters
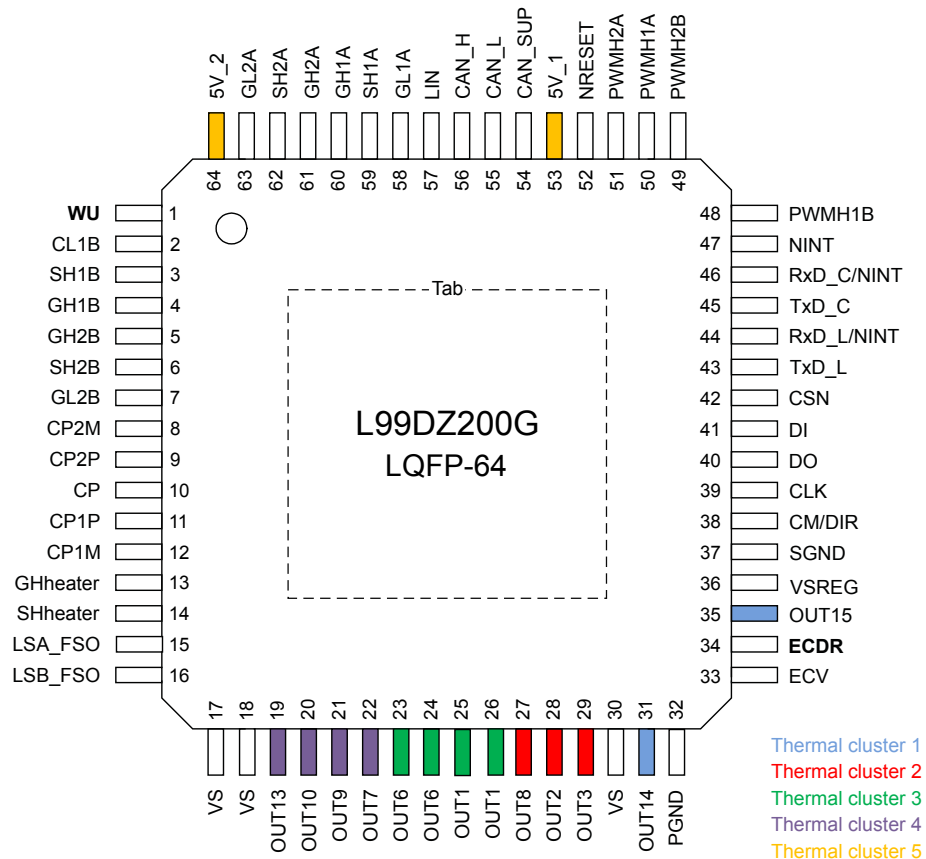
When the temperature of a cluster is higher than TSD1 the device reaction depends on thermal cluster configuration bit value (bit TSD_CONFIG in CFR).

In standard mode (TSD_CONFIG = 0, default), as soon as any cluster reaches TSD1:

- All outputs drivers, charge-pump and 5V2 regulator are turned OFF
- 5V1 remains ON until TSD2
- LIN and CAN transmitter are turned OFF (but they are forced in "receive only" mode)

In cluster mode (TSD_CONFIG = 1), only the cluster which reaches TSD1 is switched OFF. This applies for all clusters except for thermal cluster 6 (global); in this case, the behavior is like standard mode.

For example, with the device configured in cluster mode (TSD_CONFIG = 1):

- If thermal cluster 3 (OUT1, OUT6 related) reaches TSD1:
    - Only OUT1 and OUT6 are turned OFF (all other outputs remain active)
    - 5V1 remains ON until TSD2

15 Unwanted GND loss event

A specific protection at device level is dedicated to the Loss of Ground event that occurs when the SGND pin (internal ground reference for the device logic) is disconnected from PGND pin (GND of all the H-bridges).

An internal comparator senses the voltage difference between the two pins and, if this voltage is high enough to reach the comparator threshold ($V_{SGNDloss}$, typ. 420 mV) for a time interval higher than the filter time ($t_{SGNDloss}$, typ. 7 µs), the device detects a ground loss situation, and L99DZ200G enters the forced VBAT standby mode to prevent damage to the system.

The forced VBAT standby mode can be terminated by any wake-up source, while the cause of the forced VBAT standby mode is indicated in the SPI status registers (SGND_LOSS bit in SR1).

The voltage threshold and filter time values are reported in section 3.4.32 of the L99DZ200G datasheet.

A possible condition that could generate an unwanted GND loss event can be the module power ON (or battery connector hot plug) when the following conditions are met:

• One or more high side output (typically OUT7 and/or OUT8) are connected to a load (for example, bulb) with its return path connected to a local GND (for example, vehicle frame) instead of the module GND (see the Figure 25).

• Vs/Vsreg decoupling capacitors and module capacitors are completely discharged (cold start).

Figure 25. Door module simplified circuitry (unwanted GND loss event)
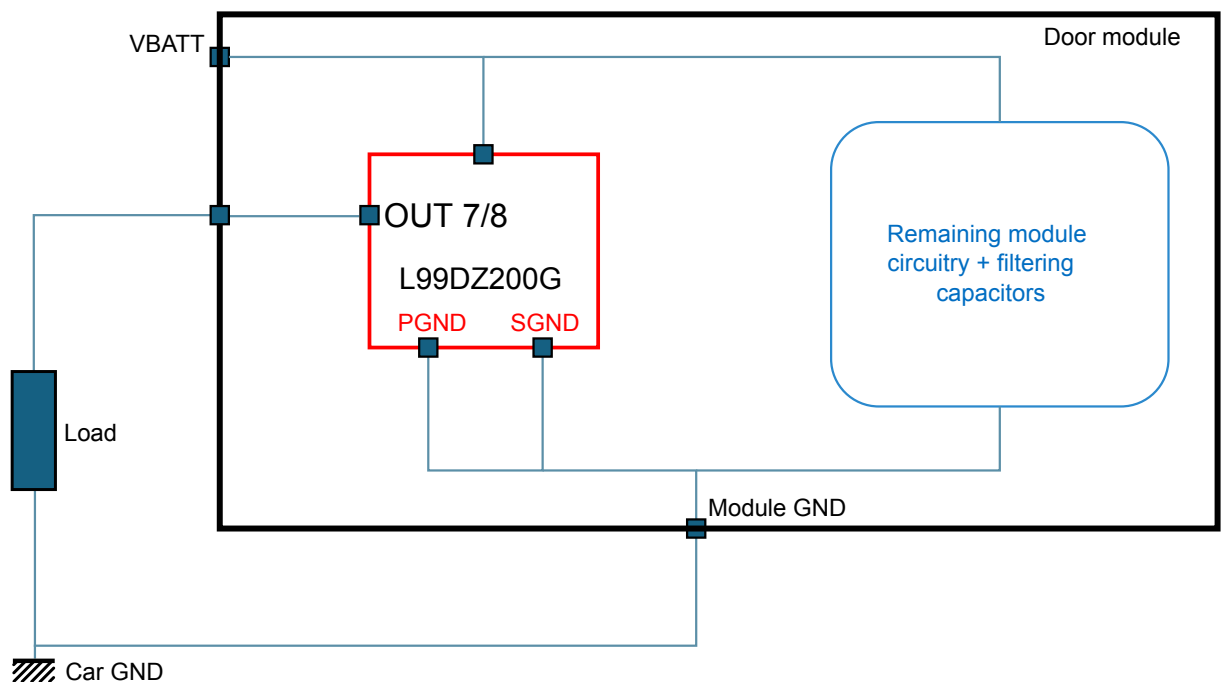
In this situation, it could happen that the device internal GND loss comparator is engaged as graphically described in the Figure 26 (numbers from 1 to 6).

At power ON (1), due to the associated dV_{BAT}/dt, a current spike (2) is generated because of the significant decoupling capacitors on the module (Ispike,batt = Cmodule * dVBAT/dt). This current spike flows through ground module wires and generates a ground module shift (3) versus car ground (Rgnd * Ispike,batt + Lgnd * dIspike,batt/dt).

OUT8/7 voltage (4), referred to car GND, becomes dynamically lower than module ground. Consequently, a current flows inside the L99DZ200G internal path (through metal resistance and OUT7/8 pin ESD protection diode) and generates a delta voltage (5) on the ground comparator inputs. If this delta voltage is high enough to reach the comparator threshold ($V_{SGNDloss}$), the digital block circuitry (6) detects a ground loss situation, and L99DZ200G enters the forced VBAT standby mode to prevent damage to the system.

Figure 26. Unwanted GND loss event (L99DZ200G simplified internal structure)
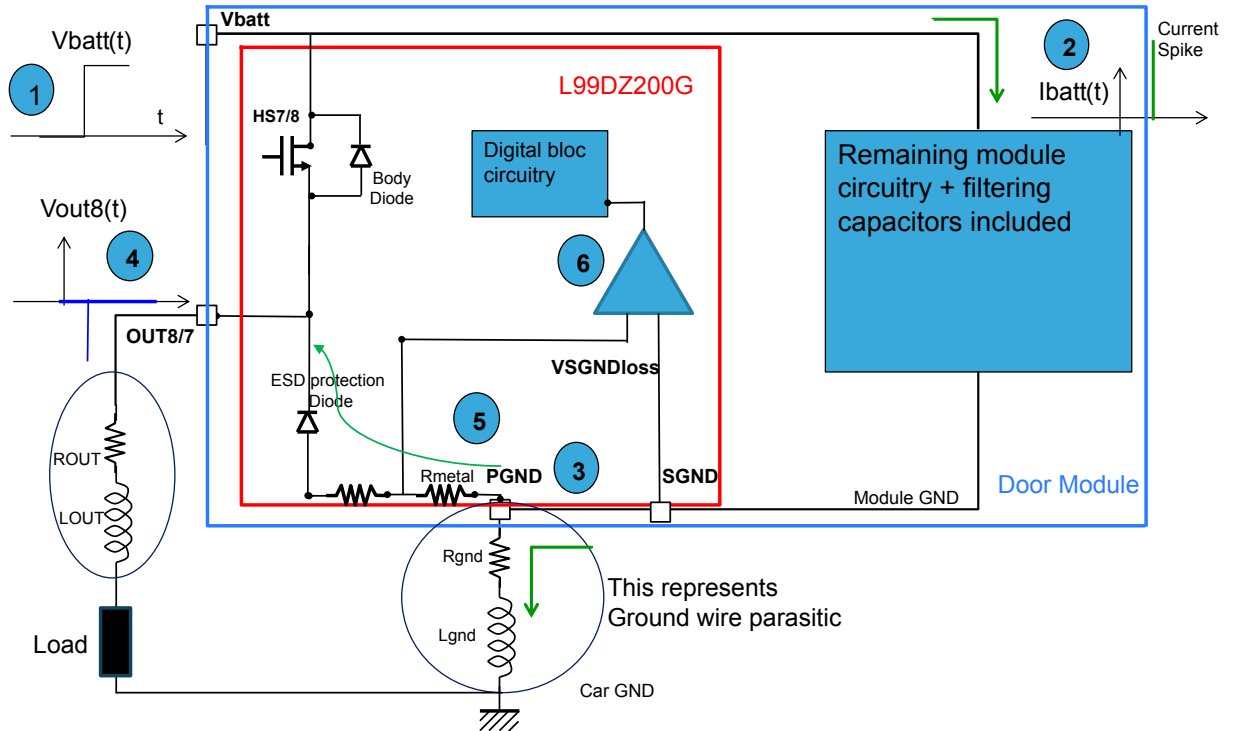
There are two possible solutions to avoid this kind of unwanted GND loss triggering event (see the Figure 27):

1. The load return path must be connected to the module ground instead of the car ground.

2. In case the return path cannot be connected to the module ground, it is possible to add an external clamp between the involved pins (OUT7/8 and SGND) such as a Schottky diode. This external diode is in parallel to the internal structure (ESD diode + Rmetal) and will prevent any significant current flow across the internal path that could lead to Ground Loss comparator triggering.

Figure 27. Solutions: load connected to module GND (left) and diode between OUT7/8 and SGND (right)
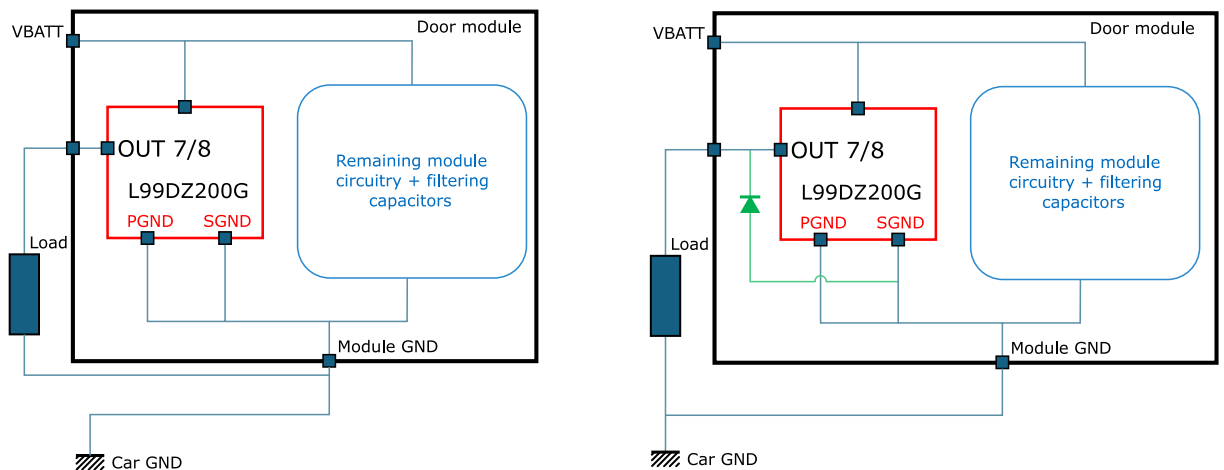
16 Hardware design points

It is recommended to adopt the following rules for external component dimensioning (see numbers in the Figure 28):

1. Capacitance value on Vs pin has to be dimensioned according to load (motors) current (rule of thumb is 500 µF each 10 A)

2. The capacitance value on Vsreg pin has to be dimensioned according to LDO voltage drop out requirements and a diode for reverse Vsreg reverse battery protection must be added between Vbat and Vsreg

3. External components must be dimensioned according to LIN and CAN OEM requirements

4. For both LDO a capacitor of at least 220 nF is required for output voltage stability. For EMC optimization purposes, capacitance could be re-dimensioned (2.2 µF recommended)

5. To guarantee EC drive loop stability all components must be placed as close as possible to the relevant pins. To improve loop stability a resistor on MOSFET gate could be added (range 120 Ω to 220 Ω). It is also recommended to enlarge as much as possible the MOSFET heat dissipation area

6. It is recommended to insert series resistors (1 kΩ) on all signal lines between L99DZ200G and MCU to protect the MCU in case of device failure. If device functionality (that is, CAN at very high frequency) is impacted by such a value, the resistor value can be reduced to zero

7. All output pins must be protected from ESD with a capacitor placed close to the module connector (not close to device pin). The suggested values (22 nF of 47 nF) comply with "Contact discharge, 150 pF, 330 Ω, ±8 kV" specification

Important: *If OUT10 is not used as an EC driver a 22 nF ESD capacitor must be used like other OUT channels.*

Figure 28. **Hardware design points**
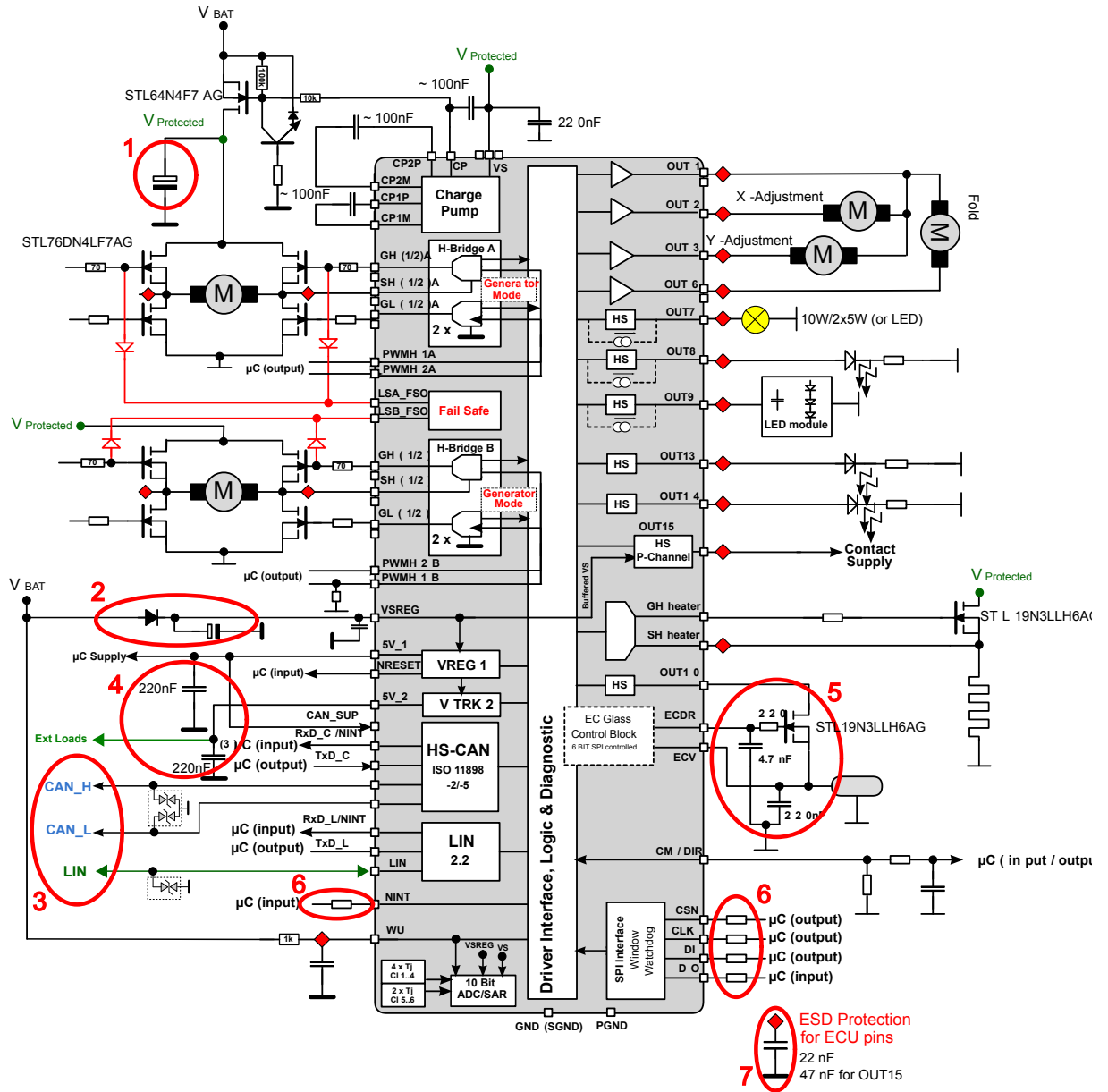
17 Unused PIN

If some device features are not used in the application, the unused pins must be treated as follows:

- CAN interface (all CAN control registers must be disabled by SPI configuration):
    - CAN_SUP supply pin must be connected to 5V1
    - CAN_H and CAN_L must be left floating
    - RxD_C/NINT pin must be left floating (HighZ) to avoid extra consumption
    - TxD_C pin must be connected to 5V1 (35 KΩ internal pull up to 5V1)
- LIN interface:
    - TXD_L pin must be connected to 5V1 (30 KΩ internal pull up to 5V1)
    - RXD_L/NINT pin must be left floating
    - LIN pin must be left floating
- EC block:
    - ECV pin must be left floating
    - ECDR pin must be left floating
- Heater power MOSFET driver:
    - GH_{HEATER} pin must be left floating
    - SH_{HEATER} pin must be left floating
- Power outputs:
    - OUTx pin must be left floating
    - LDO regulator 5V_2 must be left floating
- Digital inputs:
    - PWMH1x and PWMH2x must be connected to GND
    - LSx_FSO must be connected to GND
- WU pin must be connected to GND
- CM/DIR pin must be left floating and must be disabled by SPI configuration (see Table 67 in the datasheet)
- NINT pin must be left floating
- H-bridge interface:
    - GHxy must be left floating
    - SHxy must be left floating
    - GLxy must be left floating

All unused features must be disabled by SPI configuration.

Revision history

Table 7. Document revision history

Date	Version	Changes
10-Jan-2025	1	Initial release.

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IMPORTANT NOTICE – READ CAREFULLY