AN829
APPLICATION NOTE

SEMICONDUCTOR KIT FOR POWER FACTOR CORRECTOR

by J.M. Borgeous

This paper present a new line of P.F.C. dedicated products. Both silicon and packaging have been optimized to reduce system cost, including filtering. The products shown here are offered as a kit for power factor correction.

BOOST CIRCUIT OPTIMIZATION PARAMETERS

Among the available topologies, a boost circuit operating in continuous current mode is the only topology which enables the RFI noise across the input capacitor to be limited, and consequently a lower cost filter is required. Also, the boost inductor stores only a part of the transferred energy, because the mains still supplies energy during the demagnetization phase of the boost inductor - so the magnetic part required is smaller than needed with any other topology. Therefore the boost topology leads to the cheapest solution. Figure 1 shows the general topology of a boost PFC. Its optimization requires careful adjustment of the following parameters:

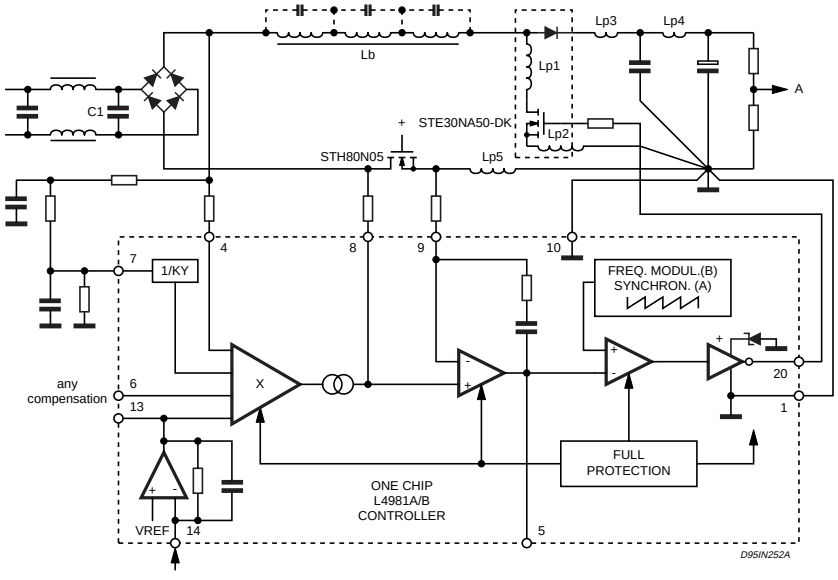
– the value of the input capacitor C_i

– the current ripple in the boost inductor L_b

– the parasitic capacitances of the boost inductor and power semiconductors, including those associated with the heatsink

– the operating frequency and also the frequency modulation technique.

Figure 1. Semiconductor Kit for PFC Schematic.



SEMI-CONDUCTOR KIT

The semiconductor kit consists of an L4981 controller, an STE36N50-DK power module and an STH80N05 power sense (see figure 1).

L4981A/B controller:

The L4981 operates with an input voltage range of 85V to 270V and uses average current mode PWM control, providing feed forward line and load compensation. Two versions are available: version (A) provides synchronization with the down stream converter, whereas version (B) provides linear frequency modulation, spreading the RFI noise spectrum.

Both versions incorporate overvoltage and overcurrent protection, soft start and under voltage lockout with programmable threshold.

Other features include an on chip voltage reference (2%) which is externally available, a typical starting current of only 0.5mA and separate grounds for the power and signal stages.

L4981 use an optimum current control method. It is an average current control using feed forward line regulation and variable or fixed switching frequency.

The oscillator simultaneously turns on the power switch and starts the ramp of the PWM current control. The average inductor current is compared with the current reference by means of the current error amplifier. It operates as an integrator, allowing the circuit to accurately follow the current reference generated by the multiplier. This current reference is obtained by sinewave modulating the error voltage of the voltage control loop.

A feed forward compensation of the mains voltage has been added to the multiplier in order to keep constant the voltage control loop bandwidth whatever the mains fluctuation. A fourth multiplier input allows external compensation to be applied to the current modulation.

The oscillator can operate at constant or modulated switching frequency. In applications where modulated frequency is used, the RFI noise spectrum can be spread adjusting the depth of modulation by means of an external resistor. Then the maximum inductor current occurs at the minimum operating frequency.

STE30NA50-DK Power Module:

Built in an isolated ISOTOP^{TM} package, which can be mounted directly on a PCB, this module integrates a low $R_{DS(ON)}$ Power MOSFET and a TURBOSWITCH^{TM} Diode. Putting these two components in a single isolated package with very low parasitic inductance and capacitance reduces the component count, and significantly reduces transient overvoltages, and EMI and RFI.

As a result, the design safety margin can be relaxed and the voltage rating of the power MOSFET can be just $500V_{(br)DSS}$, meaning also that the $R_{DS(on)}$ of the MOSFET can be lower - in this case it is 0.14 Ohm. Both the current and avalanche handling capabilities of the power MOSFET section are specified at 100°C junction temperature, allowing for maximum utilization of the device. The MOSFET is a low gate-charge type and so its drive requirements are compatible with the 2A peak current capability of the L4981 controller.

The integrated TURBOSWITCH^{TM} freewheeling diode is an ultra-fast, soft recovery device using planar epitaxial technology, and is a part of the STTA series. Its low trr (30ns) keeps the MOSFET switching losses to a minimum. Other ratings are $600V_{RRM}$ and a maximum V_F of 1.5V at the rated average forward current (I_{Fav} = 20A).

STH80N05 Power sense:

Using a high density low voltage Power MOSFET for current sensing has many advantages:

– low resistance, typically 10m2

– Can be mounted on the same heatsink as the ISOTOP
– intrinsic diode for controller input protection
– very low parasitic inductance improving signal/noise ratio.

However, the peak current limitation will be affected by the MOSFET thermal characteristic.

DESIGN RULE EXAMPLE

Taking the following operating conditions (see figure 2):

$V_{in\ rms}$ = 230Vac +10% -15% (f=50Hz)

$I_{in\ rms}$ = 16Arms

P_{out} = 3000W

V_{out} = 400Vdc

or

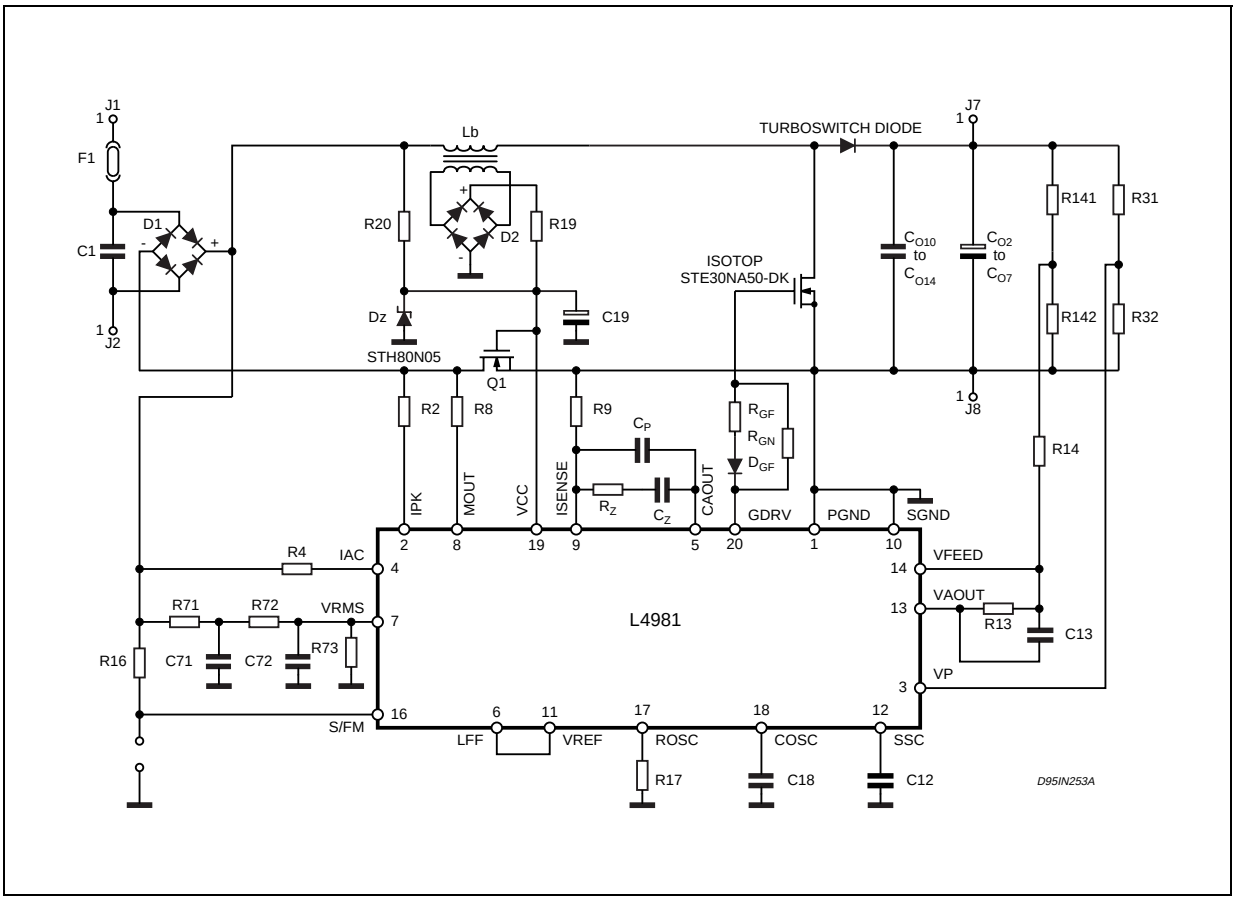
$V_{in\ rms}$ = 120Vac +20% -20% (f=60Hz)

$I_{in\ rms}$ = 15Arms

P_{out} = 1400W

V_{out} = 400Vdc

Figure 2. 1500W/3000W PFC Schematic.



Component List

1	1	C1	10µF/250Vac
2	6	Co2,Co3,Co4,Co5,Co8,Co7	330µF/450V
3	5	Co10,Co11,Co12,Co13,Co14	0.33µF/450V
4	1	Cp	tbd
5	1	Cz	150pF/100V
6	2	C12, C72	1µF/100V
7	1	C13	22nF/100V
8	1	C18	2.2nF/100V
9	1	C19	220µF/25V
10	1	C71	68nF/100V
11	1	DIODE	TURBOSWITCH
12	1	DgF	BYW100
13	1	D1	regular diode bridge or 2xMDS35
14	1	D2	4 x BYW100
15	1	F1	3AG FUSE
16	1	ISOTOP	STE36N50DK
17	2	J2, J1	CON5
18	2	J7, J8	CON2
19	1	Laux	Auxiliary winding
20	1	Lb	BOOST INDUCTOR
21	1	Q1	STH80N05
22	1	Rgf	1 1/4W
23	1	Rhn	4.7 1/2W
24	2	R72, Rz	100k 1/4W
25	2	R142, R2	10k 1/4W
26	2	R31, R4	1M 1/4W
27	1	R8, R9	4k 1/4W
28	1	R13	390k 1/4W
29	1	R14	47k 1/4W100k
30	1	R16	no R16 with L4981A
31	1	R17	24k 1/4W
32	1	R19	47 1W
33	1	R20	100k 2W
34	1	R32	4.7k 1/4W
35	1	R71	820k 1/4W
36	1	R73	22k 1/4W
37	1	R141	750k 1/4W
38	1	U1	L4981A/B

SWITCHING FREQUENCY fs is kept below 50kHz to maintain the RFI noise within the optimum frequency range of the VFG 243 standard. Figure 3 shows that in the range of 10kHz/50kHz the switching frequency fundamental spectrum requires less filtering. C18 = 2.2nF and R17 = 24k2 give a switching frequency of 46kHz.

BOOST INDUCTOR: For applications in the range of 3kW, the boost inductor design is greatly determined by material choice and core availability.

As mentioned the inductor parasitic capacitance determines the filter requirements in the range 1MHz-30MHz (with regards to the switching noise). To keep this capacitance as low as possible, a single layer winding is the best solution, but this requires the use of a toroidal core shape to balance winding turns and core section. In this case a material with distributed air gaps, for example iron powder, is a good choice (see #2).

This is the cheapest core material available with an inherently high saturation flux density combined with a distributed air gap. Test have been performed using two different cores:

– T300-26D core from MICROMETAL (Anaheim, CA) made of iron powder / 60 turns / 12 AWG.

– 2 x CO55866A2 core from MAGNETICS, made of nickel, iron and molybdenum / 46 turns / 12 AWG.

OUTPUT CAPACITANCE value depends upon the expected output voltage drop during the specified holdup time. Considering a value of 2000F, the voltage drop during a 10msec holdup can be calculated from:

Pout × 10msec = 1/2 Cout (Vout - Vmin)

then V_{min} = 382V at 1400W

and V_{min} = 360V at 3000W

FEED FORWARD COMPENSATION:

Pin 7 should be supplied with a voltage proportional to the rms mains voltage. This voltage must be in the range of 1.5V to 5.5V.

The circuit shown in figure 4 gives a good compromise between response time and harmonic attenuation with the following values: C71=68nF, C72 = 1mF, R71=820kΩ, R72 =1 00kΩ and R73 = 22kΩ.

Figure 3. VFG 243 LIMITS

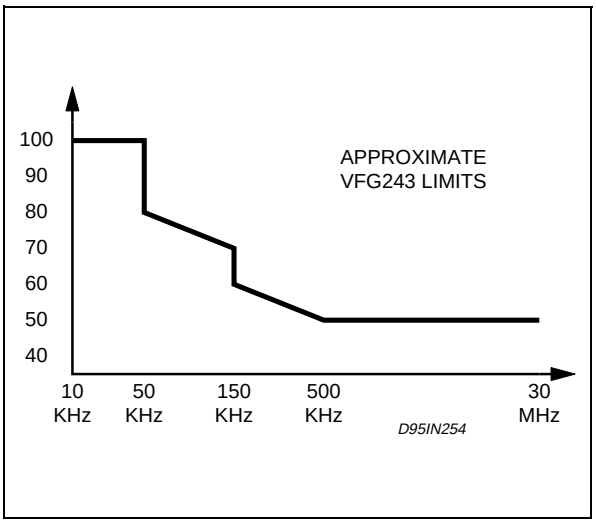
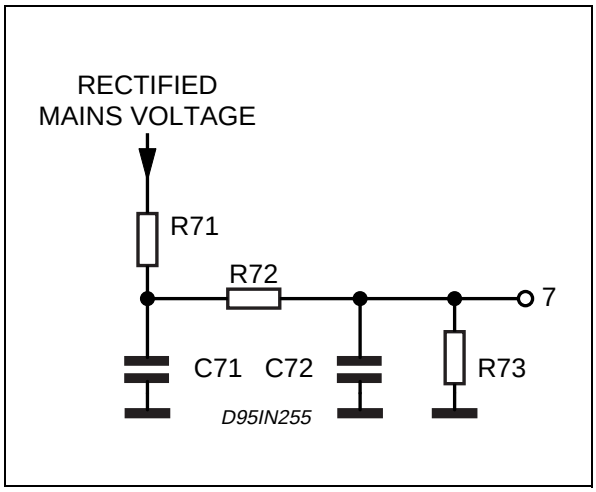


Figure 4. Feed Forward Compensation Network



VOLTAGE ERROR AMPLIFIER:

Operating with P_{out} = 3000W and V_{out} = 400Vdc, the mean I_{out} is 7.5A. The corresponding 100Hz capacitor current is defined by: $I_{capa} = (P_{out} / V_{out})$ cos 4!ft So the peak current is: P_{out}/V_{out} = 7.5A

Then the output voltage ripple V_r can be evaluated as:

$V_r = 7.5A / 2\pi \times 100 \times 3500 \times E\text{-}6 = 6Vpeak$

Voltage divider R141/R142 attenuates the output voltage ripple to:

V_{ri} = 6Vpeak x 5.1/400 = 0.0765Vpeak

Assuming 3% peak voltage ripple at the voltage error amplifier output, ripple can be evaluated as:

Vro = (5.1V - 1.27V) 0.03 = 0.115Vpeak

where the first term is the output error amplifier voltage range.

Then the global voltage error amplifier gain at 100Hz must be:

$G_{vea} = V_{ro}/V_{ri}$ = 0.115/0.0765 = 1.5

as G_{vea} # 1 / R14 2πf C13

with R14 = 47kΩ then C13=22nF

To maintain voltage loop stability requires the placement of a pole at a unity-gain frequency of about 18Hz (see #5)

then R13C13 = 1/2π · 18

and R13 = 390kΩ

LOAD COMPENSATION:

A voltage applied at pin 6 can be used to perform compensation, for example a load feed forward compensation. With reference to the multiplier section, this input is equivalent to the voltage error amplifier output. If not used, it should be connected to the reference voltage (pin 11).

MULTIPLIER circuit has the following response:

Imult = K_{mult} Iac (V_{vea}-1.27) (0.8LFF-1.27)/Vrms

where:

K_{mult} is the multiplier constant (.37) V_{vea} is the voltage error amplifier output. LFF is the voltage at pin 6.

Iac is the current supplied into pin 4. Vrms is voltage at pin 7.

To keep the maximum multiplier output current below 300µA, R4 should be set to 1MΩ, meaning I_{ac} rms varies from 95µA to 270µArms.

The previous equation gives: I_{mult} # 60µArms with Vin=95Vrms and Pout=1400W, or Vin=195Vrms and Pout=3000W.

CURRENT AMPLIFIER SECTION:

Using a low R_{DSon} Power MOSFET as current sense instead of a resistance leads to a reduction of the parasitic inductance and allows the heat generated to be dissipated in the heatsink. Using the specifications of the STH80N05, R_{sense} max is $11m_W$ at 25°C and $15m_W$ at 80°C.

Then the maximum rms voltage across the sense is:

RMS sense voltage = 15mΩ 16A = .24V

Then R8 = R9 = .24V / 60µA # 4kΩ

Critical current amplifier gain occurs when the current error amplifier slope exceeds the oscillator slope. This condition occurs when:

$V_{oca}\ f_s = (V_o/L_b)\ Rsense\ G_{ca}$

G_{ca} = current amplifier gain

V_{oca} = current amplifier output voltage

f_s = switching frequency

L_b = boost inductor value

Then $G_{ca} = V_{oca}\ f_s\ L_b / (V_o\ R_{sense})$ = 5 45E+3 0.8E-3 / 400 0.015 = 28

Setting G_{ca} # 25 enables the calculation of R_z and C_z:

R_z # G_{ca}R9 # 100kΩ

C_z = 1 / 2pfcRz with a crossover frequency fc of 10kHz.

then C_z=150pF.

Capacitor C_p can eventually be added to reduce the phase lag of the amplifier.

IMPLEMENTATION AND SWITCHING BEHAVIOR

Using a double-sided PCB significantly reduces the parasitic inductances of the circuit:

- parasitic inductance Lp1 and Lp2 shown in figure 1 are intrinsic characteristics of the ISOTOP module itself; these values are very low (less than 10nH).
- parasitic inductances Lp3 and Lp4 are due to the ISOTOP/capacitor loop. The proposed layout results in about 20 nH for Lp3+Lp4.

These values mean that the total voltage overshoot during the turn off of the MOSFET is limited to about 30V with a di/dt of 1000A/sec with no snubber.

- parasitic inductance Lp5 is a few nH due to the use of an active current sense in a TO- 218 package. This results in an excellent signal/ noise ratio at the current error amplifier input. The following measurements have been made with the iron powder inductor as described in paragraph 4.

Figure 5 shows the most important signals with an input voltage of 208Vac and an output power of 1600W. To show the current ripple more clearly, one second persistence has been used. The slight overshoot of the current error amplifier output during the mains zero voltage crossing is due to the rise of the inductor permeability at low induction. Indeed, the inductor size optimisation requires operation with 50% saturation of the iron at maximum peak current.

Figure 6 shows average values of the waveforms in figure 5.

Figure 7 shows the input current and voltage with 120Vac mains and 1600W output Power.

Figure 8 shows the drain voltage and source current during turn off. Note that the source current probing creates a parasitic inductance, limiting the di/dt. Thus there is no significant turn off overvoltage.

Figure 9 shows the diode recovery current with a forward current of 20A and a di/dt of 700A/µsec. Note that the R_{gn} gate drive resistance can be adjusted to tightly control the di/dt. This is still acting with high di/dt value due to the low parasitic inductance of the gate drive. Thermal measurements have been performed enabling the

junction temperature to be accurately estimated:

with :

V_{in} = 220Vac/I_{in} = 8Arms

V_{out} = 400Vdc/R_{gn} = 0Ω

MOSFET+DIODE conduction losses = 10W

MOSFET+DIODE commutat. losses = .52W/kHz

with:

V_{in} = 120Vac/I_{in} = 15Arms

V_{out} = 400Vdc/Rgn = 0Ω

MOSFET+DIODE conduction losses = 40W

MOSFET+DIODE commutat. losses = .88W/kHz

with a gate drive resistance R_{gn}=102, 25% must be added to the commutation losses.

Figure 5. Current & Voltage Recorders-

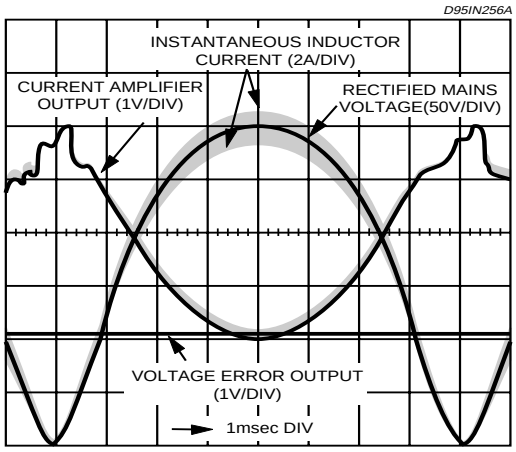


Figure 6. Average Current & Voltage-

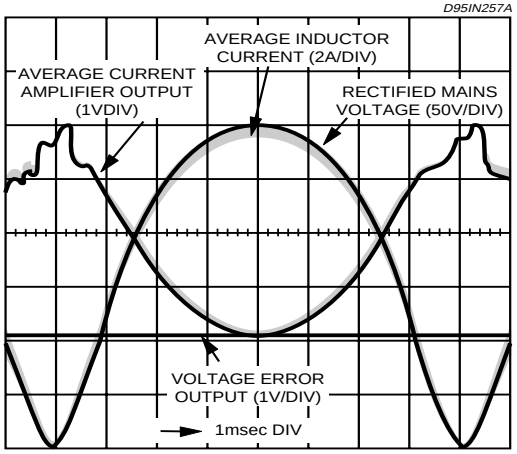


Figure 7. Average Current & Voltage-

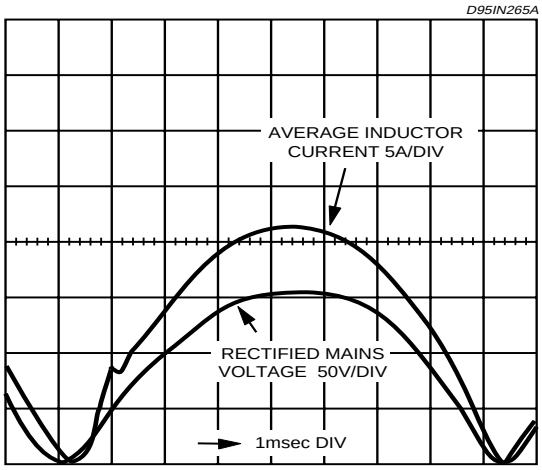


Figure 8. Turn Off Mosfet behavior-

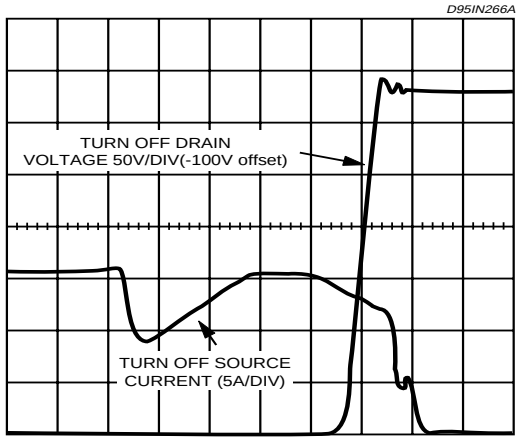
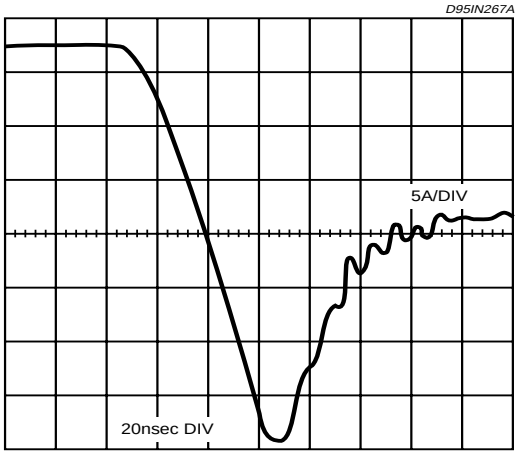


Figure 9. Diode Recovery Current



CONCLUSIONS

This paper presents an optimized Power Factor Corrector built around a power module driven by the L4981 control IC. This STE36N50-DK ISOTOP power module is mounted directly on the PCB providing both very low inductance layout and compact hardware.

Eliminating parasitic inductances enables tight control of switching di/dt and prevents turn off overvoltage. Therefore faster switching speeds are allowed to reduce switching losses. The 2Amps current capability of the controller is also a useful feature.

Combined with a single layer winding inductor, such a configuration results in very low EMI and RFI generation.

Finally, there is potential for further improvements using two features of the L4981:

– the possibility either to synchronize the IC with an external signal, or to modulate the PFC switching frequency to spread the RFI noise.

– the extra multiplier input, which enables external compensation.