Getting started with STM32U5 MCU hardware development

Introduction

This application note is intended for system designers who require a hardware implementation overview of the development board features: power supply, clock management, reset control, boot mode settings, and debug management.

It details how to use the STM32U5 series microcontrollers (named STM32U5) and describes the minimum hardware resources required to develop an application using these MCUs.

This document also includes detailed reference design schematics with the description of the main components, interfaces, and modes.

1 General information

This document applies to the STM32U5 series Arm® Cortex®-M33-based microcontrollers.

Note: *Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.*

Reference documents

[1] Reference manual *STM32U5 series Arm®-based 32-bit MCUs* (RM0456)

[2] Application note *STM32 microcontroller system memory boot mode* (AN2606)

[3] Application note *Oscillator design guide for STM8AF/AL/S, STM32 MCUs and MPUs* (AN2867)

[4] Application note *STM32 MCUs secure firmware install (SFI) overview* (AN4992)

2 Power supply management

2.1 Power supplies

The STM32U5 devices require a 1.71 to 3.6 V operating voltage supply (V_{DD}).

The independent supplies listed below, can be provided for specific peripherals:

- **V_{DD}** = 1.71 V to 3.6 V
  V_{DD} is the external power supply for the I/Os, the internal regulator, and the system analog such as reset, power management, and internal clocks. V_{DD} is provided externally through the VDD pins.
- **V_{DDA}** = 1.62 V (ADCs/COMPs/DACs/OPAMPs) / 1.8 V (VREFBUF) to 3.6 V
  V_{DDA} is the external-analog power supply for A/D converters, D/A converters, voltage reference buffer, operational amplifiers, and comparators. The V_{DDA} voltage level is independent from the V_{DD} voltage. The VDDA pin must preferably be connected to the V_{DD} voltage supply when these peripherals are not used.

Note: In case the VDDA pin is left at high impedance or is tied to VSS, the maximum input voltage that can be applied on the I/Os with "_a" I/O structure, is reduced (refer to device datasheet for more details).

- **V_{DDSMPS}** = 1.71 V to 3.6 V
  V_{DDSMPS} is the external power supply for the SMPS step-down converter. It is provided externally through the VDDSMPS pin, and must be connected to the same supply as VDD pin when the SMPS is used in the application. When the SMPS is not used, it is recommended to connect both V_{DDSMPS} and V_{LXSMPS} to ground.
- **V_{LXSMPS}**
  The VLXSMPS pin is the switched SMPS step-down converter output.

Note: The SMPS output can not be used to power external components.

- **V_{DD11}**
  V_{DD11} is a digital core supply provided through the internal SMPS step-down converter VLXSMPS pin. VDD11 pins (two or three) are present only on packages with internal SMPS, connected to a total of 4.7 µF (typical) external capacitors.
- **V_{CAP}**
  V_{CAP} is the digital core supply, from the internal LDO regulator. VCAP pins (one or two) are present only on packages with LDO only (without SMPS), connected to a total of 4.7 µF (typical) external capacitor.

Note:
- *In case there are two VCAP pins (UFBGA169 package), each pin must be connected to a 2.2 µF capacitor, for a total around 4.4 µF.*
- *The SMPS power supply pins (VLXSMPS, VDD11, VDDSMPS, VSSSMPS) are available only on packages with SMPS. In such packages, the STM32U5 devices embed two regulators, one LDO and one SMPS in parallel, to provide the V_{CORE} supply to digital peripherals. A 4.7 µF total external capacitor and a 2.2 µH coil are required on VDD11 pins.*
- *The flash memory is supplied by V_{CORE} and V_{DD}.*

- **V_{DDUSB}** = 3.0 V to 3.6 V
  V_{DDUSB} is the external-independent power supply for USB transceivers. The V_{DDUSB} voltage level is independent from the V_{DD} voltage. The VDDUSB pin must preferably be connected to the V_{DD} voltage supply when the USB is not used.

Note: In case the VDDUSB pin is left at high impedance or is tied to VSS, the maximum input voltage that can be applied on the I/Os with "_u" I/O structure, is reduced (refer to device datasheet for more details).

- **$V_{DD11USB}$** = 1.0 V to 1.26 V (only available on STM32U59x/5Ax/5Fx/5Gx devices)
  $V_{DD11USB}$ is the external power supply for the USB transceiver. This supply is only available on specific packages and must be connected to VDD11.
- **V_{DDIO2}** = 1.08 V to 3.6 V
  V_{DDIO2} is the external power supply for 14 I/Os (port G[15:2]). The V_{DDIO2} voltage level is independent from the V_{DD} voltage, and must preferably be connected to V_{DD} when PG[15:2] is not used.

Note: On small packages, V_{DDA}, V_{DDIO2}, or V_{DDUSB} independent power supplies may not be present as a dedicated pin, and are internally bonded to a VDD pin. They are neither present when the related features are not supported on the product.

- **V_{BAT}** = 1.55 V to 3.6 V
  V_{BAT} is the power supply when V_{DD} is not present (through power switch) for RTC, TAMP, external clock 32 kHz oscillator, backup registers, and optionally backup SRAM.
- **V_{REF-}, V_{REF+}**
  V_{REF+} is the input reference voltage for ADCs and DACs. It is also the output of the internal voltage reference buffer (VREFBUF) when enabled. The VREF+ pin can be grounded when ADC and DAC are not active.
  The internal voltage reference buffer supports four output voltages that are configured with the VRS[2:0] field in VREFBUF_CSR register:
  – V_{REF+} around 1.5 V. This requires $V_{DDA} \geq 1.8$ V.
  – V_{REF+} around 1.8 V. This requires $V_{DDA} \geq 2.1$ V.
  – V_{REF+} around 2.048 V. This requires $V_{DDA} \geq 2.4$ V.
  – V_{REF+} around 2.5 V. This requires $V_{DDA} \geq 2.8$ V.

  VREF- and VREF+ pins are not available on all packages. When not available, they are bonded to VSSA and VDDA pins, respectively.
  When the VREF+ pin is double-bonded to VDDA in a package, the internal VREFBUF is not available, and must be kept disabled.
  V_{REF-} must always be equal to V_{SSA}.
- **V_{DDDSI}** = 1.71 V to 3.6 V (only available on STM32U59x/5Ax/5Fx/5Gx devices)
  V_{DDDSI} is the external power supply for the DSI controller. It is provided externally through the VDDDSI supply pin, and must be connected to the same supply as VDD pin.
- **$V_{DD11DSI}$** = 1.0 V to 1.26 V (only available on STM32U59x/5Ax/5Fx/5Gx devices)
  $V_{DD11DSI}$ is the external power supply for the DSI transceiver and must be connected to VDD11.

The following figures present an overview of the STM32U5 devices power supply, depending on the SMPS presence.

Figure 1. STM32U535xxxxQ and STM32U545xxxxQ power supply overview (with SMPS)

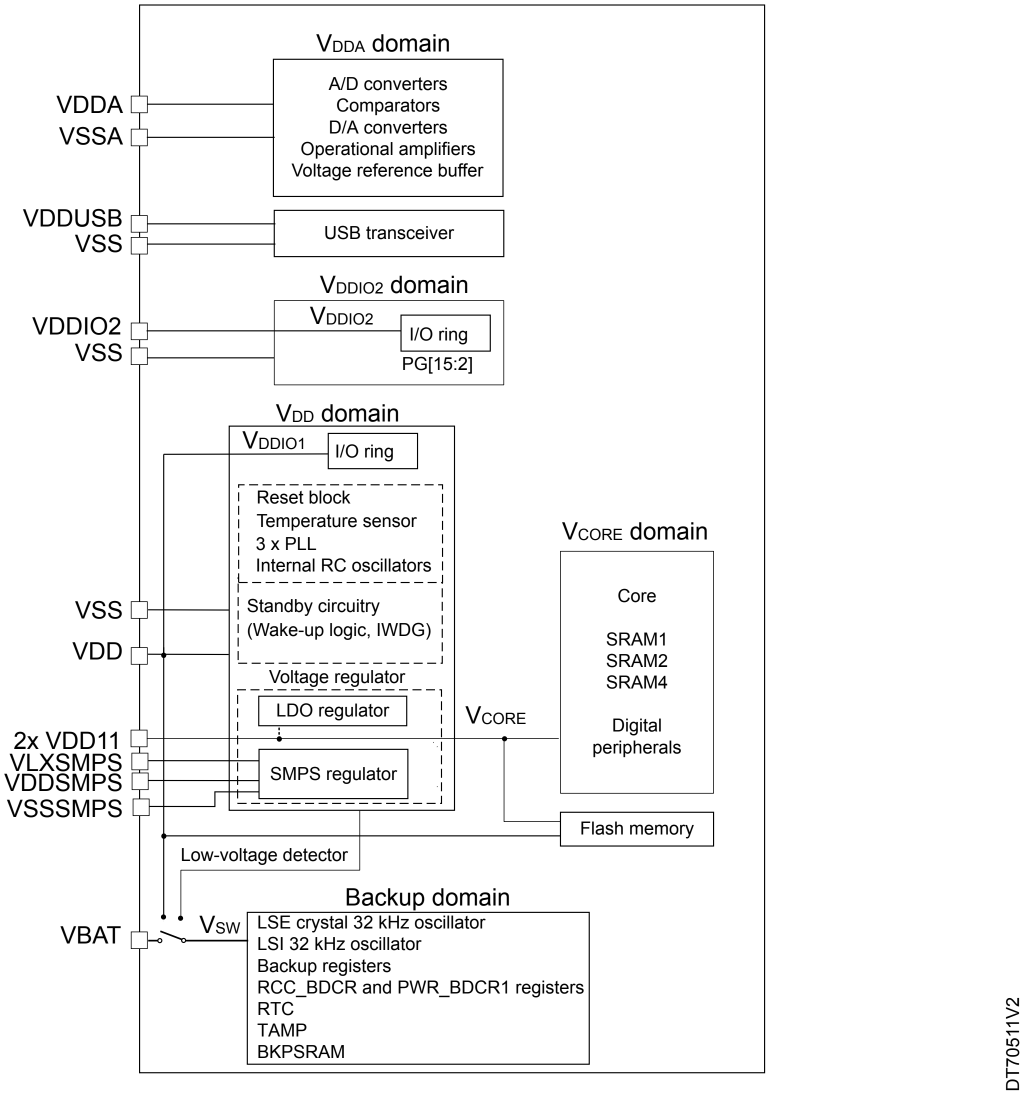
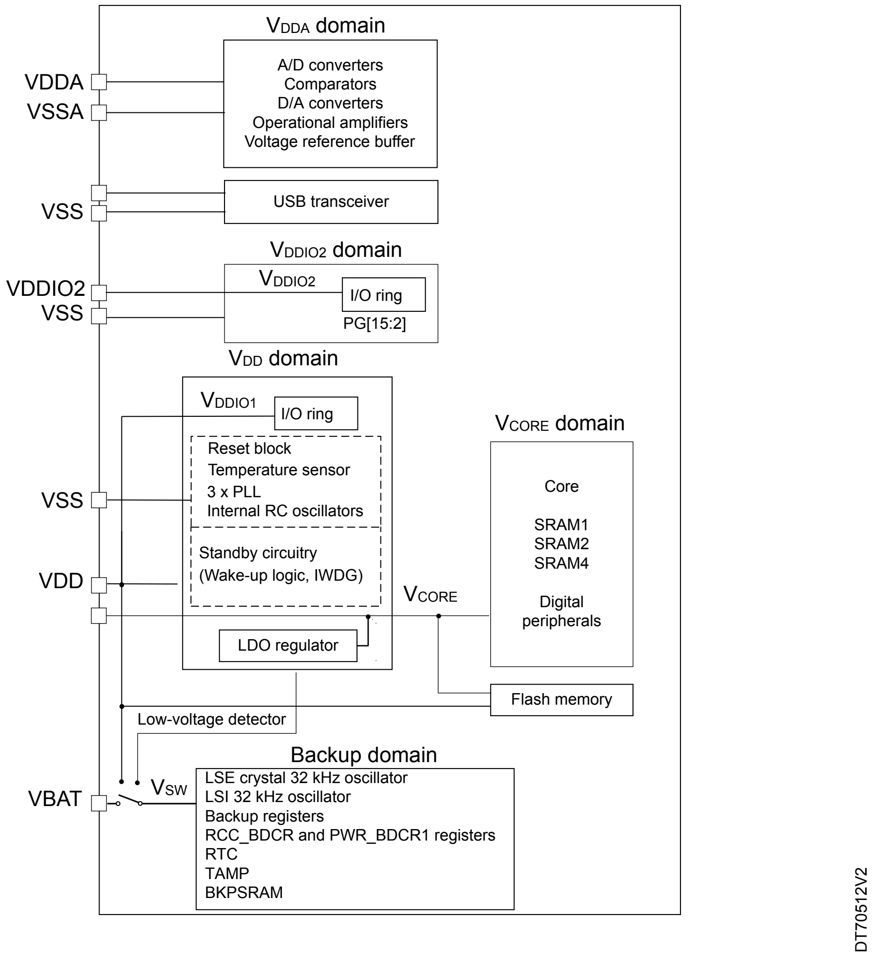


Figure 2. STM32U535xx and STM32U545xx power supply overview (without SMPS)



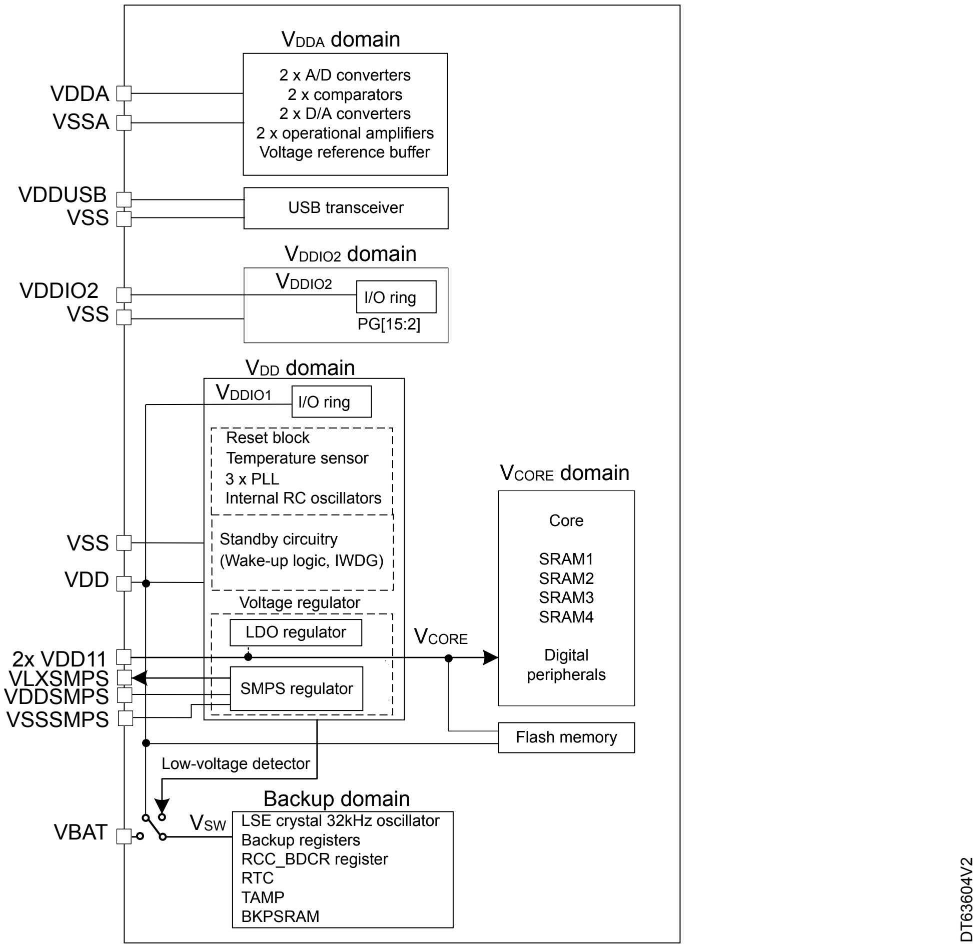


Figure 3. **STM32U575xQ and STM32U585xQ power supply overview (with SMPS)**

Figure 4. STM32U575xx and STM32U585xx power supply overview (without SMPS)

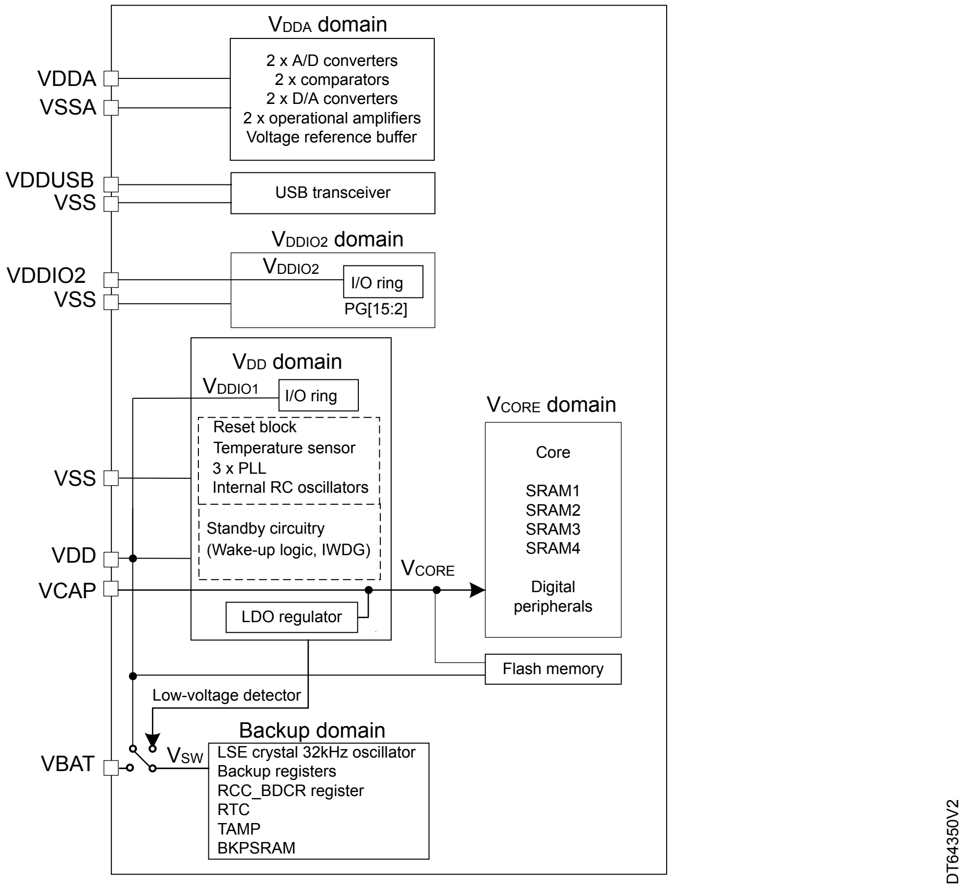
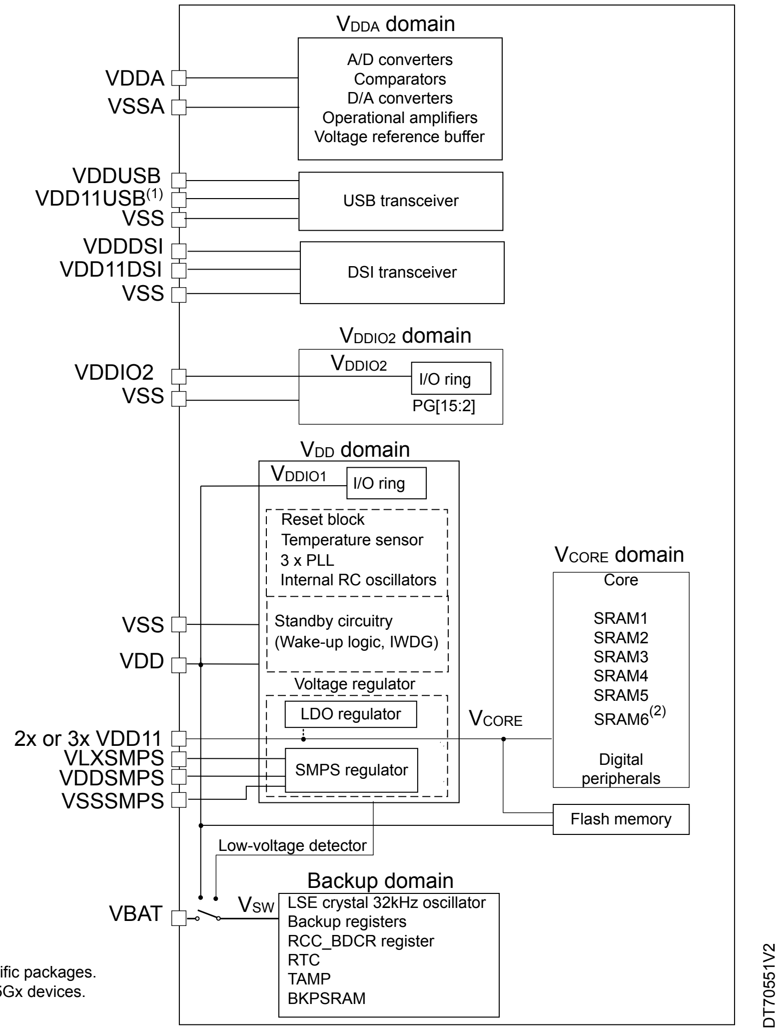
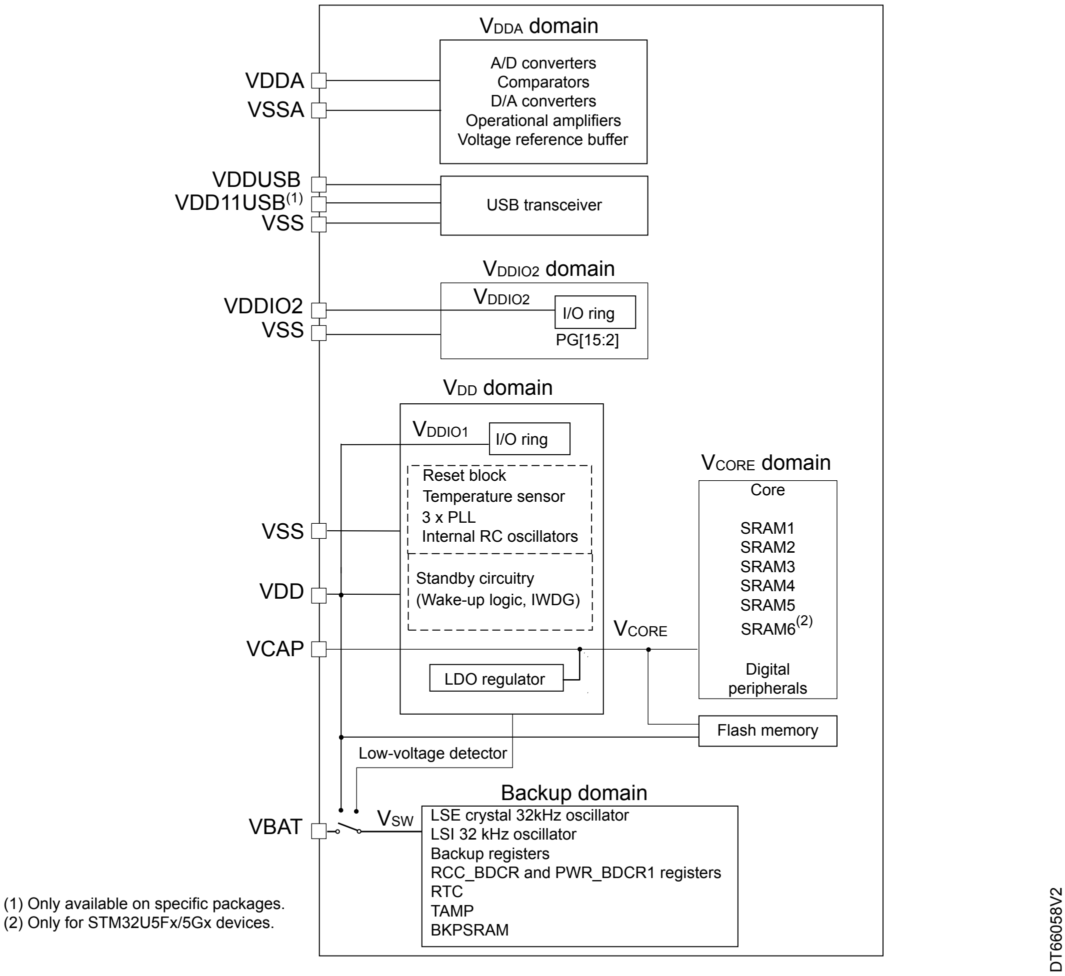


Figure 5. STM32U5F/5G/59/5AxxxxxQ power supply overview (with SMPS)



(1) Only available on specific packages.
(2) Only for STM32U5Fx/5Gx devices.

Figure 6. STM32U5F/5G/59/5Axxx power supply overview (without SMPS)



In devices without SMPS, the V_{DD} supply source feeds the I/Os and system analog peripherals (such as PLLs and reset block). The V_{CORE} power supply for digital peripherals and memories is generated from the LDO.

Note: *If the selected package has the SMPS step-down converter option but the SMPS is not used by the application (and the embedded LDO is used instead), the SMPS power supply pins must be set as follows:*

- *VDDSMPS and VLXSMPS connected to VSS*
- *VDD11 pins connected to VSS through two 2.2 µF capacitors as in normal mode*

2.1.1 Independent analog peripherals supply

To improve ADC and DAC conversion accuracy and to extend the supply flexibility, the analog peripherals have an independent power supply that can be separately filtered and shielded from noise on the PCB.

The voltage supply input of the analog peripherals is available on a separate VDDA pin. An isolated supply ground connection is provided on VSSA pin.

The V_{DDA} supply voltage can be different from V_{DD}. After reset, the analog peripherals supplied by V_{DDA} are logically and electrically isolated and therefore are not available. The isolation must be removed before using these peripherals, by setting the ASV bit in PWR_SVMCR, once the V_{DDA} supply is present.

The V_{DDA} supply can be monitored by analog voltage monitors (AVM), and compared with two thresholds (1.6 V for AVM1 or 1.8 V for AVM2). For more details, refer to the device datasheet and section *Peripheral voltage monitoring (PVM)* of document [1].

When a single supply is used, the VDDA pin can be externally connected to the same V_{DD} supply, through an external filtering circuit, to ensure a noise-free V_{DD} reference voltage.

ADC and DAC reference voltage

To ensure a better accuracy on low-voltage inputs and outputs, the user can connect to VREF+ pin, a separate reference voltage lower than V_{DDA}.

V_{REF+} is the highest voltage, represented by the full-scale value, for an analog input (ADC) or output (DAC) signal. V_{REF+} can be provided either by an external reference or by the VREFBUF that can output a configurable voltage: 1.5, 1.8, 2.048 or 2.5 V. The VREFBUF can also provide the voltage to external components through the VREF+ pin.

For further information, refer to the device datasheet and section *Voltage reference buffer (VREFBUF)* of document [1].

2.1.2 Independent I/O supply rail

Some I/Os from port G (PG[15:2]) are supplied from a separate supply rail. The power supply for this rail can range from 1.08 V to 3.6 V, and is provided externally through the VDDIO2 pin. The V_{DDIO2} voltage level is completely independent from V_{DD} or V_{DDA}.

The VDDIO2 pin is available only for some packages (refer to the pinout details in the datasheet for the I/O list).

After reset, the I/Os supplied by V_{DDIO2} are logically and electrically isolated and are therefore not available. The isolation must be removed before using any I/O from PG[15:2], by setting the IO2SV bit in PWR_SVMR, once the V_{DDIO2} supply is present.

The V_{DDIO2} supply is monitored by the V_{DDIO2} voltage monitoring (IO2VM) and compared with the internal reference voltage (3/4 V_{REFINT}, around 0.9 V).

For more details, refer to the device datasheet and section *Peripheral voltage monitoring (PVM)* of document [1].

2.1.3 Independent USB transceiver supply

The USB transceivers are supplied from a separate V_{DDUSB} power supply. V_{DDUSB} range is from 3.0 V to 3.6 V and is completely independent from V_{DD} or V_{DDA}.

After reset, the USB features supplied by V_{DDUSB} are logically and electrically isolated, and are therefore not available. The isolation must be removed before using the USB OTG peripheral, by setting the USV bit in the PWR_SVMR register, once the V_{DDUSB} supply is present.

The V_{DDUSB} supply is monitored by the USB voltage monitoring (UVM) and compared with the internal reference voltage (V_{REFINT}, around 1.2 V). For more details, refer to the device datasheet and section Peripheral voltage monitoring (PVM) of document [1].

For STM32U59x/5Ax/5Fx/5Gx devices only, the USB high-speed transceiver can be supplied from an optional power supply $V_{DD11USB}$. $V_{DD11USB}$ range is from 1.0 V to 1.26 V and must be connected to V_{DD11}.

2.1.4 Battery backup domain

To retain the content of the backup registers and supply the RTC when V_{DD} is turned off, the VBAT pin can be connected to an optional backup voltage, supplied by a battery or by another source.

The VBAT pin powers RTC, TAMP, LSE oscillator, and PC13 to PC15 I/Os. That allows the RTC to operate even when the main power supply is turned off.

The backup SRAM is optionally powered through the VBAT pin, when the BREN bit is set in PWR_BDCR1.

The switch to the V_{BAT} supply is controlled by the power-down reset embedded in the reset block.

Caution:

- During $t_{RSTTEMPO}$ (at V_{DD} startup) or after a PDR (power-down reset) detection, the power switch between V_{BAT} and V_{DD} remains connected to the VBAT pin.
- During the startup phase, if V_{DD} is established in less than $t_{RSTTEMPO}$ (refer to the datasheet for $t_{RSTTEMPO}$ value), and $V_{DD} > V_{BAT} + 0.6$ V, a current may be injected into the VBAT pin through an internal diode connected between the VDD pin and the power switch (VBAT). If the power supply/battery connected to the VBAT pin cannot support this current injection, it is strongly recommended to connect an external low-drop diode between this power supply and the VBAT pin.

If no external battery is used in the application, it is recommended to connect the VBAT pin externally to V_{DD} with a 100 nF external ceramic decoupling capacitor.

When the backup domain is supplied by V_{DD} (analog switch connected to the VDD pin), the following pins are available:

- PC13, PC14, and PC15 that can be used as GPIO pins
- PC13, PC14, and PC15 that can be configured by RTC or LSE (refer to the RTC section of document [1])
- Pins listed below, that are configured by TAMP as tamper pins:
  - PE3 (TAMP_IN6/TAMP_OUT3)
  - PE4 (TAMP_IN7/TAMP_OUT8)
  - PE5 (TAMP_IN8/TAMP_OUT7)
  - PE6 (TAMP_IN3/TAMP_OUT6)
  - PC13 (TAMP_IN1/TAMP_OUT2)
  - PA0 (TAMP_IN2/TAMP_OUT1)
  - PA1 (TAMP_IN5/TAMP_OUT4)
  - PC5 (TAMP_IN4/TAMP_OUT5)

Note:
- *Because the power switch can transfer only a limited amount of current (3 mA), the use of PC13 to PC15 I/Os in output mode is restricted: the speed must be limited to 2 MHz with a maximum load of 30 pF. These I/Os must not be used as current source (for example to drive an LED).*
- *Under V_{DD}, TAMP_OUTx pins (PE3, PE4, PE5, PE6, PA0, PA1, PC5) keep the same speed features as the GPIOs to which they are connected. However, under V_{BAT}, the speed of TAMP_OUTx pins must be limited to 500 kHz.*
- *The speed of the PC13 pin is always limited to 2 MHz, under V_{DD} or under V_{BAT}.*

Backup domain access

After a system reset, the backup domain (RCC_BDCR, PWR_BDCR1, RTC, TAMP and backup registers, plus backup SRAM) is protected against possible unwanted write accesses. To enable access to the backup domain, proceed as follows:

1. Enable the power interface clock by setting the PWREN bit RCC_AHB3ENR.
2. Set the DBP bit in PWR_DBPR to enable access to the backup domain.

V_{BAT} battery charging

When V_{DD} is present, the external battery can be charged on V_{BAT} through an internal resistance, 5 kΩ, or 1.5 kΩ, depending on the VBRS bit in PWR_BDCR2.

The battery charging is enabled by setting VBE bit in PWR_BDCR2. It is automatically disabled in VBAT mode.

2.1.5 Voltage regulator

The STM32U5 devices embed the following internal regulators in parallel to provide the V_{CORE} supply for digital peripherals, SRAMs, and the embedded flash memory:

- SMPS step-down converter
- LDO (linear voltage regulator)

They can be selected when the application runs, depending on the application requirements. The SMPS allows the power consumption to be reduced. However, the noise generated by the SMPS may impact some peripheral behaviors, requiring the application to switch to LDO when running the peripheral, in order to reach the best performances.

Except for Standby circuitries and the Backup domain, LDO or SMPS can be used in all voltage scaling ranges (range 1/2/3/4), in all Stop modes (Stop 0/1/2/3), and in Standby mode with SRAM2. Refer to the low-power mode summary table in document [1].

On some packages, the SMPS supply pins are not available, consequently only the LDO might be used to supply V_{CORE} domain.

Dynamic Voltage scaling management

Both LDO and SMPS regulators can provide four different voltages (voltage scaling) and can operate in all Stop modes. Both regulators also can operate in the following ranges:

- **Range 1 (1.2 V, 160 MHz)**, high performance: provides a typical output voltage at 1.2 V. It is used when the system clock frequency is up to 160 MHz.
- **Range 2 (1.1 V, 110 MHz)**, medium-high performance: provides a typical output voltage at 1.1 V. It is used when the system clock frequency is up to 110 MHz.
- **Range 3 (1.0 V, 55 MHz)**, medium-low power: provides a typical output voltage at 1.0 V. It is used when the system clock frequency is up to 55 MHz.
- **Range 4 (0.9 V, 24 MHz)**, low power: provides a typical output voltage at 0.9 V. It is is used when the system clock frequency is up to 24 MHz.

Voltage scaling is selected through the VOS[1:0] field in PWR_VOSR.

Caution: The EPOD (embedded power distribution) booster must be enabled and ready before increasing the system clock frequency above 50 MHz in Range 1 and Range 2 (refer to document [1] for sequences to switch between voltage scaling ranges).

2.1.6 Power supply for I/O analog switches

Some I/Os embed analog switches for both analog peripherals (ADCs, COMPs, DACs) and TSC (touch sensing controller) functions. These switches are by default supplied by V_{DDA}. However, they can be supplied by a V_{DDA} voltage booster or by V_{DD}, depending on the configuration of ANASWVDD and BOOSTEN bits in SYSCFG_CFGR1.

It is recommended to supply the I/O switches with the highest voltage value between V_{DDA}, V_{DDA} booster, and V_{DD}.

Note: If possible, select V_{DDA} or V_{DDA} booster rather than V_{DD}, as they are often less noisy.

The analog switches for TSC function are supplied by V_{DD}.

2.2 Power supply schemes

The device is powered by a stabilized V_{DD} power supply as described below:

- **VDD pins** must be connected to V_{DD} with external decoupling capacitors: a 10 µF (typical value, 4.7 µF minimum) single tantalum or ceramic capacitor for the package, and a 100 nF ceramic capacitor for each VDD pin.
- **VDD11 pins** are present only on packages with SMPS. The SMPS step-down converter requires a 2.2 µH (typical) external ceramic coil connected between VLXSMPS and VDD11 pins. In addition, two 2.2 µF capacitors on VDD11 pins are connected to the VSSSMPS pin.
- The **VCAP pin** is present only on standard packages (without SMPS). It requires a 4.7 µF (typical) external decoupling capacitor connected to V_{SS}. If there are two VCAP pins (UFBGA169 package), each VCAP pin must be connected to a 2.2 µF (typical) capacitor (for a total around 4.4 µF).
- The **VDDA pin** must be connected to two external decoupling capacitors: 100 nF ceramic and 1 µF tantalum or ceramic.
  Additional precautions can be taken to filter digital noise: VDDA can be connected to VDD through a ferrite bead.
- The **VREF+ pin** can be provided by an external voltage reference. In this case, an external 100 nF + 1 µF tantalum or ceramic capacitor must be connected on this pin.
  It can also be provided internally by the VREFBUF. In this case, an external 1 µF (typical) capacitor must be connected on this pin.
- The **VBAT pin** can be connected to an external battery to preserve the content of the Backup domain:
  – When VDD is present, the external battery can be charged on VBAT through a 5 kΩ or 1.5 kΩ internal resistor. In this case, the user can insert a capacitor according to the expected discharging time (1 µF is recommended).
  – If no external battery is used in the application, it is recommended to connect the VBAT pin to V_{DD} with a 100 nF external ceramic decoupling capacitor.

Figure 7. Power supply scheme for U535/545/575/585xxxxQ (with SMPS)

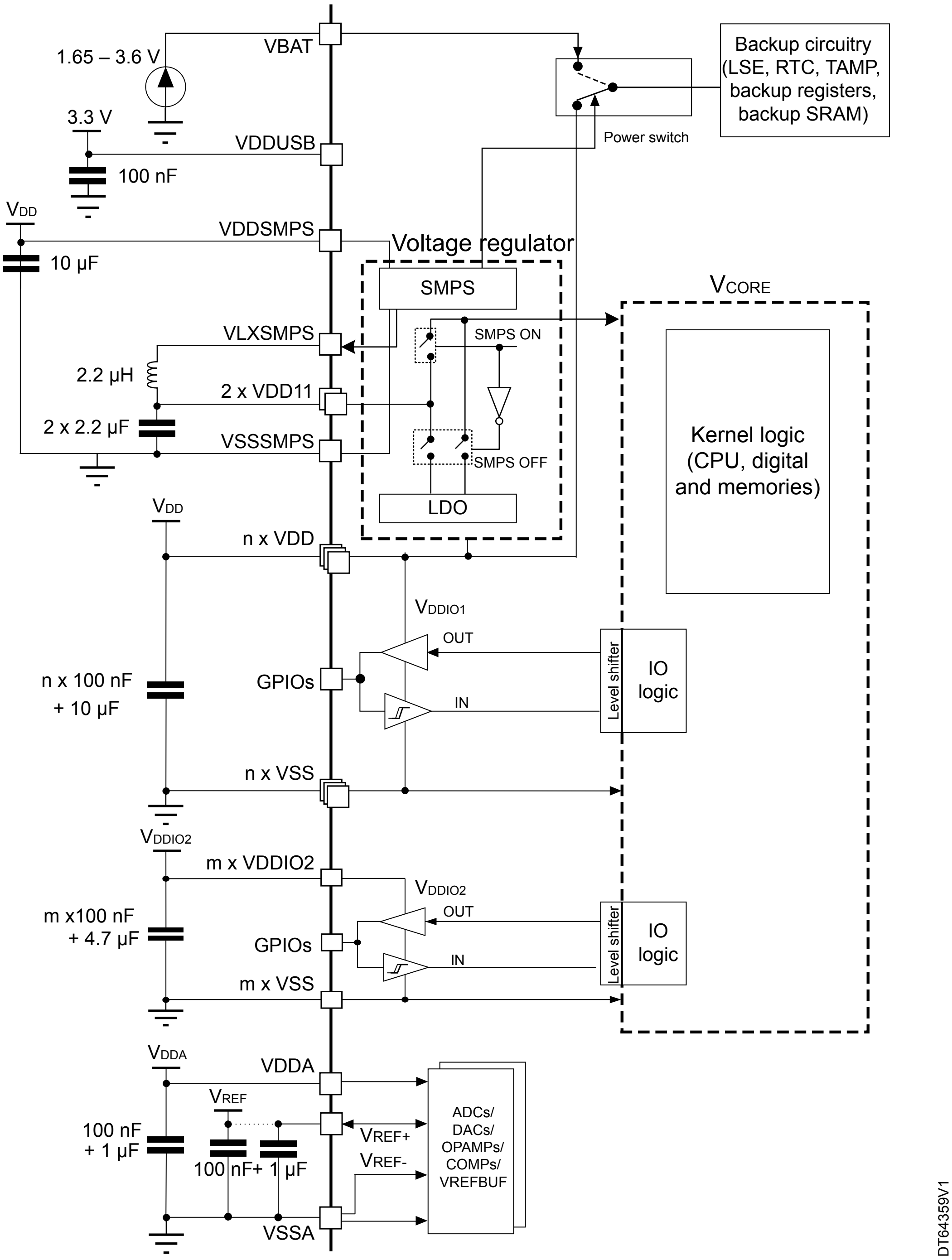
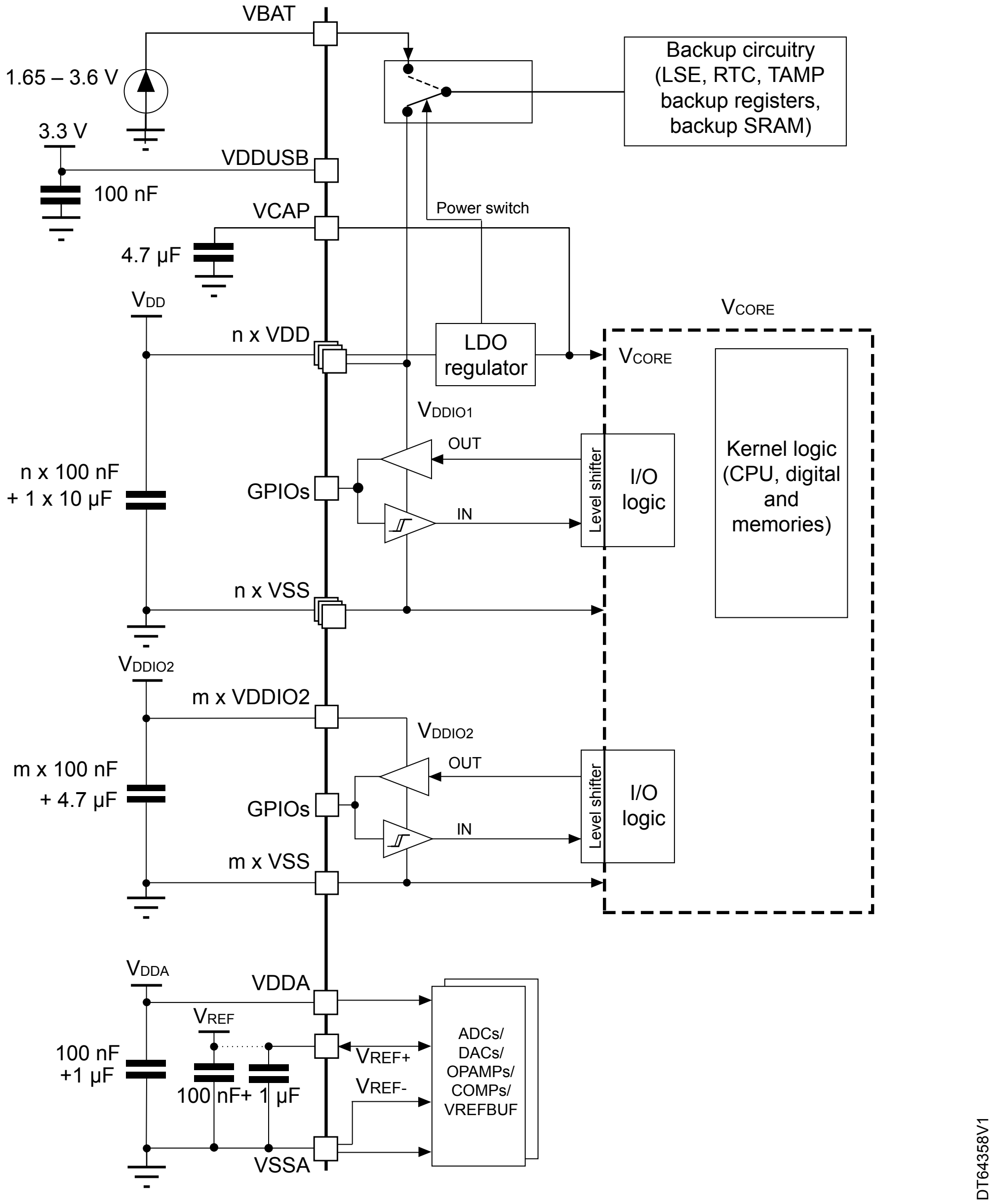


Figure 8. **Power supply scheme for STM32U535/545/575/585xx (without SMPS)**



Caution: If there are two VCAP pins (UFBGA169 package), each pin must be connected to a 2.2 µF (typical) capacitor (for a total around 4.4 µF).

Figure 9. Power supply scheme for STM32U5F/5G/59/5Axxx (with SMPS)

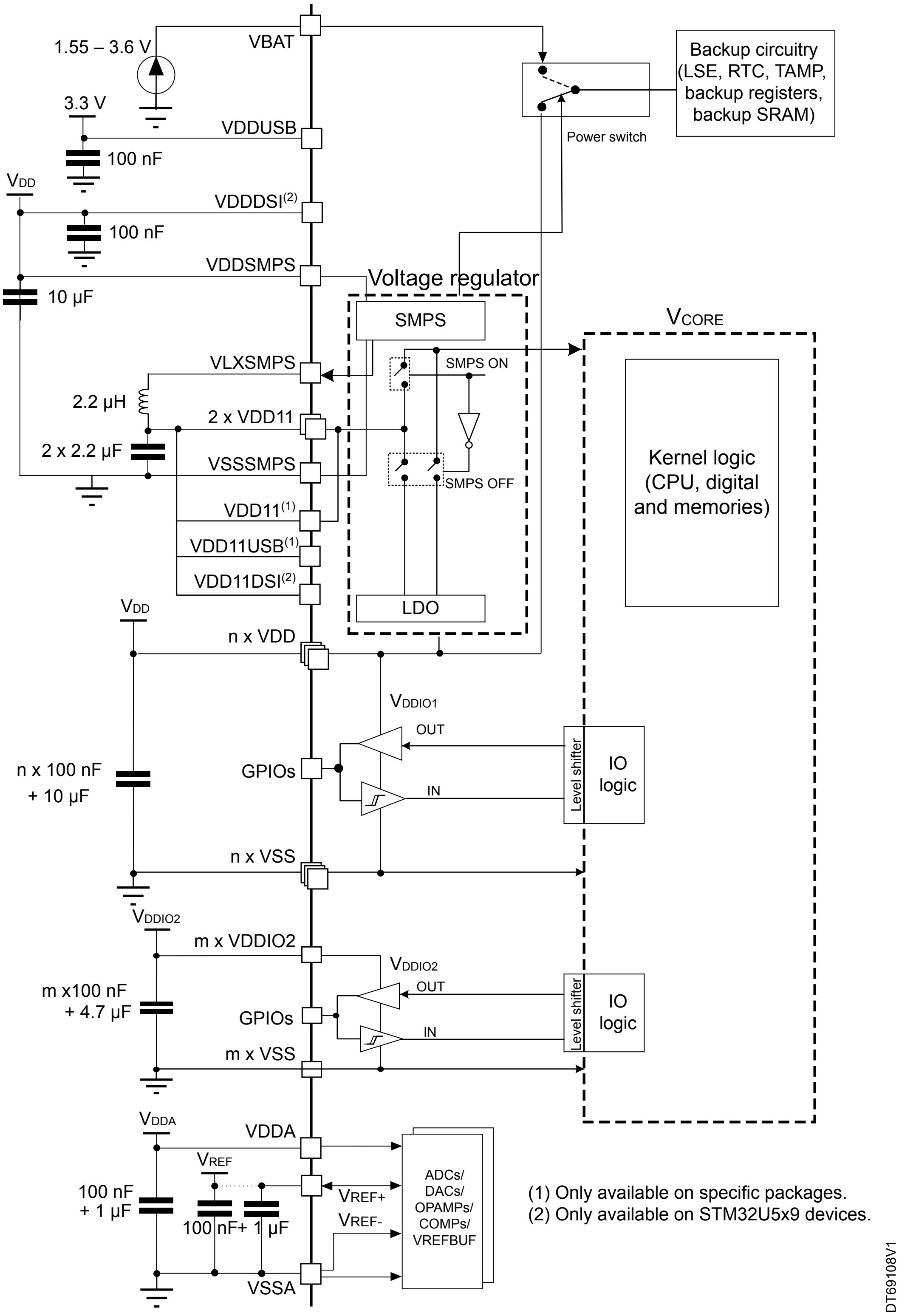
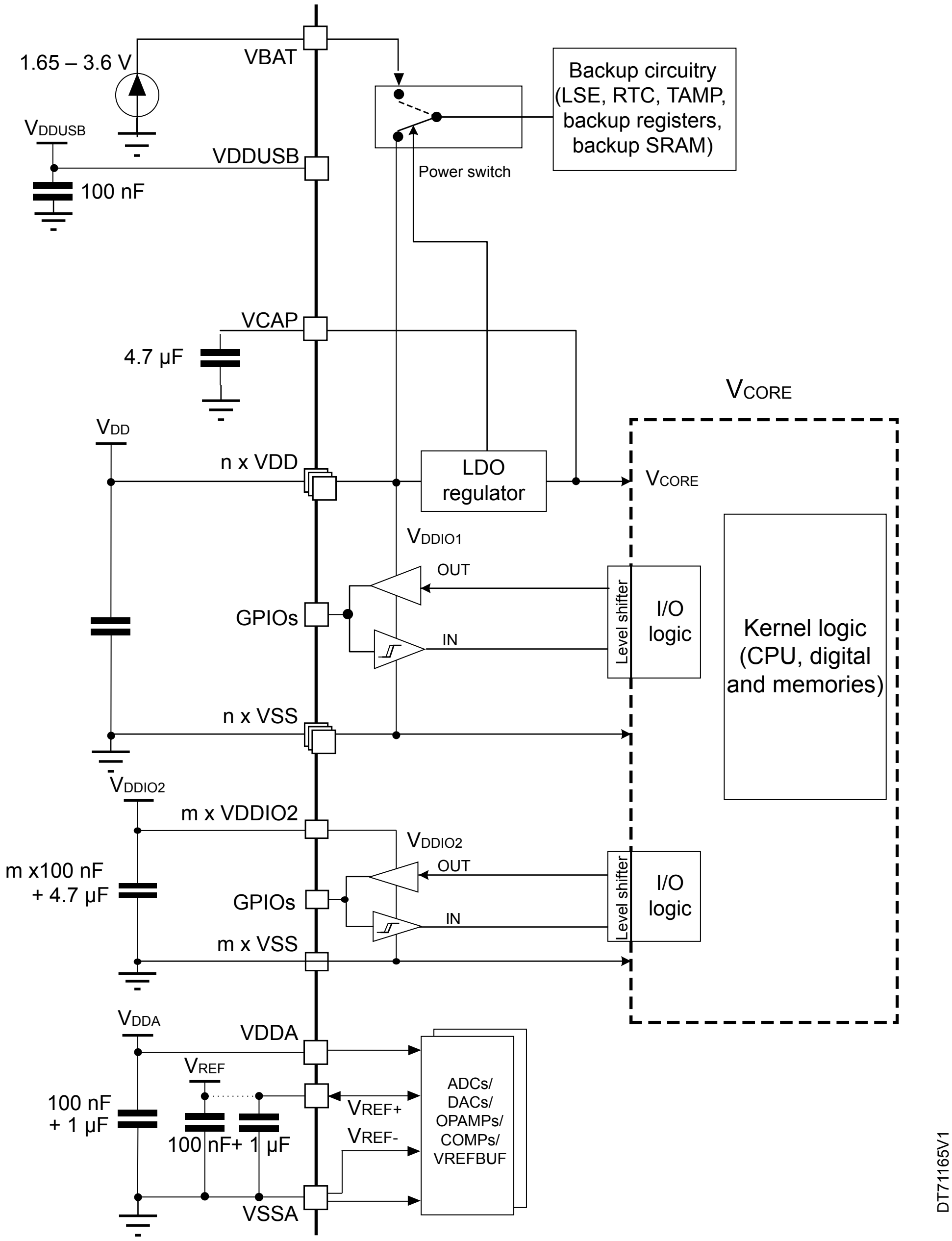


Figure 10. **Power supply scheme for STM32U5F/5G/59/5Axxx (without SMPS)**



Note:
- *SMPS and LDO regulators provide, in a concurrent way, the V_{CORE} supply depending on application requirements. However, only one of them is active at the same time. When SMPS is active, it feeds the V_{CORE} on the two VDD11 pins provided through the SMPS VLXSMPS output pin. A 2.2 µH coil and a 2.2 µF capacitor on each VDD11 pin are then required. When LDO is active, it provides the V_{CORE} and regulates it using the same decoupling capacitors on VDD11 pins.*
- *It is recommended to add a decoupling capacitor of 100 nF near each VDD11 pin/ball, but it is not mandatory.*

2.3 Power supply sequence between V_{DDA}, V_{DDUSB}, V_{DDIO2}, and V_{DD}

2.3.1 Power supply isolation

The devices feature a powerful reset system that ensures the main power supply (V_{DD}) has reached a valid operating range before releasing the MCU reset.

This reset system is also in charge of isolating the independent power domains: V_{DDA}, V_{DDUSB}, V_{DDIO2}, and V_{DD}. This reset system is supplied by V_{DD} and is not functional before V_{DD} reaches a minimal voltage (1 V in worse-case conditions).

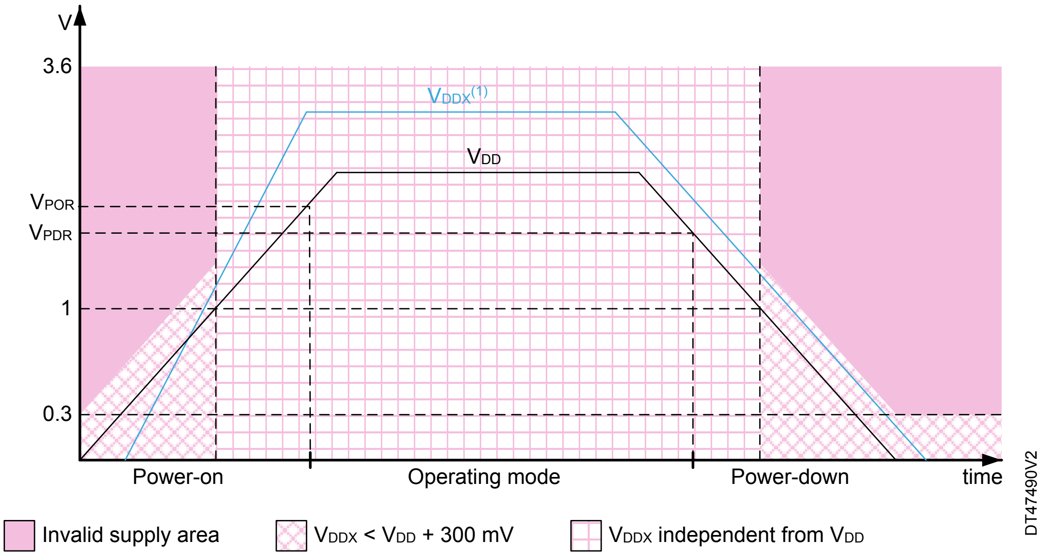
To avoid leakage currents between the available supplies and V_{DD} (or ground), V_{DD} must be provided first to the MCU, and then released with tolerance during power down (see Section 2.3.3).

2.3.2 General requirements

During power-up and power-down phases, the following power sequence requirements must be respected:

- When V_{DD} is below 1 V, other power supplies (V_{DDA}, V_{DDIO2}, and V_{DDUSB}) must remain below V_{DD} + 300 mV.
- When V_{DD} is above 1 V, all power supplies are independent.

Figure 11. **Power-up/power-down sequence**



(1) V_{DDX} refers to any power supply among V_{DDA}, V_{DDUSB}, and V_{DDIO2}.

Note: V_{BAT} is an independent supply and has no constraint versus V_{DD}. All power supply rails can be tied together.

2.3.3 Particular conditions during the power-down phase

During the power-down phase, V_{DD} can temporarily become lower than other supplies only if the energy provided to the MCU remains below 1 mJ. This allows external decoupling capacitors to be discharged with different time constants during the power-down transient phase (see Figure 11).

V_{DDX} (V_{DDA}, V_{DDIO2}, or V_{DDUSB}) power rails must be switched off before V_{DD}.

Note: During the power-down transient phase, V_{DDX} can remain temporarily above V_{DD} (see Figure 11).

Example of computation of the energy provided to the MCU during the power-down phase

If the sum of decoupling capacitors on V_{DDX} is 10 µF and V_{DD} drops below 1 V while V_{DDX} is still at 3.3 V, the energy remaining in the decoupling capacitors is:

$$E = \frac{1}{2} C \times V^2 = \frac{1}{2} \times 10^{-5} \times 3.3^2 = 0.05\, mJ$$

The energy remaining in the decoupling capacitors is below 1 mJ, so it is acceptable for the MCU to absorb it.

2.4 Reset and power-supply supervisor

2.4.1 Brownout reset (BOR)

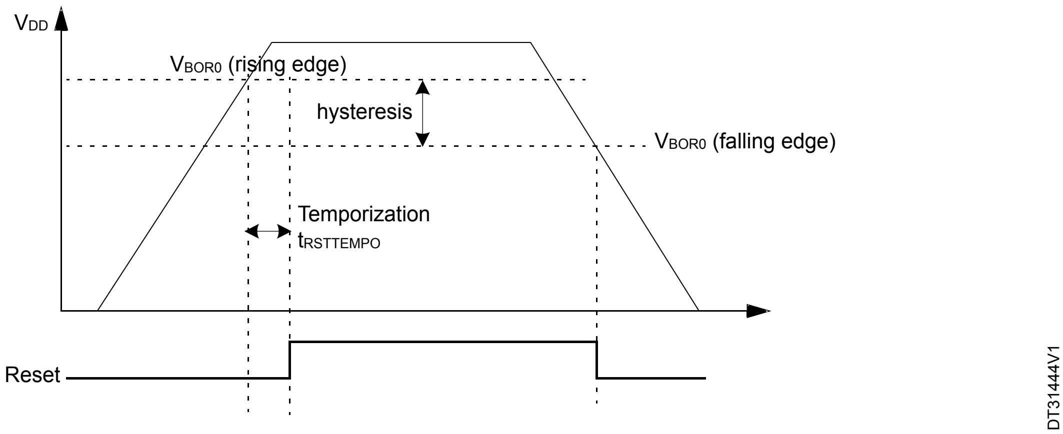
The devices have a brownout reset (BOR) circuitry. The BOR is active in all power modes except Shutdown mode, and cannot be disabled. The BOR monitors the backup domain supply voltage that is V_{DD} when present, V_{BAT} otherwise.

Five BOR thresholds can be selected through option bytes.

During power-on, the BOR keeps the device under reset until the supply voltage V_{DD} reaches the specified V_{BORx} threshold. When V_{DD} drops below the selected threshold, a device reset is generated. When V_{DD} is above the V_{BORx} upper limit, the device reset is released, and the system can start.

For more details on the brownout reset thresholds, refer to the electrical characteristics section in the datasheet.

Figure 12. Brownout reset waveform



Note: The reset temporization $t_{RSTTEMPO}$ is present only for the BOR lowest threshold (V_{BOR0}).

2.4.2 System reset

A system reset sets all registers to their reset values except the reset flags in RCC_CSR and the registers in the backup domain.

A system reset is generated when one of the following events occurs (refer to document [1] for more details):

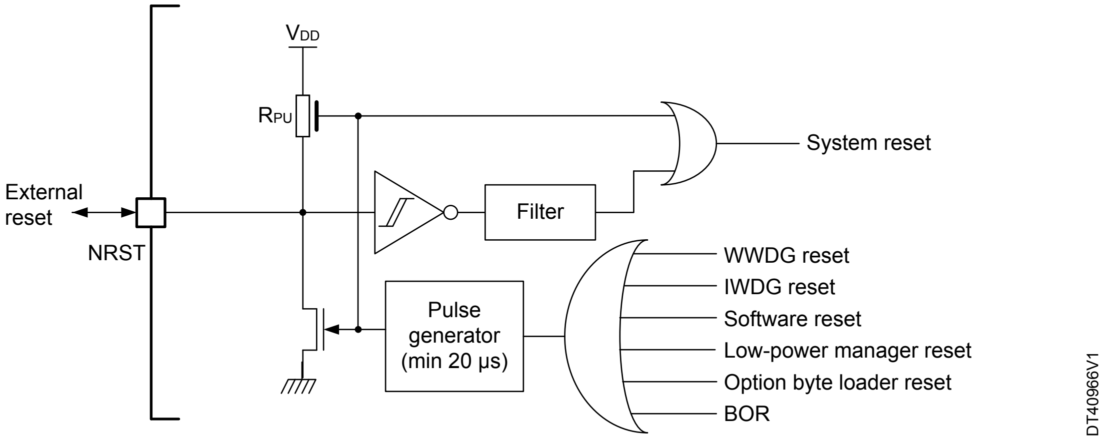
- a low level on the NRST pin (external reset)
- a window watchdog event (WWDG reset)
- an independent watchdog event (IWDG reset)
- a software reset
- a low-power mode security reset
- an option-byte loader reset
- a brownout reset

These sources act on the NRST pin that is always kept low during the delay phase. The reset service routine vector is selected via the boot option bytes.

The system reset signal provided to the device is output on the NRST pin. The pulse generator guarantees a minimum reset pulse duration of 20 µs for each internal reset source. In case of an external reset, the reset pulse is generated while the NRST pin is asserted low.

In case of an internal reset, the internal pull-up RPU is deactivated in order to save the power consumption through the pull-up resistor.

Figure 13. Simplified diagram of the reset circuit



2.4.3 Backup domain reset

A backup domain reset is generated when one of the following events occurs:

- a software reset, triggered by setting the BDRST bit in RCC_BDCR
- a V_{DD} or V_{BAT} power-on, if both supplies have previously been powered off

A backup domain reset only affects the LSE oscillator, RTC and TAMP, backup registers, the backup SRAM, and RCC_BDCR and PWR_BDCR1.

3 Packages

3.1 Package summary

The package selection must consider the constraints that are strongly dependent upon the application.

The list below summarizes the most frequent ones:

- Number of interfaces required: Some interfaces may not be available on some packages. Some interfaces combinations may not be possible on some packages.
- PCB technology constrains: Small pitch and high-ball density may require more PCB layers and higher-class PCB.
- Package height
- PCB available area
- Noise emission or signal integrity of high-speed interfaces
- Smaller packages usually provide better signal integrity. This is further enhanced as small-pitch and high-ball density requires multilayer PCBs that allow better supply/ground distribution.
- Compatibility with other devices

Table 1. Package summary for STM32U5 devices

Package	Size (mm)	Pitch (mm)	Height (mm)	STM32U535/ 545xx	STM32U575/ 585xx	STM32U59/ 5Axxx	STM32U5F/ 5Gxxx
LQFP48	7 × 7	0.5	1.6	X	X	-	-
UFQFPN48	7 × 7	0.5	0.6	X	X	-	-
LQFP64	10 × 10	0.5	1.6	X	X	X	-
UFBGA64	5 × 5	0.5	0.6	X	-	-	-
LQFP100	14 × 14	0.5	1.6	X	X	X	X
UFBGA100	7 × 7	0.5	0.6	X	-	-	-
UFBGA132	7 × 7	0.5	0.6	-	X	X	-
LQFP144	20 × 20	0.5	1.6	-	X	X	-
UFBGA169(1)	7 × 7	0.5	0.6	-	X	-	-
TFBGA169(1)	7 × 7	0.5	1.1	-	-	X	-
LQFP48 SMPS	7 × 7	0.5	1.6	X	X	-	-
UFQFPN48 SMPS	7 × 7	0.5	0.6	X	X	-	-
WLCSP56 SMPS	3.38 × 3.38	0.4	0.59	X	-	-	-
LQFP64 SMPS	10 × 10	0.5	1.6	X	X	X	-
UFBGA64 SMPS	5 × 5	0.5	0.6	X	-	-	-
WLCSP72 SMPS	3.38 × 3.38	0.35	0.58	X	-	-	-
WLCSP90 SMPS	4.20 × 3.95	0.40	0.59	-	X	-	-
LQFP100 SMPS	14 × 14	0.5	1.6	X	X	X	X
LQFP100 DSI SMPS	14 × 14	0.5	1.6	-	-	-	X
UFBGA100 SMPS	7 × 7	0.5	0.6	X	-	-	-
UFBGA132 SMPS	7 × 7	0.5	0.6	-	X	X	-
LQFP144 SMPS	20 × 20	0.5	1.6	-	X	X	-
LQFP144 DSI SMPS	20 × 20	0.5	1.6	-	-	-	X
UFBGA144 DSI SMPS	10 × 10	0.8	0.850	-	-	-	X
WLCSP150 SMPS	5.38 × 5.47	0.4	0.58	-	-	X	-
WLCSP150 DSI SMPS	5.38 × 5.47	0.4	0.58	-	-	X	-
UFBGA169 SMPS(1)	7 × 7	0.5	0.6	-	X	-	-
TFBGA169 SMPS(1)	7 × 7	0.5	1.1	-	-	X	-
WLCSP208 DSI SMPS	-(2)	0.35	0.58	-	-	X	X
TFBGA216 DSI SMPS	13 × 13	0.8	1.1	-	-	X	X

1. *For more information about the compatibility between UFBGA169 and TFBGA169, refer to Section 3.2.*
2. *Size in mm for STM32U59/5Axxx: 5.38 × 5.47*
   Size in mm for STM32U5F/5Gxxx: 5.8 × 5.6

3.2 Conversion from UFBGA169 to TFBGA169 boards

The UFBGA169 and TFBGA169 packages are compatible. However, it is important to note that the TFBGA169 balls have a larger diameter than the UFBGA169 balls, while the pitch of both packages is the same. To ensure compatibility between the two packages, STMicroelectronics recommends maintaining a 280 µm solder mask opening on the PCB. Additionally, customers must consider the height difference between the TFBGA169 and UFBGA169 packages when designing their application.

3.3 Pinout summary

Table 2. Pinout summary for STM32U5 devices

Pin name	LQFP48 UFQFPN48	LQFP64	UFBGA64	LQFP100	UFBGA100	UFBGA132	LQFP144	UFBGA169	TFBGA169	LQFP48 SMPS UFQFPN48 SMPS	WLCSP56 SMPS	LQFP64 SMPS	UFBGA64 SMPS	WLCSP72 SMPS	WLCSP90 SMPS	LQFP100 SMPS	LQFP100 DSI SMPS	UFBGA100 SMPS	UFBGA132 SMPS	LQFP144 SMPS	LQFP144 DSI SMPS	UFBGA144 DSI SMPS	WLCSP150 SMPS	WLCSP150 DSI SMPS	UFBGA169 SMPS	TFBGA169 SMPS	WLCSP208 DSI SMPS	TFBGA216 DSI SMPS
Specific I/Os																												
PC14-OSC32_IN	X[1]	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
PC15-OSC32_OUT	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
PH0-OSC_IN	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
PH1-OSC_OUT	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
System pins																												
NRST	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
PH3-BOOT0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Power pins																												
VBAT	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
VDDUSB[2]	o	X	X	X	X	X	X	X	X	o	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
VSSA[3]	o	o	o	X	X	o	X	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	X	X
VREF-	o	o	o	X	X	o	X	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	X	X
VREF+[4]	o	o	o	X	X	o	X	X	X	o	o	o	o	o	X	X	o	X	X	X	X	X	X	X	X	X	X	X
VDDA	o	o	X	X	X	o	X	X	X	o	o	o	o	o	X	X	X	X	X	X	X	X	X	X	X	X	X	X
VDDIO2	-[5]	-	-	-	-	X	X	X	X	-	-	-	-	X	X	-	-	-	X	X	-	-	X	X	X	X	X	X
VDD11	-	-	-	-	-	-	-	-	-	X	X	X	X	X	X	X	X	X	X	X	X	-	X	X	X	X	X	X
VDDSMPS	-	-	-	-	-	-	-	-	-	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Pin name	LQFP48 UFQFPN48	LQFP64	UFBGA64	LQFP100	UFBGA100	UFBGA132	LQFP144	UFBGA169	TFBGA169	LQFP48 SMPS UFQFPN48 SMPS	WLCSP56 SMPS	LQFP64 SMPS	UFBGA64 SMPS	WLCSP72 SMPS	WLCSP90 SMPS	LQFP100 SMPS	LQFP100 DSI SMPS	UFBGA100 SMPS	UFBGA132 SMPS	LQFP144 SMPS	LQFP144 DSI SMPS	UFBGA144 DSI SMPS	WLCSP150 SMPS	WLCSP150 DSI SMPS	UFBGA169 SMPS	TFBGA169 SMPS	WLCSP208 DSI SMPS	TFBGA216 DSI SMPS
VSSSMPS	-	-	-	-	-	-	-	-	-	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
VLXSMPS	-	-	-	-	-	-	-	-	-	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
VCAP	X	X	X	X	X	X	X	X	X	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
VDDDSI	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	X	-	-	-	X	X	-	X	-	-	X	X
VDD11DSI	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	X	-	-	-	X	X	-	X	-	-	X	X
VSSDSI	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	X	-	-	-	X	X	-	X	-	-	X	X
VDD11USB	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	X	-	-	X	X
Number of VDD	3	3	3	5	5	6	9	10	10	3	3	3	4	4	4	5	9	5	6	9	10	8	9	9	10	10	17	10
Number of VSS	3	4	4	5	5	6	11	11	11	3	4	3	3	6	4	5	7	6	6	11	10	12	12	10	11	11	19	20

1. *'X' means that the pin is present.*
2. *'o' means that VDD and VDDUSB are internally connected and available on a single pin.*
3. *'o' means that VSSA and VREF- are internally connected and available on a single pin.*
4. *'o' means that VDDA and VREF+ are internally connected and available on a single pin.*
5. *'-' means that the pin is absent.*

Caution: Packages with and without SMPS are not compatible, in almost all power supply pins of Table 2.

Example: VDDIO2 is the pin number 130 on SMPS package. Pin 130 on the package without SMPS is mapped to a VSS pin. It means that the system is short-circuited when a legacy package is mounted on an SMPS socket.

4 Clocks

The following clock sources can be used to drive the system clock (SYSCLK):
- HSI16: high-speed internal 16 MHz RC oscillator clock
- MSIS: multi-speed internal RC oscillator clock
- HSE: high-speed external crystal or clock, from 4 to 50 MHz
- PLL1 clock

The MSIS is used as system clock source after startup from reset, configured at 4 MHz.

The devices have the following additional clock sources:
- MSIK: multi-speed internal RC oscillator clock used for peripherals kernel clocks
- LSI: 32 kHz low-speed internal RC that drives the independent watchdog and optionally the RTC used for auto-wakeup from Stop and Standby modes
- LSE: 32.768 kHz low-speed external crystal or clock that optionally drives the real-time clock (rtc_ck)
- HSI48: internal 48 MHz RC that potentially drives the OTG FS, the SDMMC and the RNG
- SHSI: secure high-speed internal RC that drives the secure AES (SAES).
- PLL2 and PLL3 clocks

Each clock source can be switched on or off independently when it is not used, to optimize power consumption.

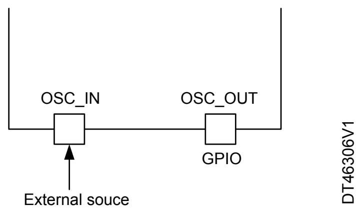
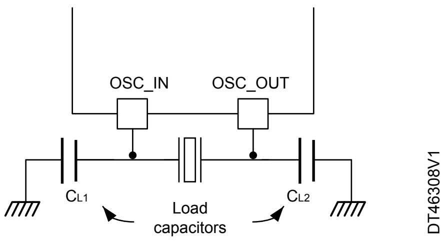
Several pre-scalers can be used to configure the AHB and the APB frequencies domains with a maximum frequency of 160 MHz.

4.1 HSE clock

The high-speed external clock signal (HSE) can be generated from the following clock sources:
- HSE external crystal/ceramic resonator
- HSE user external clock that feeds OSC_IN pin

The resonator and the load capacitors must be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. The loading capacitance values must be adjusted according to the selected oscillator.

Table 3. HSE/LSE clock sources

Clock source	Hardware configuration
External clock	
Crystal/ceramic resonators	 CL1 and CL2 values depend on the quartz. Refer to document [3] for more details.

4.1.1 External crystal/ceramic resonator (HSE crystal)

The 4 to 50 MHz external oscillator has the advantage of producing a very accurate rate on the main clock. The associated hardware configuration is shown in Table 3. Refer to the electrical characteristics section of the datasheet for more details.

4.1.2 External source (HSE bypass)

In this mode, an external clock source must be provided, with a frequency up to 50 MHz. The external clock signal (square, sinus or triangle) with ~40 to 60 % duty cycle depending on the frequency (refer to the datasheet), must drive the OSC_IN pin while the OSC_OUT pin can be used as a GPIO (see Table 3).

Note: *For details on pin availability, refer to the pinout section of the datasheet. To minimize the consumption, the square signal is recommended.*

4.2 HSI16 clock

The HSI16 clock signal is generated from an internal 16 MHz RC oscillator. The HSI16 RC oscillator provides a clock source at low cost (no external components). It also has a faster startup time than the HSE crystal oscillator. However, even with calibration, the frequency is less accurate than an external crystal oscillator or ceramic resonator.

The HSI16 clock can be used as a backup clock source (auxiliary clock) if the HSE crystal oscillator fails.

For more details, refer to section *Clock security system (CSS)* in document [1].

4.3 MSI (MSIS and MSIK) clocks

The MSI is made of four internal RC oscillators: MSIRC0 (48 MHz), MSIRC1 (4 MHz), MSIRC2 (3.072 MHz), and MSIRC3 (400 kHz). Each oscillator feeds a prescaler providing a division by 1, 2, 3 or 4.

Two output clocks are generated from these divided oscillators:

- MSIS that can be selected as system clock
- MSIK that can be selected by some peripherals as kernel clock

MSIS and MSIK frequency range can be adjusted by software, by using respectively the MSISRANGE [3:0] and MSIKRANGE [3:0] fields in RCC_ICSCR1, with MSIRGSEL = 1. Sixteen frequency ranges are available, generated from the four internal RCs (refer to document [1] for more details).

The MSI clock can also be used as a backup clock source (auxiliary clock) if the HSE crystal oscillator fails (refer to section Clock security system (CSS) in document [1]).

The MSI oscillator provides a low-cost (no external components) low-power clock source. In addition, when the MSI is used in PLL-mode with the LSE, it provides a very accurate clock source that can be used by the USB OTG_FS peripheral, and feeds the PLL to run the system at the maximum speed 160 MHz.

Hardware auto calibration with LSE (PLL-mode)

When a 32.768 kHz external oscillator is present in the application, either MSIS or MSIK can be configured in a PLL-mode. This mode is enabled as follows:

- for MSIS: by setting the MSIPLLEN bit to 1 in RCC_CR
- for MSIK: by setting the MSIPLLEN bit to 0 in RCC_CR

In case MSIS and MSIK ranges are generated from the same MSIRC source, the PLL-mode is applied on both MSIS and MSIK. When configured in PLL-mode, the MSIS or MSIK automatically calibrates itself thanks to the LSE. This mode is available for all MSI frequency ranges. At 48 MHz, the MSIK in PLL-mode can be used for the USB OTG_FS peripheral, avoiding the need of an external high-speed crystal.

For more details on how to measure the MSI frequency variation, refer to section Internal/external clock measurement with TIM15/TIM16/TIM17 in document [1].

Note: *On STM32U5Ax/59x/5Fx/5Gx, the OTG_HS peripheral cannot be clocked by the MSI in PLL-mode. The HSE crystal must be used.*

4.4 LSE clock

The LSE crystal is a 32.768 kHz low-speed external crystal or ceramic resonator (see Table 3). It provides a low-power but highly accurate clock source to the RTC (real-time clock) peripheral for clock/calendar or other timing functions.

The crystal oscillator driving strength can be changed at runtime using the LSEDRV[1:0] bits in RCC_BDCR, to obtain the best compromise between robustness and short startup time on one side, and low-power-consumption on the other side.

External source (LSE bypass)

In this mode, an external clock source must be provided, with a frequency up to 1 MHz. The external clock signal (square, sinus, or triangle) with ~50 % duty cycle, must drive the OSC32_IN pin while the OSC32_OUT pin can be used as GPIO (see Table 3).

5 Boot configuration

5.1 Boot mode selection

At startup, a BOOT0 pin, nBOOT0, and NSBOOTADDx[24:0]/SECBOOTADD0[24:0] option bytes are used to select the boot memory address that includes:

- Boot from any address in user flash memory
- Boot from system memory (bootloader)
- Boot from any address in embedded SRAM
- Boot from root security service (RSS)

The BOOT0 value may come from the PH3-BOOT0 pin or from an option bit depending on the value of a user option bit to free the GPIO pad if needed.

When TrustZone® is disabled by resetting TZEN option bit (TZEN = 0), the boot space is as detailed in the table below.

Table 4. **Boot modes when TrustZone® is disabled (TZEN = 0)**

nBOOT0 FLASH_ OPTR[27]	BOOT0 pin PH3	nSWBOOT0 FLASH_ OPTR[26]	Boot address option-byte selection	Boot area	ST programmed default value
-	0	1	NSBOOTADD0[24:0]	Boot address defined by user option bytes NSBOOTADD0[24:0]	Flash: 0x0800 0000
-	1	1	NSBOOTADD1[24:0]	Boot address defined by user option bytes NSBOOTADD1[24:0]	Bootloader: 0x0BF9 0000
1	-	0	NSBOOTADD0[24:0]	Boot address defined by user option bytes NSBOOTADD0[24:0]	Flash: 0x0800 0000
0	-	0	NSBOOTADD1[24:0]	Boot address defined by user option bytes NSBOOTADD1[24:0]	Bootloader: 0x0BF9 0000

When TrustZone® is enabled by setting the TZEN option bit (TZEN = 1), the boot space must be in a secure area. The SECBOOTADD0[24:0] option bytes are used to select the boot secure memory address. A unique boot entry option can be selected by setting the BOOT_LOCK option bit. All other boot options are ignored.

The table below details the boot modes when the TrustZone® is enabled.

Table 5. **Boot modes when TrustZone® is enabled (TZEN = 1)**

BOOT_ LOCK	nBOOT0 FLASH_ OPTR[27]	BOOT0 pin PH3	nSWBOOT0 FLASH_ OPTR[26]	RSS command	Boot address option-byte selection	Boot area	ST programmed default value
0	-	0	1	0	SECBOOTADD0[24:0]	Secure boot address defined by user option bytes SECBOOTADD0[24:0]	Flash: 0x0C00 0000
	-	1	1	0	N/A	RSS	RSS: 0x0FF8 0000
	1	-	0	0	SECBOOTADD0[24:0]	Secure boot address defined by user option bytes SECBOOTADD0[24:0]	Flash: 0x0C00 0000
	0	-	0	0	N/A	RSS	RSS: 0x0FF8 0000
	-	-	-	≠ 0	N/A	RSS	RSS: 0x0FF8 0000
1	-	-	-	-	SECBOOTADD0[24:0]	Secure boot address defined by user option bytes SECBOOTADD0[24:0]	Flash: 0x0C00 0000

5.2 Embedded bootloader and RSS

The embedded bootloader is located in the system memory and programmed by ST during production. It is used to reprogram the flash memory by using the following serial interfaces:

- **USART**: USART1 on pins PA9/PA10, USART2 on pins PA2/PA3, USART3 on pins PC10/PC11
- **I2C**: I2C1 on pins PB6/PB7, I2C2 on pins PB10/PB11, I2C3 on pins PC0/PC1
- **SPI**: SPI1 on pins PA4/PA5/PA6/PA7, SPI2 on pins PB12/PB13/PB14/PB15, SPI3 on pins PB5/PG9/PG10/PG12
- **FDCAN**: FDCAN1 on pins PB8/PB9
- **USB** in device mode through the DFU (device firmware upgrade) interface, on pins PA11/PA12

For further details on the STM32 bootloader, refer to document [2].

The RSS (root secure services) are embedded in a flash memory area named secure information block, programmed during ST production.

The RSS enable, for example, the SFI (secure firmware installation) using the RSS extension firmware (RSSe SFI). This feature allows the customers to protect the confidentiality of the firmware to be provisioned into the STM32 device when the production is subcontracted to a third party. Refer to document [4].

The RSS are available on all devices, after enabling the TrustZone® through the TZEN option bit.

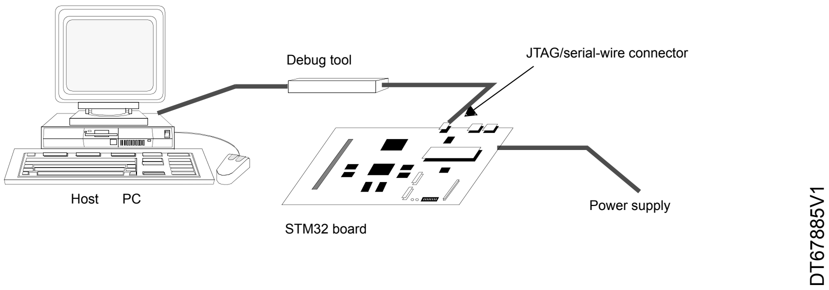
6 Debug management

The serial wire/JTAG debug port (SWJ-DP) is an Arm® standard CoreSight™ debug port.

The host/target interface is the hardware equipment that connects the host to the application board. This interface is made of three components: a hardware debug tool, a serial-wire connector, and a cable connecting the host to the debug tool.

The figure below shows the connection of the host to a development board.

Figure 14. Host-to-board connection



The Nucleo demonstration board embeds the debug tools (STLINK), so it can be directly connected to the PC through a USB cable.

6.1 SWJ-DP (serial-wire and JTAG debug port)

The SWJ-DP combines:

- a JTAG-DP that provides a 5-pin standard JTAG interface to the AHP-AP port
- an SW-DP that provides a 2-pin (clock + data) interface to the AHP-AP port

In the SWJ-DP, the two JTAG pins of the SW-DP are multiplexed with some of the five JTAG pins of the JTAG-DP.

Note: The software can configure all SWJ-DP port I/Os to other functions, but debugging is no longer possible.

6.2 Pinout and debug port pins

The devices are offered in various packages with different numbers of available pins. As a result, some functionality related to the pin availability may differ from one package to another.

6.2.1 SWJ-DP pins

Five pins are used as outputs for the SWJ-DP, as alternate functions of the GPIOs (general-purpose I/Os). These pins, detailed in the table below, are available on all packages.

Table 6. Debug port pin assignment

SWJ-DP pin	JTAG debug port		SW debug port		Pin assignment
	Type	Description	Type	Debug assignment	
JTMS/SWDIO	Input	JTAG test mode selection	Input/Output	Serial-wire data input/output	PA13
JTCK/SWCLK	Input	JTAG test clock	Input	Serial-wire clock	PA14
JTDI	Input	JTAG test data input	-	-	PA15
JTDO/TRACESWO	Output	JTAG test data output	-	TRACESWO if asynchronous trace is enabled	PB3
JNTRST	Input	JTAG test nReset	-	-	PB4

6.2.2 Flexible SWJ-DP pin assignment

After reset (SYSRESETn or PORESETn), all five pins used for the SWJ-DP are assigned as dedicated pins that are immediately usable by the debugger host.

Note: *The trace outputs are not assigned except if explicitly programmed by the debugger host.*

The table below shows the different possibilities for releasing some pins (refer to document [1] for more details).

Table 7. SWJ-DP I/O pin availability

<table>
<tr><th rowspan="2">Available debug ports</th><th colspan="5">SWJ-DP I/O pin assigned</th></tr>
<tr><th>PA13 / JTMS/ SWDIO</th><th>PA14 / JTCK/ SWCLK</th><th>PA15 / JTDI</th><th>PB3 / JTDO</th><th>PB4/ JNTRST</th></tr>
<tr><td>Full SWJ-DP (JTAG-DP + SW-DP)
Reset state</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td></tr>
<tr><td>Full SWJ-DP (JTAG-DP + SW-DP) but without JNTRST</td><td>X</td><td>X</td><td>X</td><td>X</td><td rowspan="3">-</td></tr>
<tr><td>JTAG-DP disabled and SW-DP enabled</td><td>X</td><td>X</td><td colspan="2">-</td></tr>
<tr><td>JTAG-DP disabled and SW-DP disabled</td><td colspan="4">Released</td></tr>
</table>

6.2.3 Internal pull-up and pull-down resistors on JTAG pins

The JTAG input pins must not be floating since they are directly connected to flip-flops that control the debug mode features. Special care must be taken with the SWCLK/TCK pin that is directly connected to the clock of some of these flip-flops.

To avoid any uncontrolled I/O levels, the devices embed the following internal resistors on the JTAG input pins:

- JNTRST: internal pull-up
- JTDI: internal pull-up
- JTMS/SWDIO: internal pull-up
- TCK/SWCLK: internal pull-down

Once the user software releases the JTAG I/O, the GPIO controller takes the control again, and the software can then use these I/Os as standard GPIOs. The reset states of the GPIO control registers put the I/Os in the following equivalent states:

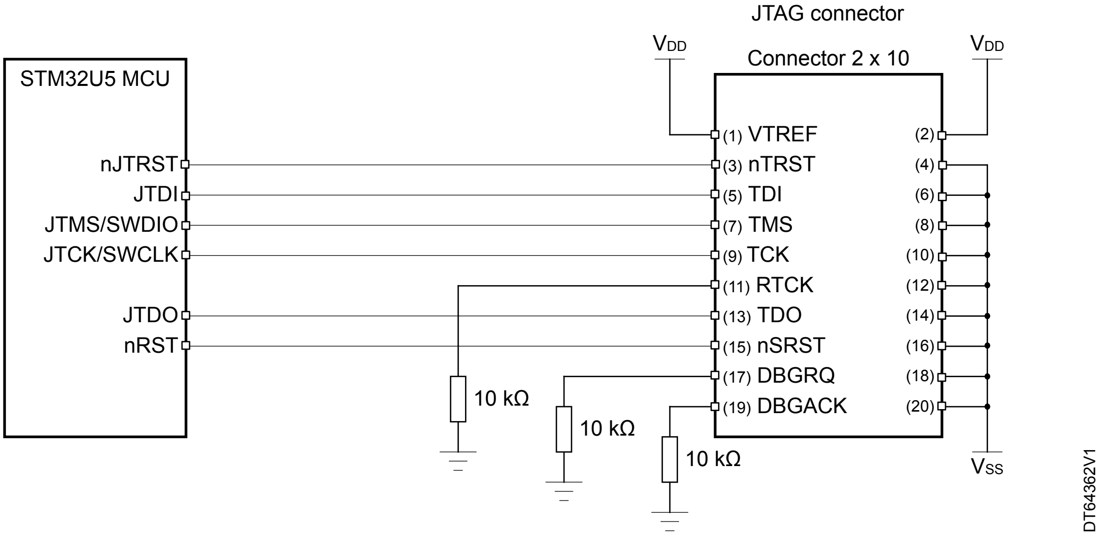
- JNTRST: input pull-up
- JTDI: input pull-up
- JTMS/SWDIO: input pull-up
- JTCK/SWCLK: input pull-down
- JTDO: input floating

Note: *The JTAG IEEE standard recommends adding pull-up resistors on TDI, TMS, and nTRST, but there is no special recommendation for TCK. However, for the devices, an integrated pull-down resistor is used for JTCK. Having embedded pull-up and pull-down resistors removes the need to add external resistors.*

6.2.4 SWJ-DP connection with standard JTAG connector

The figure below shows the connection between the device and a standard JTAG connector.

Figure 15. JTAG connector implementation



6.3 Serial-wire debug (SWD) pin assignment

The same SWD pin assignment, detailed in the table below, is available on all packages.

Table 8. SWD port pins

SWD pin	SWD port		Pin assignment
	Type	Debug assignment	
SWDIO	Input/Output	Serial-wire data input/output	PA13
SWCLK	Input	Serial-wire clock	PA14

After reset, the pins used for the SWD are assigned as dedicated pins that can be immediately used by the debugger host.

However, the MCU offers the possibility to disable the SWD, therefore releasing the associated pins for GPIO use.

For more details on how to disable SWD port, refer to section *I/O pin alternate function multiplexer and mapping* of document .

6.3.1 Internal pull-up and pull-down on SWD pins

Once the user software releases the SWD I/O, the GPIO controller takes control of it. The reset states of the GPIO control registers put the I/Os in the equivalent states:

- SWDIO: alternate function pull-up
- SWCLK: alternate function pull-down

Having embedded pull-up and pull-down resistors removes the need to add external resistors.

6.3.2 SWD port connection with standard SWD connector

The figure below shows the connection between the device and a standard SWD connector.

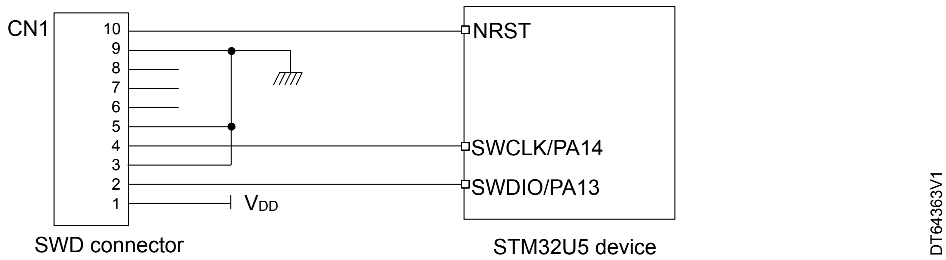


Figure 16. SWD connector implementation

7 Recommendations

7.1 PCB (printed circuit board)

For technical reasons, it is best to use a multilayer PCB, with a separate layer dedicated to ground (V_{SS}) and another dedicated to the V_{DD} supply.

This provides a good decoupling and a good shielding effect. For many applications, economical reasons prohibit the use of this type of board. In this case, the major requirement is to ensure a good structure for ground and power supply.

7.2 Component position

A preliminary layout of the PCB must separate circuits into different blocks:

- high-current circuits
- low-voltage circuits
- digital component circuits
- circuits separated according to their EMI contribution, in order to reduce noise due to cross-coupling on the PCB

7.3 Ground and power supply

The following rules related to grounding must be respected:

- Ground every block (noisy, low-level sensitive, digital, or others) individually.
- Return all grounds to a single point.
- Avoid loops (or ensure they have a minimum area).

In order to improve analog performance, the user must use separate supply sources for V_{DD} and V_{DDA}, and place the decoupling capacitors as close as possible to the device.

The power supplies (V_{SS}, V_{DD}, V_{SSA}, V_{DDA}, V_{DDUSB}, V_{DDIO2}, V_{DDDSI}, or V_{DDSMPS}) must be implemented close to the ground line to minimize the area of the supplies loop. This is because the supply loop acts as an antenna, and acts as the main transmitter and receiver of EMI. All component-free PCB areas must be filled with additional grounding to create a kind of shielding (especially when using single-layer PCBs).

7.4 Decoupling

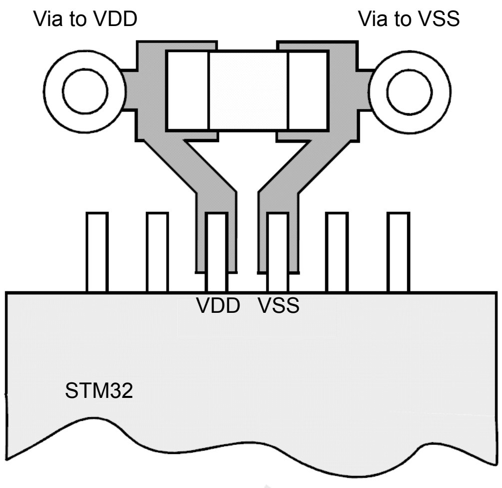
All power-supply and ground pins must be properly connected to the power supplies. These connections (including pads, tracks, and vias) must have the lowest possible impedance. This is typically achieved with thick track widths and, preferably, the use of dedicated power-supply planes in multilayer PCBs.

In addition, each power supply pair must be decoupled with filtering ceramic capacitors (100 nF) and a tantalum or ceramic capacitor of about 10 µF, connected in parallel on the device.

Some packages use a common VSS pin for several VDD pins, instead of a pair of power pins (one VSS for each VDD). In that case, the capacitors must be between each VDD pin and the common VSS pin. These capacitors must be placed as close as possible to, or below the appropriate pins on the underside of the PCB. Typical values are 10 to 100 nF, but exact values depend on the application needs.

The figure below shows the typical layout of such a VDD/VSS pin pair.

Figure 17. Typical layout for VDD/VSS pin pair



7.5 Other signals

When designing an application, the EMC performance can be improved by closely studying the following:

- Signals for which a temporary disturbance affects the running process permanently (it is the case for interrupts and handshaking strobe signals but not the case for LED commands)
  For these signals, a surrounding ground trace, shorter lengths, and the absence of noisy and sensitive traces nearby (crosstalk effect) improve EMC performance.
  For digital signals, the best possible electrical margin must be reached for the two logical states. Slow Schmitt triggers are recommended to eliminate parasitic states.
- Noisy signals (example: clock)
- Sensitive signals (example: high impedance)

7.6 Unused I/Os and features

All microcontrollers are designed for a variety of applications and often a particular application does not use 100 % of the MCU resources.

To increase the EMC performance and avoid extra power consumption, the unused features of the device must be disabled and disconnected from the clock tree, as follows:

- The unused clock source must be disabled.
- The unused I/Os must not be left floating.
- The unused I/O pins must be configured as analog input by software, and must be connected to a fixed logic level 0 or 1 by an external or internal pull-up or pull-down, or configured as output mode using software.

8 Reference design

8.1 Description

The reference designs shown in the next sections are based on STM32U5 devices in LQFP144 and TFBGA216 packages. This reference design can be tailored to any STM32U5 device with a different package, using the pin correspondence given in Section 8.2 and Design reference for a STM32U599/5A9/5F9/5G9 device (with SMPS).

Clock

Two clock sources are used for the MCU (see Section 4 for more details):

- LSE: X1 – 32.768 kHz crystal for the embedded RTC
- HSE: X2 – 16 MHz crystal for the MCU

See Section 4 for more details.

Reset

The reset signal is active low in the reference design figures shown in Section 8.2.

The reset sources include:

- the reset button (B1)
- debugging tools via the connector CN1

See Section 2.4 for more details.

Boot mode

The user can add a switch on the board to change the boot option.

See Section 5 for more details.

Note: When waking up from Standby mode, the BOOT pin is sampled and the user must pay attention to its value.

SWD interface

The reference design shows the connection between the STM32U575/585 device and a standard SWD connector.

See Section 6 for more details.

Note: To allow tools to reset the applications, the RESET pins must be connected.

Power supply

See Section 2 for more details.

8.2 Design reference for a STM32U5 device (with and without SMPS)

Table 9 lists the components used for a STM32U5 design reference :
- based on STM32U535/545/575/585xxxxQ device, with SMPS (see Figure 18)
- based on a STM32U5xxx device, without SMPS (see Figure 19)

Table 9. Components of STM32U5 device design reference

Reference	Type	Value	Quantity	Comments
B1	Push-button	-	1	-
C1, C4, C6	Ceramic capacitor	1 µF	3	Decoupling capacitors C6 used for the internal VREFBUF
C2, C16	Tantalum or ceramic capacitor	10 µF	2	Decoupling capacitors required for the package
C3 (x5), C5, C7, C8, C13, C17	Ceramic capacitor	100 nF	10	For each external power pin
C15	Tantalum or ceramic capacitor	4.7 µF	1	Decoupling capacitor
C18, C19		2.2 µF	2	Required on each VDD11 pin of packages with SMPS
C11, C12		3.9 µF		Used for LSE: the value depends on the crystal characteristics (refer to document [3])
C9, C10		6.8 pF		
L1	Coil	2.2 µH	1	Required for SMPS packages on VLXSMPS pin
X1	Quartz	32.768 kHz	1	Used for LSE
X2		16 MHz	1	Used for HSE
R1	Resistor	10 KΩ	1	R1 maintains PH3-BOOT0 pin at a logic low or high level
R2, R3, R4			3	Used for the ST-LINK interface
SW1	Switch	-	1	Used to select the right boot mode
U1, U2, U3	ESD protection 6V1	-	3	Used for ESD protection
R5, R6, R7, R8, R9	-	47 Ω	5	
P1	ST LINK V2 connector	-	1	Used to connect an external ST-LINK

Figure 18. STM32U535/545/575/585xxxxQ reference design (with SMPS)

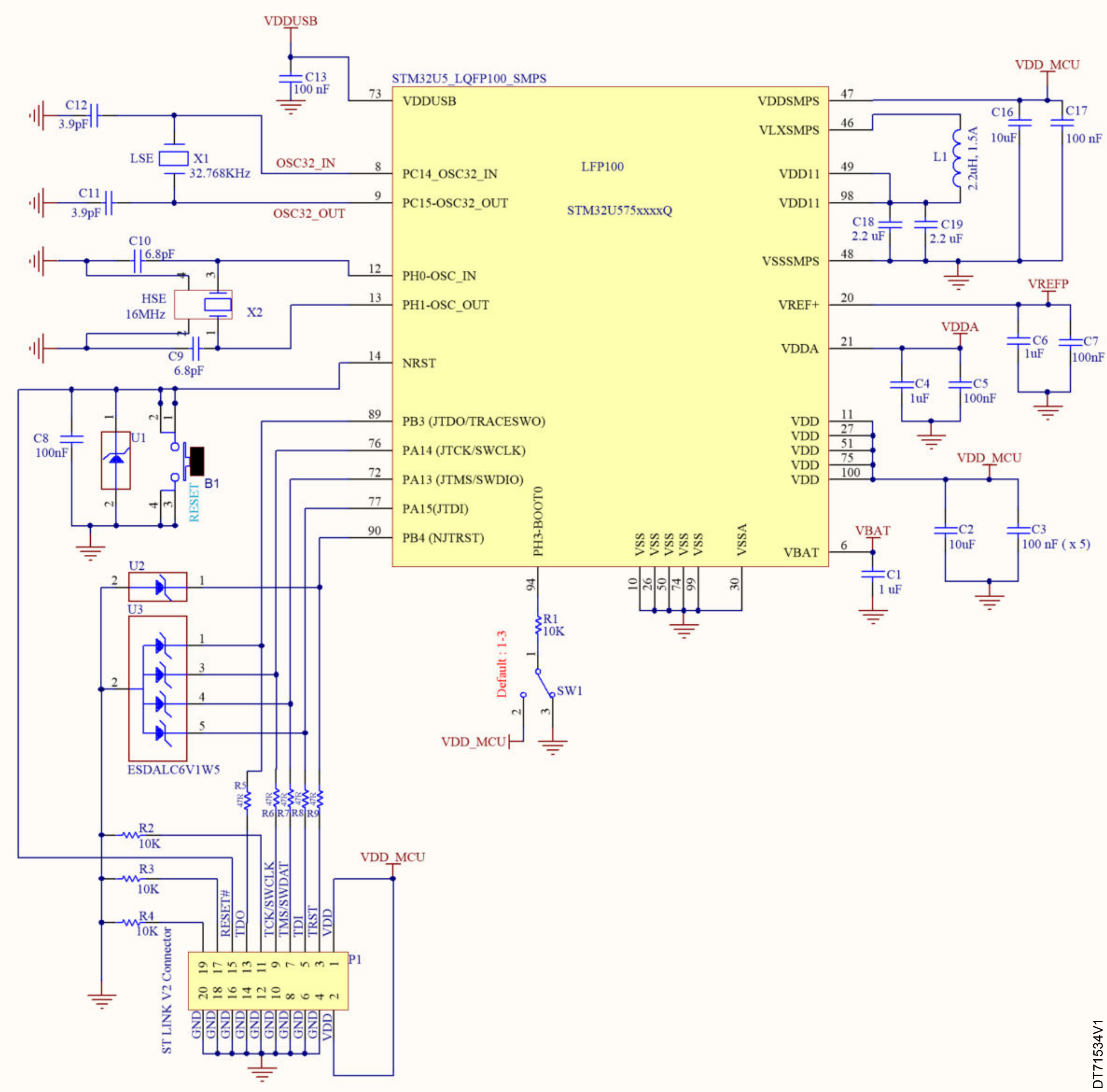


Figure 19. STM32U5xxx reference design (without SMPS)

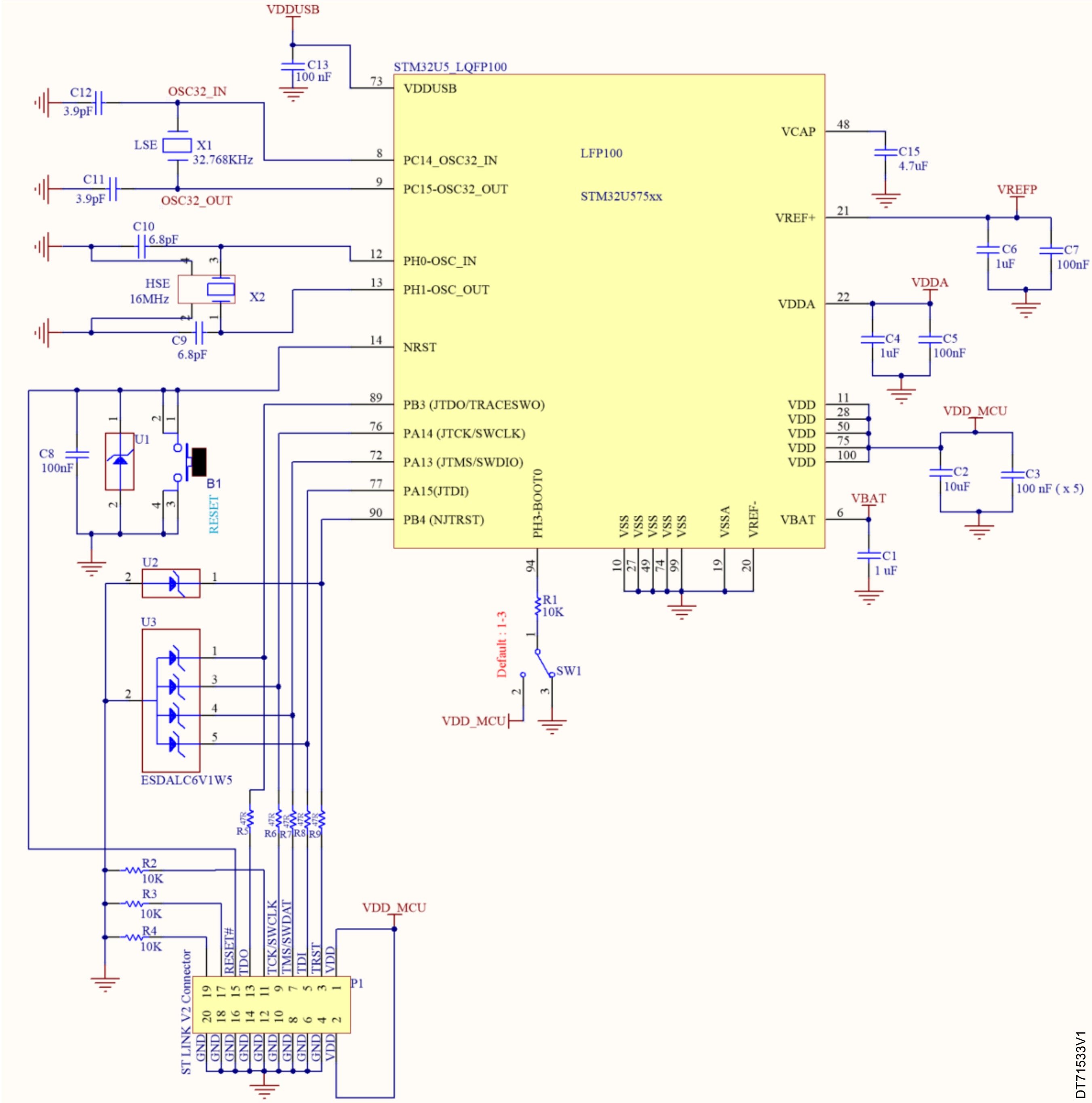
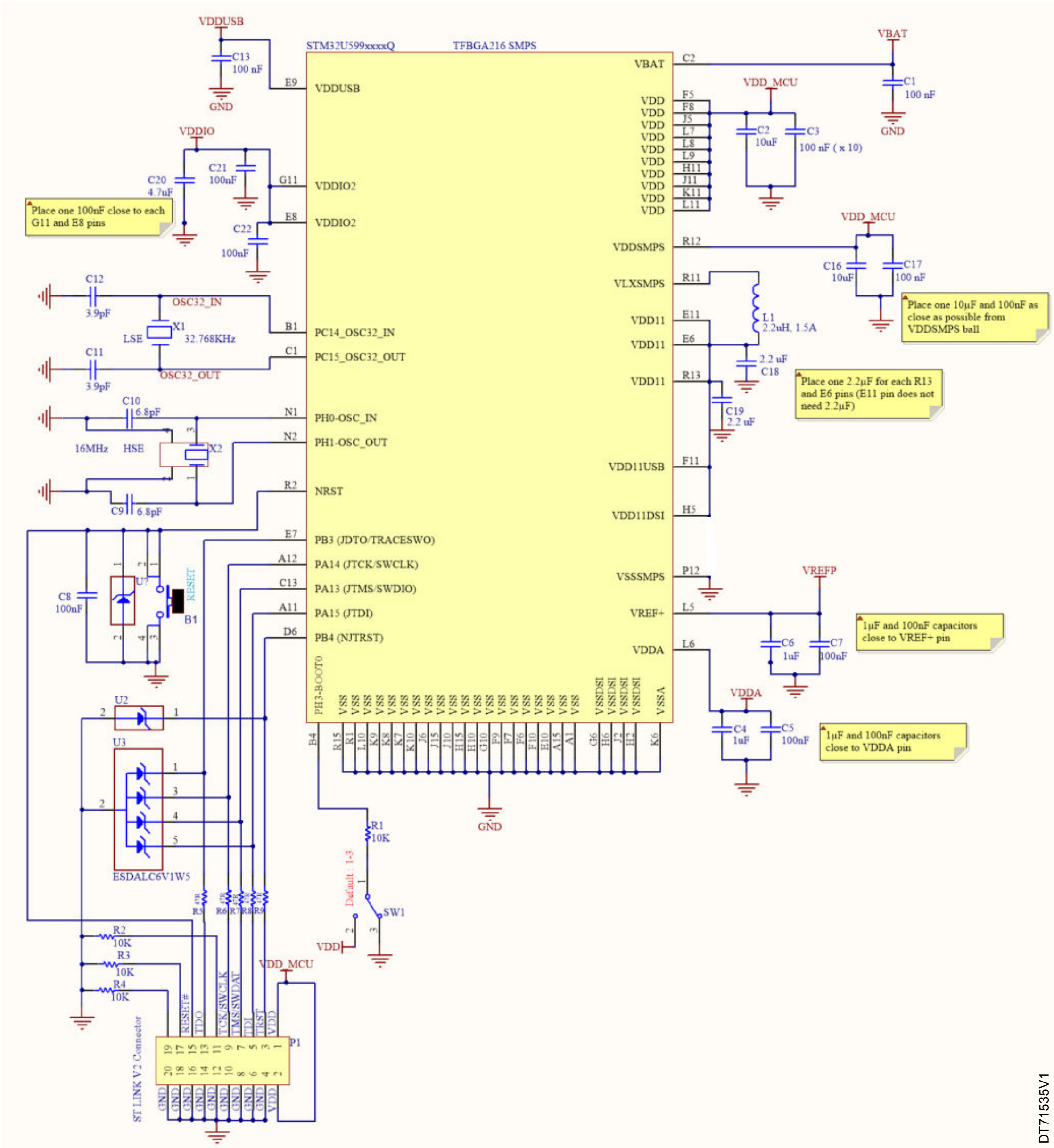


Table 10 lists the components in the STM32U599 discovery kit STM32U599J-DK (reference design MB1662) based on STM32U599xxxxQ device, with SMPS (see Figure 20).

Table 10. Components of STM32U599 discovery kit

Reference	Type	Value	Quantity	Comments
B1	Push-button	-	1	-
C4, C6	Ceramic capacitor	1 µF	2	Decoupling capacitors C6 used for the internal VREFBUF
C2, C16	Tantalum or ceramic capacitor	10 µF	2	Decoupling capacitors required for the package
C1, C3 (x10), C5, C7, C8, C13, C17, C21, C22, C23	Ceramic capacitor	100 nF	19	For each external power pin
C20	Tantalum or ceramic capacitor	4.7 µF	1	Decoupling capacitor
C18, C19		2.2 µF	2	Required on each VDD11 pin of packages with SMPS
C11, C12		3.9 pF	2	Used for LSE: the value depends on the crystal characteristics (refer to document [3])
C9, C10		6.8 pF	2	
L1	Coil	2.2 µH	1	Required for SMPS packages on VLXSMPS pin
X1	Quartz	32.768 kHz	1	Used for LSE
X2		16 MHz	1	Used for HSE
R1	Resistor	10 KΩ	1	R1 maintains PH3-BOOT0 pin at a logic low or high level
R2, R3, R4			3	Used for the ST-LINK interface
SW1	Switch	-	1	Used to select the right boot mode
U1, U2, U3	ESD protection 6V1	-	3	Used for ESD protection
R5, R6, R7, R8, R9	-	47 Ω	5	
P1	ST LINK V2 connector	-	1	Used to connect an external ST-LINK

Figure 20. STM32U59/5A/5F/5GxxxxxQ reference design (with SMPS)



Revision history

Table 11. Document revision history

Date	Version	Changes
21-Jun-2021	1	Initial release.
03-Jan-2022	2	Updated: • Section 2 Power supply management • Section 8.2 Component references
14-Nov-2022	3	Updated various typos and Section 8.2 Component references
16-Feb-2023	4	Document updated to cover entire STM32U5 series microcontrollers
12-Apr-2023	5	Updated: • Voltage range values for V_{DDDSI} and $V_{DD11DSI}$ in Section 2.1 Power supplies • Figure 1. STM32U535xxxxQ and STM32U545xxxxQ power supply overview (with SMPS) • Figure 2. STM32U535xx and STM32U545xx power supply overview (without SMPS) • Figure 3. STM32U575xQ and STM32U585xQ power supply overview (with SMPS) • Figure 4. STM32U575xx and STM32U585xx power supply overview (without SMPS) • Figure 5. STM32U5F/5G/59/5AxxxxxQ power supply overview (with SMPS) • Figure 6. STM32U5F/5G/59/5Axxx power supply overview (without SMPS)
01-Sep-2023	6	Updated: • Note added for V_{LXSMPS} in Section 2.1 Power supplies • Table 1. Package summary for STM32U5 devices • Section 8.1 Description • Table 9. Components of STM32U5 device design reference • Table 10. Components of STM32U599 discovery kit Added Section 3.2 Conversion from UFBGA169 to TFBGA169 boards
24-Nov-2023	7	Updated R1 description in Table 9. Components of STM32U5 device design reference and Table 10. Components of STM32U599 discovery kit

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