Materials Science Forum
ISSN: 1662-9752, Vol. 924, pp 124-127
doi:10.4028/www.scientific.net/MSF.924.124

Submitted: 2017-09-01
Revised: 2018-01-13
Accepted: 2018-01-17
Online: 2018-06-05

Stacking Faults Defects on 3C-SiC Homo-Epitaxial Films

Grazia Litrico[1,a*], Ruggero Anzalone[2,b], Alessandra Alberti[3,c], Corrado Bongiorno[3,d], Giuseppe Nicotra[3,e], Massimo Zimbone[3,f], Marco Mauceri[4,g], Salvatore Coffa[2,h], Francesco La Via[3,i]

[1]Laboratori Nazionali del Sud, via S. Sofia, 62, 95123 Catania, Italy

[2]STMicroelectronics, Stradale Primosole, 50, 95121 Catania, Italy

[3]IMM-CNR, VIII Strada, 5, 95121 Catania, Italy

[4]LPE, XVI Strada, 95121, Catania, Italy

[a]grazia.litrico@lns.infn.it, [b]ruggero.anzalone@st.com, [c]alessandra.alberti@imm.cnr.it, [d]corrado.bongiorno@imm.cnr.it, [e]giuseppe.nicotra@imm.cnr.it, [f]massimo.zimbone@imm.cnr.it, [g]marco.mauceri@lpe-epi.com, [h]salvo.coffa@st.com, [i]francesco.lavia@imm.cnr.it

Keywords: 3C-SiC, Stacking Faults, HR-XRD, STEM, homo-epitaxy, growth rate

Abstract. Stacking Faults (SFs) are the main defect of 3C-SiC material and in this work a detailed study of this typology of defect is presented. We studied the behavior of SFs with High Resolution XRD and STEM analysis. The homo-epitaxial growth was proposed as a solution for the reduction of SFs density in 3C-SiC material and the influence of the growth condition on the SFs density was studied. The knowledge of the mechanism of SFs reduction is crucial for the development of a high quality material for devices fabrication.

Introduction

Cubic Silicon Carbide (3C-SiC) is considered a very promising candidate for high power and high frequency devices, since 3C-SiC allows a high speed of electron transport within the crystal [1]. The growth of thick 3C-SiC layers can be extremely interesting for the realization of power devices in the region below a breakdown voltage of 800 V, where DC-DC converter and DC-AC inverter should be realized for electric vehicles or hybrid cars. For these applications, 3C-SiC is the ideal material for its high channel mobility with almost the same characteristics of the hexagonal polytypes [2].

Currently the main limitation for devices fabrication on 3C-SiC comes from the quality of such material. 3C–SiC can be grown on large diameter Si (silicon) substrates but the hetero-epitaxial growth is affected by intrinsic problems as the mismatch in the lattice parameters and/or the thermal expansion coefficients between two dissimilar materials. The interface between 3C-SiC and Si is the origin of a high density of planar and volume defects, such as misfit dislocations, micro twins (MTs), anti-phase boundaries (APBs) and stacking faults (SFs) in the epilayer and voids in Si underneath the hetero-interface. Some of these defects, such as MTs, vanished by growing very thick films while, in general, extended defects reduce their density but do not disappear. The reduction of these defects with the film thickness follows a self-annihilation mechanism, most of them (such as SFs and MTs) propagate along opposite crystallographic directions and are stimulated to meet one another in the film [3, 4]. Some of these defects are also generated during the film growth, due to local strain fields or mistakes in the arrangement sequence during the deposition, therefore defects such as SFs reduce their density but they tend to a saturation value without vanishing. Hence, the defects density in SiC decreases when the 3C-SiC thickness increases. Misfit dislocation and stacking faults are the two most important paths for stress relief on a highly mismatched hetero-epitaxy as 3C-SiC on Si. Misfit dislocations act to relieve a large part of the stress generated at the hetero-interface.

Stacking faults decrease in density by increasing the film thickness but also in thick films the values of SFs density are still high, with devastating consequences on the performances of 3C-SiC

based devices due to their high electrical activity [5, 6] that has been confirmed also by theoretical calculations [7]. The high electrical activity of crystallographic defects in n-type 3C-SiC can be due to accumulation of nitrogen at defects, the current will preferentially flow through them [8]. This observation further supports the experimental results of Nagasawa *et al.* [9], an increase of one order of magnitude in the SF linear density corresponds to an increase in the leakage current density of about three orders of magnitude at $V_R = 600V$.

Despite the great amount of work on the hetero-epitaxy of 3C-SiC, the mechanism of SFs reduction is not completely clear. Several studies have been performed in the past years to try to reduce the SFs density but it has been observed that is extremely difficult. It is known that close to the 3C-SiC/Si interface a high density of SFs is generated and then SFs growing on different [111] planes annihilate each other. This mechanism is not any more active when the SFs density decreases and then generally a saturation value for this density is observed around 10^4/cm. To decrease under this value the SFs density it is necessary to use a structured substrate [10].

Another strategy is proposed in this work and consists in the homo-epitaxial growth of 3C-SiC thick films, using the typical bulk growth techniques used for 4H-SiC [11], this process allows the reduction of SFs density under 10^4/cm depending on the growth rate conditions. We realized some thick 3C-SiC samples with homo-epitaxial processes on thin 3C-SiC films free standing, using three different values of growth rate (30 – 60 – 90 μm/h) to analyze the effect of growth condition on the formation of stacking faults defects.

Experimental Setup

The growth of 3C-SiC films was realized with a homo-epitaxial chemical vapor deposition (CVD) process, in a horizontal hot-wall reactor (LPE – PE1O6). Trichlorosilane ($SiHCl_3$ or TCS), ethylene (C_2H_4) and hydrogen (H_2) were used as silicon and carbon precursors and gas carrier, respectively. The processes were realized in a low pressure regime at a temperature of 1650°C, using a growth rate of 30 μm/h, 60 μm/h and 90 μm/h. The homo-epitaxies were realized on thin 3C-SiC films (50 μm) grown on Si (001). Before the homo-epitaxial growth the silicon substrate was removed with an etching process in a solution of HNO_3 and HF. After the homo-epitaxial deposition the total thickness of 3C-SiC samples realized was 150 μm. XRD analysis were performed to a large area investigation on the overall quality of the material and several TEM samples were prepared and analyzed in STEM mode in a JEOL 2010F, to understand the mechanisms of SFs generation and annihilation. To evaluate the SFs density, potassium hydroxide (KOH) etching was performed on homo-epitaxial films and then the observations of delineated defects by optical microscope were realized.

Results and Discussion

High Resolution XRD (HR-XRD) analyses were performed on 3C-SiC samples grown by hetero-epitaxy on [001] Silicon and by homo-epitaxial processes on a seed. The penetration depth of the beam is ~20μm. The thickness of the hetero-epitaxial layer is 50μm, also used as seed for homo-epitaxial growth (90μm/h). The data were represented through Reciprocal Space Maps [12] in the q_x-q_z scale as shown in Fig. 1. In the figure, the arrows represent the [111] crystallographic directions, where stacking faults are expected to contribute. The comparison between those two representative samples highlights that the homo-layer gains, within the depth probed, a higher degree of order which reflects on a shrinkage of the FWHM of the intensity distribution along the [111] direction in the RSM. The defects density consistently reduces, as will be discussed later on.

TEM cross-section analysis gives the opportunity to follow the SFs defects and determine their behavior. In Fig. 2 STEM cross section analyses are reported, showing some phenomena characterizing the SFS defects in a homo-epitaxial 3C-SiC film.

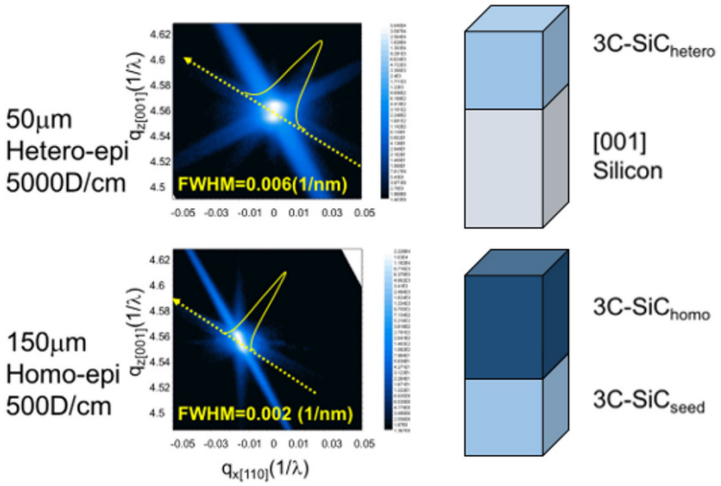

Fig. 1. HR-XRD analyses in RSM. The quality gained by a homo-epitaxial process reflects on the FWHM of the linescan along the [111] directions. The SFs densities are reported on the left side.

After the first microns of growth on Silicon (hetero-epitaxy), where the density of this defect is too high to follow, it is possible to observe that when different stacking faults, growing along opposite (111) planes, meet each other, some of them are annihilated while others continue to propagate as shown in Fig. 2a (the red arrow indicates the growth direction). This process continues in the first microns of growth until the linear density of the SFs decreases to a saturation value (~ 10^4/cm). Then, starting from thickness of about 10 microns, it is extremely difficult to reduce the stacking fault density under this value with a standard flat substrate. A large SFs reduction can be obtained at lower thickness only using a compliant substrate [10], while to further reduce the defect density, different process parameters should be tuned. One strategy consists of melting the original Silicon substrate to make the as grown 3C-SiC as seed for further growth. This is a process of homo-epitaxial growth that allowed reducing the SFs density under 10^4/cm, depending on the growth rate. The trend is represented in Fig. 3, providing the stacking fault linear density (per unit length) as a function of the growth rate in 3C-SiC homo-epitaxial layers grown at 1650°C. In Fig. 4 an image of a KOH etched 3C-SiC sample is shown where the SFs are visible. By cross-section TEM it was consistently found that SFs density is reduced far from the original interface, in full agreement with the HR-XRD data. It was also observed that SFs can be generated quite far from the 3C-SiC/Si interface (Fig. 2b) and annihilate without crossing with others SFs (Fig. 2c). Understanding how to increment the annihilation of SFs would allow further reducing the SFs density.

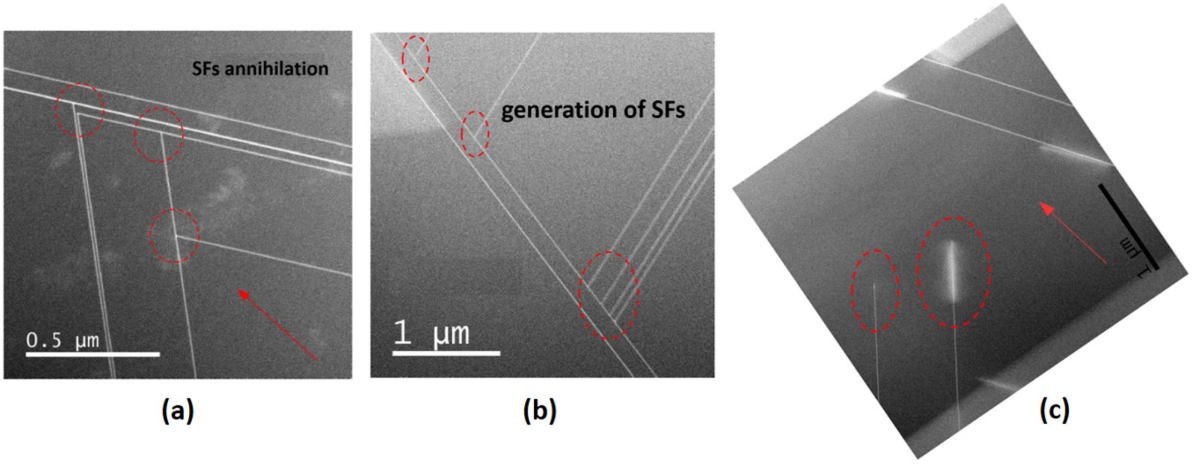

Fig. 2. (a) STEM cross section showing different SFs annihilation when these defects meet, (b) STEM cross section showing the generation of SFs, (c) STEM cross section showing the closing of two SFs without annihilation. Red arrows indicate the growth direction.

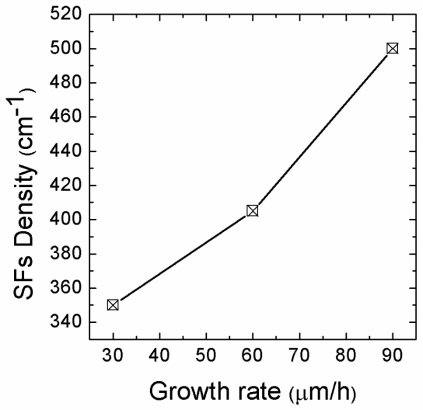

Fig. 3. Stacking Faults density versus the growth rate conditions.

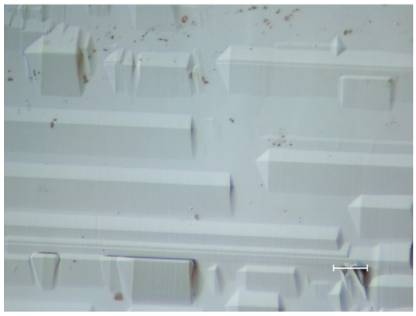

Fig. 4. Optical microscope image (1000X) of 3C-SiC etched in KOH.

In Fig. 3 is shown that for a thickness of 150 microns the SFs density is about 500/cm at a growth rate of 90 μm/h, while the SFs density decreases to 350/cm for a growth rate of 30 μm/h. This implies that the SFs closing is favorited by a condition of slow growth rate. A similar behavior has been predicted for some type of stacking faults in 4H-SiC [13]. In that case, by Monte Carlo simulations, it has been observed that increasing the temperature and decreasing the growth rate some SFs close because the growth rate of the "good" crystal is larger than the growth rate of the stacking fault.

Conclusions

A detailed characterization of Stacking Faults on 3C-SiC material was realized with the HR-XRD and STEM analysis, showing the behaviour of this typology of defect in the homo-epitaxial material. The homo-epitaxial growth of 3C-SiC thick films allows the reduction of the SFs density and in particular the use of slow growth rate favours the SFs closing. So homo-epitaxy is an alternative solution to the growth of 3C-SiC on compliant substrates for the reduction of defects in the material.

Acknowledgements

This work has been partially supported by the CHALLENGE project (HORIZON 2020 – NMBP – 720827)

References

[1] W.E. Nelson, F.A. Halden, and A. Rosengreen, J. Appl. Phys. 37 (1966) 333.
[2] S.E. Saddow, A. Agarwal, Advances in Silicon Carbide Processing and Applications, Artech House Publisher, Boston, © 2004.
[3] E. Polychroniadis, M. Syvajarvi, R.Yakimova, J.Stoemenos, J. Cryst. Growth 263 (2004) 68.
[4] Nagasawa H, Yagi K, Kawahara T, Hatta N, Chemical Vapor Deposition 12 (2006) 502.
[5] Lebedev AA, Abramov PL, Lebedev SP, Oganesyan GA, Tregubova AS, Shamshur DV, Physica B, 404 (2009) 4758.
[6] Song X, Michaud JF, Cayrel F, Zielinski M, Portail M, Chassagne T, Collard E, Alquier D, Applied Physics Letters, 96 (14) (2010) 142104.
[7] I. Deretzis, M. Camarda, F. La Via, and A. La Magna, Phys. Rev. B 85 (2012) 235310.
[8] A. Severino, G. D'Arrigo, C. Bongiorno, S. Scalese, F. La Via, and G. Foti, J. Appl. Phys. 102 (2007) 023518.
[9] Nagasawa H, Yagi K, Kawahara T, Hatta N, Abe M, Microelectronic Engineering, 83 (2006) 185.
[10] M. Meduňa, T. Kreiliger, I. Prieto, M. Mauceri, M. Puglisi, F. Mancarella, F. La Via, D. Crippa, L. Miglio and H. von Känel, Mater. Sci. Forum, 858 (2016) 147-150.
[11] L. Calcagno, G. Izzo, G. Litrico, G. Foti, F. La Via, G. Galvagno, M. Maceri and S. Leone J. Appl. Phys. 102 (2007) 043523.
[12] P. Klang and V. Holý, Semicond. Sci. Technol. 21 (2006) 352–357.
[13] M. Camarda, A. La Magna, A. Canino, F. La Via, Surf. Sci. 604 (2010) 939–942.