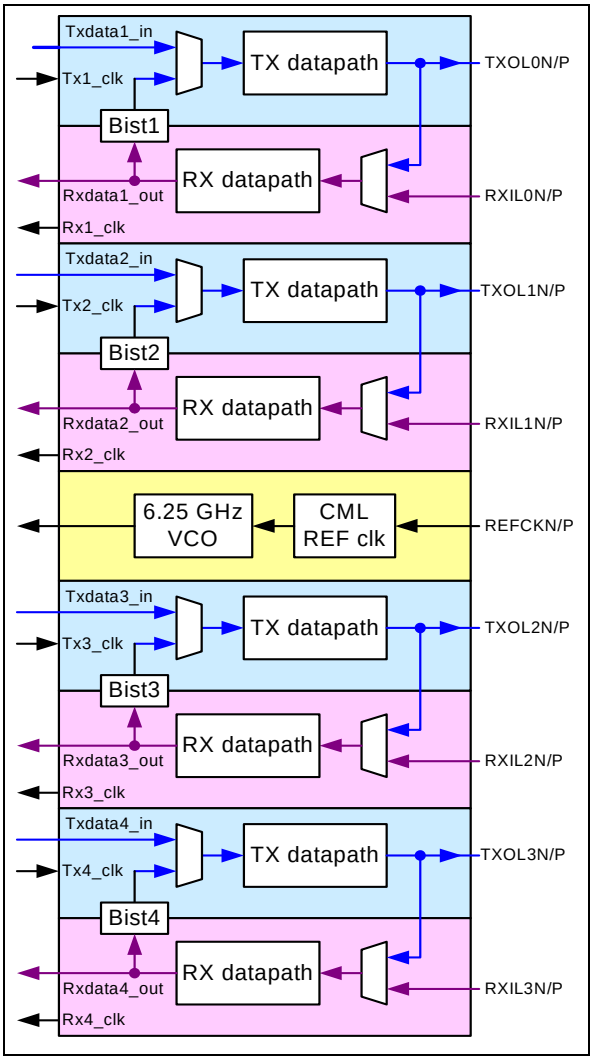
C65SPACE-HSSL

6.25 Gbps multi-rate, multi-lane, SerDes macro IP

Data brief



Features

- ST CMOS065LP low-power 65 nm CMOS technology
- 1.5625, 3.125 and 6.25 Gbps operation
- BER < 10^{-14}
- 20 bit TX and RX parallel data interface width / sub-rate mode
- Global power down and per link TX & RX power downs
- Compact form factor: 3040u x 1600u (tbc)
- Flip chip only layout
- Full immunity to single event latch-up (SEL) failures with a LET up to 60MeVcm2/mg
- No single event functional interrupts (SEFIs), up to 60MeVcm2/mg
- 1.2V power supply

Description

The ST 65 nm HSSL IP is a radiation hardened high-performance SERDES developed in ST CMOS065LP Low Power 65 nanometer CMOS technology and is provided as Flip chip only layout with build-in 2KV ESD protection. It features 8 channels (4Tx + 4 Rx) and is supplied by 1.2 volt.

It embeds a PLL and four identical data slices. Each data slice is composed of a data transmission lane and a data reception lane. The PLL provides very stable 6.25 GHz internal bit clock which is synthesized from a lower frequency input reference clock. This bit clock is used to generate each transmission bit clock and to recover each received bit clock.

Each data slice is running independently to each other. In each data slice, the transmitter and receiver are running independently to each other and may have different bit rate.

A +/-100ppm plesiochronous operation is guaranteed by design in each data lane individually and independently (Tx data lane and Rx data lane).

Each data slice embeds one BIST which contains: a PRBS generator, a BER monitor, an internal data lane loopback TX -> RX (in each data slice) and a TX clock jitter generator.

Overview

Tx lane features

- Differential CML outputs with polarity and/or bit order inversion.
- Programmable differential terminations of 100 ohms.
- 5 tap programmable pre-emphasis (1 precursor,1 cursor, 3 post-cursor).
- Programmable output amplitude with level boost mode.
- 20 bit parallel Interface running at 312.5 MHz with a possible frequency offset up to ±100ppm relative to the 6.25 GHz internal reference clock divided by 20.
- Clock aligner for Rx to Tx loop-back.
- Partial standby mode controlled by register.
- Test features:
  - IEEE 1149.1 (DC) and 1149.6 (AC) JTAG boundary scan support.
  - TX – RX full speed serial loop-back (in analog at pin level or internally in digital).
  - TX – RX and RX –TX parallel loop-back.
  - Five standard PRBS patterns generation.
  - Programmable 20 bit fixed transmission pattern generation.
  - Programmable triangular phase jitter generation for BER measurement.
  - Additional programmable bit rate frequency offset versus the 6.25 GHz reference clock for BER measurement.

Rx lane features

- Differential CML signaling with polarity and order inversion.
- Programmable differential terminations of 100 ohms.
- 20 bit parallel Interface running at 312.5 MHz.
- Up to ± 100ppm data rate offset tracking capability relative to 6.25 GHz internal reference clock.
- Up to ± 100ppm additional CDR tracking capability for received bit frequency swing.
- 4 tap adaptive Decision Feedback Equalizer (DFE).
- Linear Equalizer and gain control.
- Separate sampler for eye mapping & extraction of ISI coefficients for equalizer adaptation.
- Independently configurable per link multi-rate digital Clock and Data Recovery (CDR).
- Bit-Slip / phase control via the control bus.
- Test features:
  - IEEE 1149.1 (DC) and 1149.6 (AC) JTAG boundary scan support.
  - RX –TX parallel loop-back.
  - BER with Five standard PRBS patterns.
  - In-service eye mapping and spot measurement (vertical and horizontal).
  - Programmable RX sampling position within the data eye.

Radiation target performance

This high performance SERDES IP architecture was originally designed for communication networking market. Its intrinsic high robustness to terrestrials environment perturbations made it selected to be adapted to Space applications.

Intensive analysis of the sensitivity to radiations of all the blocks/cells was conducted and the design was significantly reworked while keeping original architecture and speed performance.

Specific layout precautions, fully compatible with SoC design practices, were applied to insure Single Event Latch-up (SEL) immunity up to 60 MeVcm2/mg Heavy Ions at 125°C Tj and Max voltage supply (ECSS-Q-60-15C standard).

Systematic usage of ST hardened cells library in combination with Triple Mode Redundancy (TMR) techniques were also implemented to ensure that no Single Event Functional Interrupt (SEFI) can occur up to 60 Mev/cm2/mg.

A BER < 10E-14 is obtained under terrestrial conditions, BER minimized degradations under different radiations (protons, heavy ions) have been characterized allowing users to determine the global system performance versus the space mission profile.

Revision history

Table 1. Document revision history

Date	Revision	Changes
13-May-2015	1	Initial release.