



L6743, L6743Q

High current MOSFET driver

Data Brief

Features

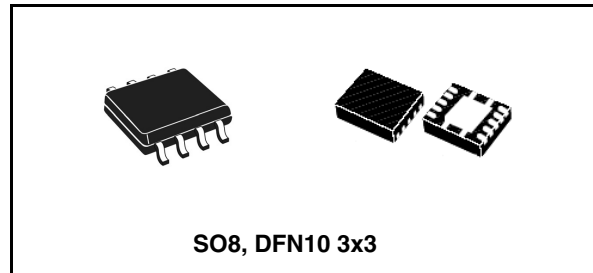
- Dual MOSFET driver for synchronous rectified converters
- High driving current for fast external MOSFET switching
- Integrated bootstrap diode
- High frequency operation
- Enable pin
- Adaptive dead-time management
- Flexible gate-drive: 5V to 12V compatible
- High-impedance (HiZ) Management for output stage shutdown
- Preliminary OV protection
- SO8 and DFN10 3x3 Package

Applications

- High current VRM / VRD for Desktop / Server / Workstation CPUs
- High current and high efficiency DC / DC Converters

Description

L6743, L6743Q is a flexible, high-frequency dual-driver specifically designed to drive N-Channel MOSFETs connected in Synchronous-Rectified Buck topology.



Combined with ST PWM Controllers, the driver allows implementing complete voltage regulator solutions for modern high-current CPUs and DCDC conversion in general. L6743, L6743Q embeds high-current drivers for both high-side and low-side MOSFETs. The device accepts flexible power supply (5V to 12V) to optimize the gate-drive voltage for High-Side and Low-Side maximizing the System Efficiency.

The Bootstrap diode is embedded saving the use of external diodes. Anti shoot-through management avoids high-side and low-side MOSFET to conduct simultaneously and, combined with Adaptive Dead-Time control, minimizes the LS body diode conduction time.

L6743, L6743Q embeds Preliminary OV Protection: after Vcc overcomes the UVLO and while the device is in HiZ, the LS MOSFET is turned ON to protect the load in case the output voltage overcomes a warning threshold protecting the output against HS failures.

The driver is available in SO8 and DFN10 3x3 packages.

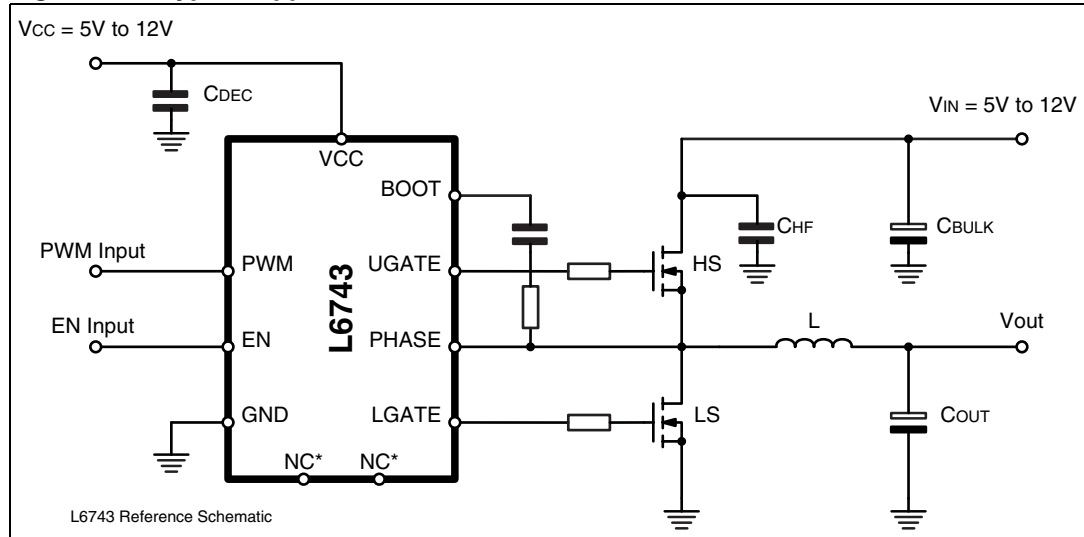
Table 1. Device summary

| Part Number | Package | Packaging |
|-------------|---------|-------------|
| L6743 | SO8 | Tube |
| L6743TR | SO8 | Tape & Reel |
| L6743Q | DFN10 | Tube |
| L6743QTR | DFN10 | Tape & Reel |

1 Typical application circuit and block diagram

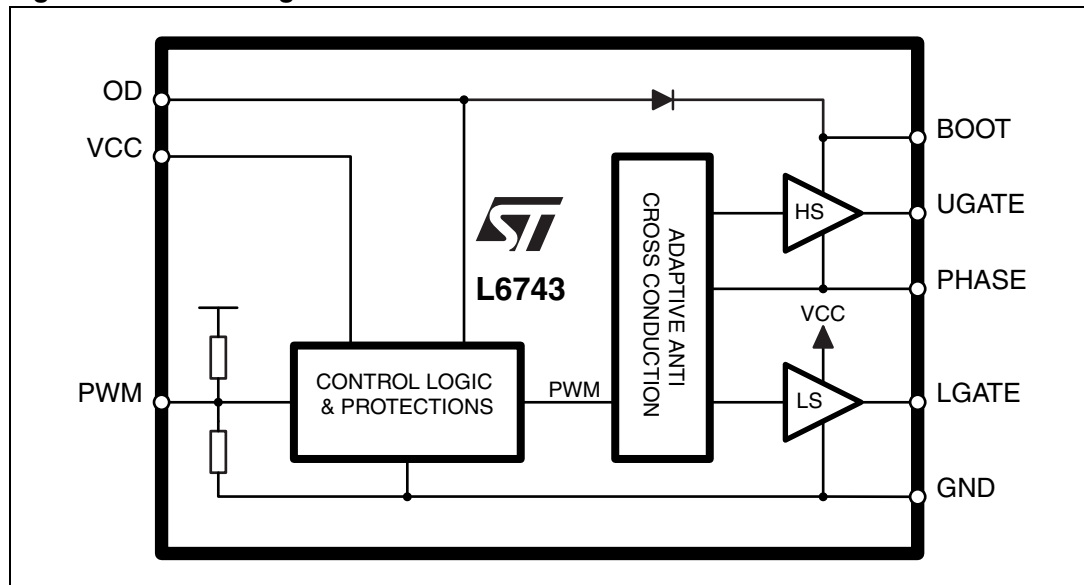
1.1 Application circuit

Figure 1. Typical application circuit



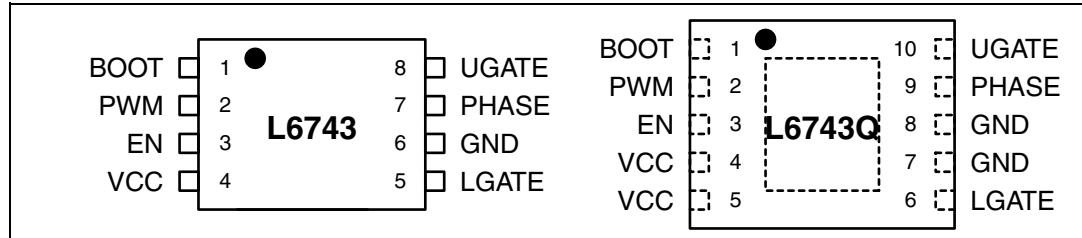
1.2 Block diagram

Figure 2. Block diagram



2 Pins description and connection diagrams

Figure 3. Pins connection (Top view)



2.1 Pin description

Table 2. Pins descriptions

| Pin # | | Name | Function |
|-------|-------|---------|---|
| SO8 | DFN10 | | |
| 1 | 1 | BOOT | High-Side Driver Supply. This pin supplies the High-Side floating driver. Connect through a $R_{BOOT} - C_{BOOT}$ capacitor to the PHASE pin. Internally connected to the cathode of the integrated Bootstrap diode. |
| 2 | 2 | PWM | Control input for the driver, 5V compatible. This pin controls the state of the driver and which external MOSFET have to be turned-ON according to EN status. If left floating and in conjunction with EN asserted, it causes the driver to enter the High-Impedance (HiZ) state which causes all MOSFETs to be OFF. |
| 3 | 3 | EN | Enable Input for the Driver. Pull High to enable the driver according to the PWM status. If pulled low will cause the drive to enter HiZ state with all MOSFET OFF regardless of the PWM status. |
| 4, 5 | 4 | VCC | Device and LS Driver power supply. Connect to any voltage between 5V and 12V. Bypass with low-ESR MLCC capacitor to GND. |
| 6 | 5 | LGATE | Low-Side Driver Output. Connect directly to the Low-Side MOSFET gate. A small series resistor can be useful to reduce dissipated power especially in high frequency applications. |
| 7, 8 | 6 | GND | All internal references, logic and drivers are referenced to this pin. Connect to the PCB ground plane. |
| 9 | 7 | PHASE | High-Side Driver return Path. Connect to the High-Side MOSFET Source. This pin is also monitored for the adaptive dead-time management and Pre-OV Protection. |
| 10 | 8 | UGATE | High-Side Driver Output. Connect to High-Side MOSFET gate. |
| PAD | - | TH. PAD | Thermal pad connects the Silicon substrate and makes good thermal contact with the PCB. Connect to the PGND plane. (DFN10 only) |

3 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

Table 3. SO8 Mechanical data

| Dim. | mm. | | | inch | | |
|-------|----------------------|------|------|-------|-------|-------|
| | Min | Typ | Max | Min | Typ | Max |
| A | 1.35 | | 1.75 | 0.053 | | 0.069 |
| A1 | 0.10 | | 0.25 | 0.004 | | 0.010 |
| A2 | 1.10 | | 1.65 | 0.043 | | 0.065 |
| B | 0.33 | | 0.51 | 0.013 | | 0.020 |
| C | 0.19 | | 0.25 | 0.007 | | 0.010 |
| D (1) | 4.80 | | 5.00 | 0.189 | | 0.197 |
| E | 3.80 | | 4.00 | 0.15 | | 0.157 |
| e | | 1.27 | | | 0.050 | |
| H | 5.80 | | 6.20 | 0.228 | | 0.244 |
| h | 0.25 | | 0.50 | 0.010 | | 0.020 |
| L | 0.40 | | 1.27 | 0.016 | | 0.050 |
| k | 0° (min.), 8° (max.) | | | | | |
| ddd | | | 0.10 | | | 0.004 |

1. Dimensions D does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm (.006inch) in total (both side).

Figure 4. SO8 package dimensions

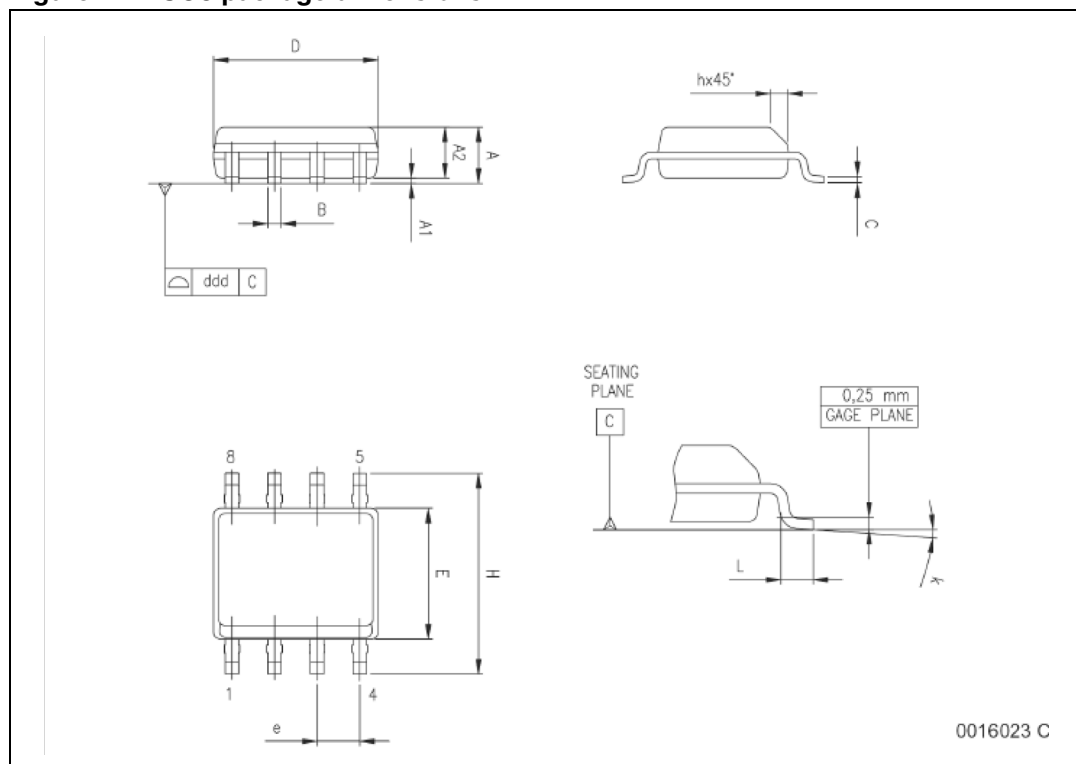
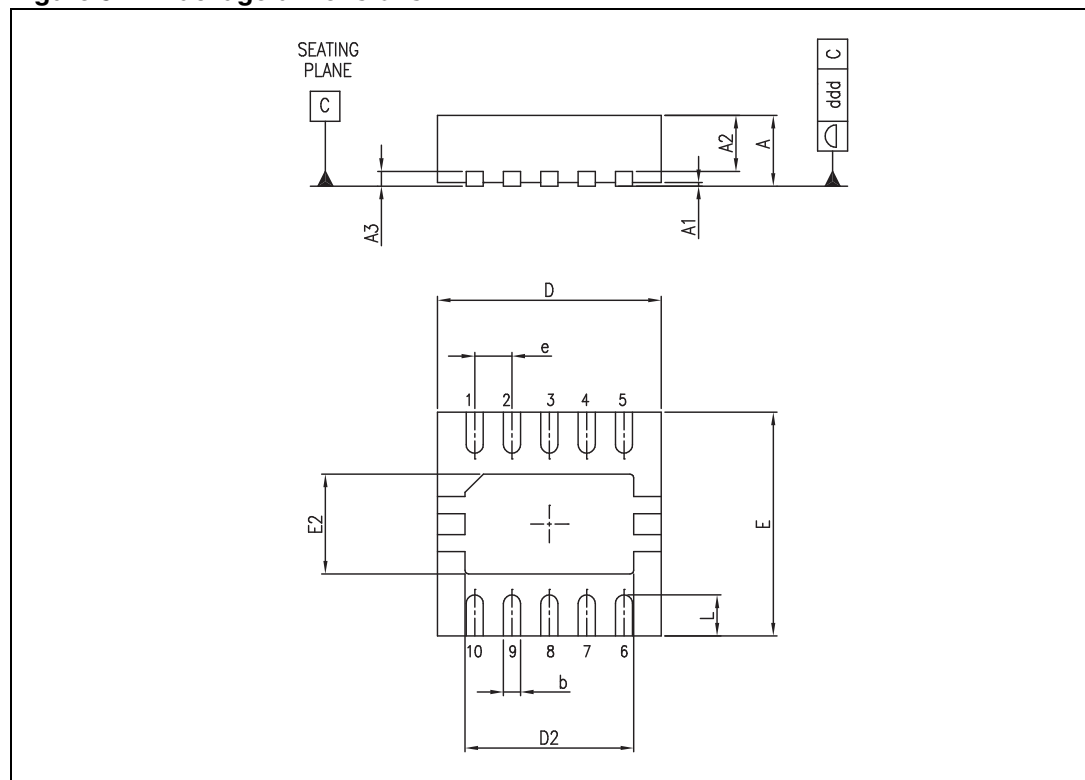


Table 4. DFN10 mechanical data

| Ref. | mm | | | inch | | |
|------|------|------|------|-------|-------|-------|
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| A | 0.80 | 0.90 | 1.00 | 0.031 | 0.035 | 0.039 |
| A1 | | 0.02 | 0.05 | | 0.001 | 0.002 |
| A2 | | 0.70 | | | 0.028 | |
| A3 | | 0.20 | | | 0.008 | |
| b | 0.18 | 0.23 | 0.30 | 0.007 | 0.009 | 0.012 |
| D | | 3.00 | | | 0.118 | |
| D2 | 2.21 | 2.26 | 2.31 | 0.087 | 0.089 | 0.091 |
| E | | 3.00 | | | 0.118 | |
| E2 | 1.49 | 1.64 | 1.74 | 0.059 | 0.065 | 0.069 |
| e | | 0.50 | | | 0.20 | |
| L | 0.3 | 0.4 | 0.5 | 0.012 | 0.016 | 0.020 |

Figure 5. Package dimensions



4 Revision history

Table 5. Document revision history

| Date | Revision | Changes |
|-------------|----------|------------------|
| 30-Mar-2007 | 1 | Initial release. |

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