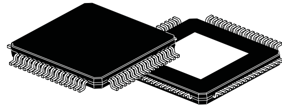
L9965A

Data brief

Automotive 18s battery monitor

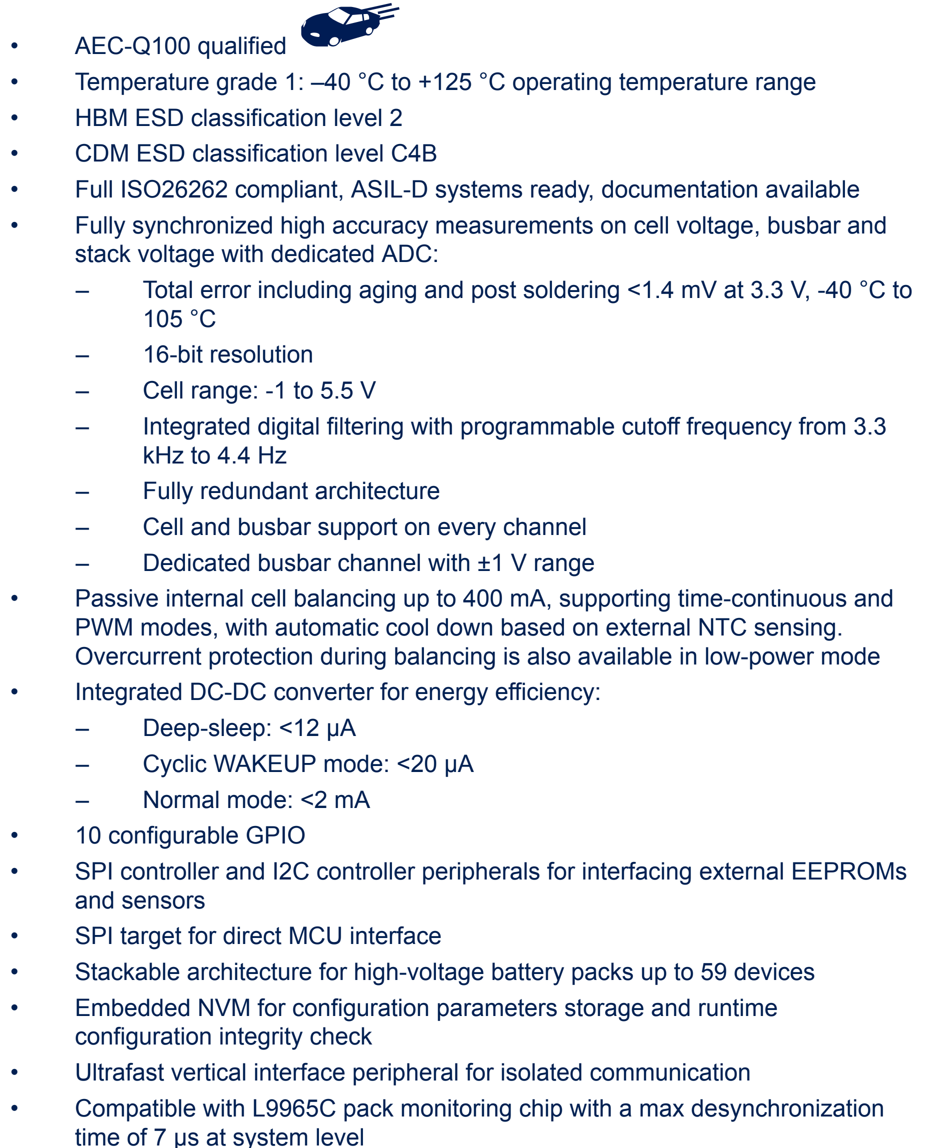


TQFP64 exposed pad down

Product status link
L9965A

Product summary	
Order code	L69965A-TR
Package	TQFP64
Packing	Tape and reel

Features



- AEC-Q100 qualified
- Temperature grade 1: –40 °C to +125 °C operating temperature range
- HBM ESD classification level 2
- CDM ESD classification level C4B
- Full ISO26262 compliant, ASIL-D systems ready, documentation available
- Fully synchronized high accuracy measurements on cell voltage, busbar and stack voltage with dedicated ADC:
  – Total error including aging and post soldering <1.4 mV at 3.3 V, -40 °C to 105 °C
  – 16-bit resolution
  – Cell range: -1 to 5.5 V
  – Integrated digital filtering with programmable cutoff frequency from 3.3 kHz to 4.4 Hz
  – Fully redundant architecture
  – Cell and busbar support on every channel
  – Dedicated busbar channel with ±1 V range
- Passive internal cell balancing up to 400 mA, supporting time-continuous and PWM modes, with automatic cool down based on external NTC sensing. Overcurrent protection during balancing is also available in low-power mode
- Integrated DC-DC converter for energy efficiency:
  – Deep-sleep: <12 µA
  – Cyclic WAKEUP mode: <20 µA
  – Normal mode: <2 mA
- 10 configurable GPIO
- SPI controller and I2C controller peripherals for interfacing external EEPROMs and sensors
- SPI target for direct MCU interface
- Stackable architecture for high-voltage battery packs up to 59 devices
- Embedded NVM for configuration parameters storage and runtime configuration integrity check
- Ultrafast vertical interface peripheral for isolated communication
- Compatible with L9965C pack monitoring chip with a max desynchronization time of 7 µs at system level

Application

- Automotive battery management system
- Battery storage system for commercial
- UPS

Description

The L9965A is an 18 channel battery cells monitoring and balancing IC.

1 Overview

The L9965A BMIC device provides all the functions needed to manage battery pack configurations up to 18s. It features a comprehensive set of cell/pack monitoring, balancing, and protection functions designed to achieve ASIL-D targets in demanding systems.

The device belongs to the L9965 chipset family for high-voltage battery management systems monitoring and control.

L9965A uses dedicated high-precision ADCs synchronously acquiring cells, busbar and pack voltage. The cell measurement ranges from -1 V to 5.5 V, making the L9965 family suitable for most battery chemistries.

An arbitrary number of busbars can be monitored by every cell voltage pair and a dedicated BB channel.

The BMIC is supplied via an efficient buck preregulator, thus optimizing energy consumption and heat dissipation. It also integrates a 5V LDO available for biasing external sensors and supplying external EEPROMs.

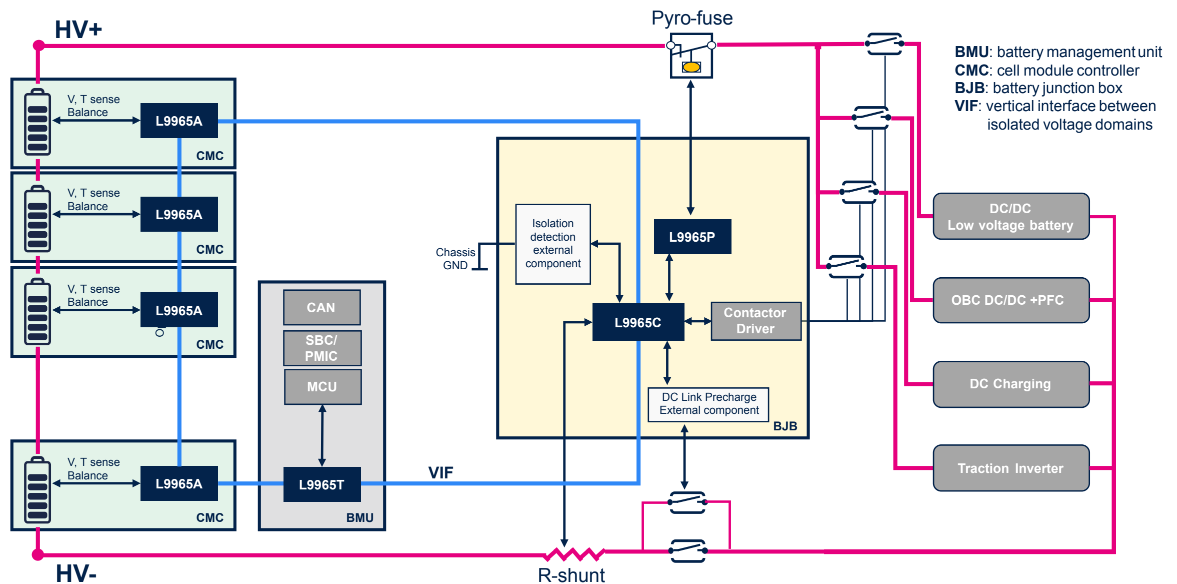
A SPI controller and I2C controller peripherals allow interfacing the device with external sensors and EEPROMs.

Passive balancing is available in both continuous and PWM mode.

Up to 59 addressable devices can be stacked in a vertical isolated communication interface.

L9965A implements an ultrafast isolated communication protocol allowing to transfer voltage and temperature data of the whole daisy-chain and in less than 10 ms.

Figure 1. L9965A battery monitor in BMS system



L9965A embeds a functional state machine to optimize system power consumption without compromising safety functions:

- NORMAL: full operation mode.
- CYCLIC WAKEUP: low-power mode triggered by L9965T companion chip, to perform cyclic diagnostics during low-power operation. In this state, the device is sensitive to fault/wake-up tones from the VIF.
- SILENT BALANCING: low-power state for managing long balancing periods. In this state the device is sensitive to wake-up tones both from the VIF in case of fault and from the SPI if directly connected to the MCU, moreover the balancing overcurrent is active.
- DEEP SLEEP: Ultralow power state for managing long inactivity periods. In this state, the device is sensitive to wake-up tones both from the VIF in case of fault and from the SPI if directly connected to the MCU.

2 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

2.1 TQFP64 (10x10x1 mm exp. pad down) package information

Figure 2. TQFP64 (10x10x1 mm exp. pad down) package outline

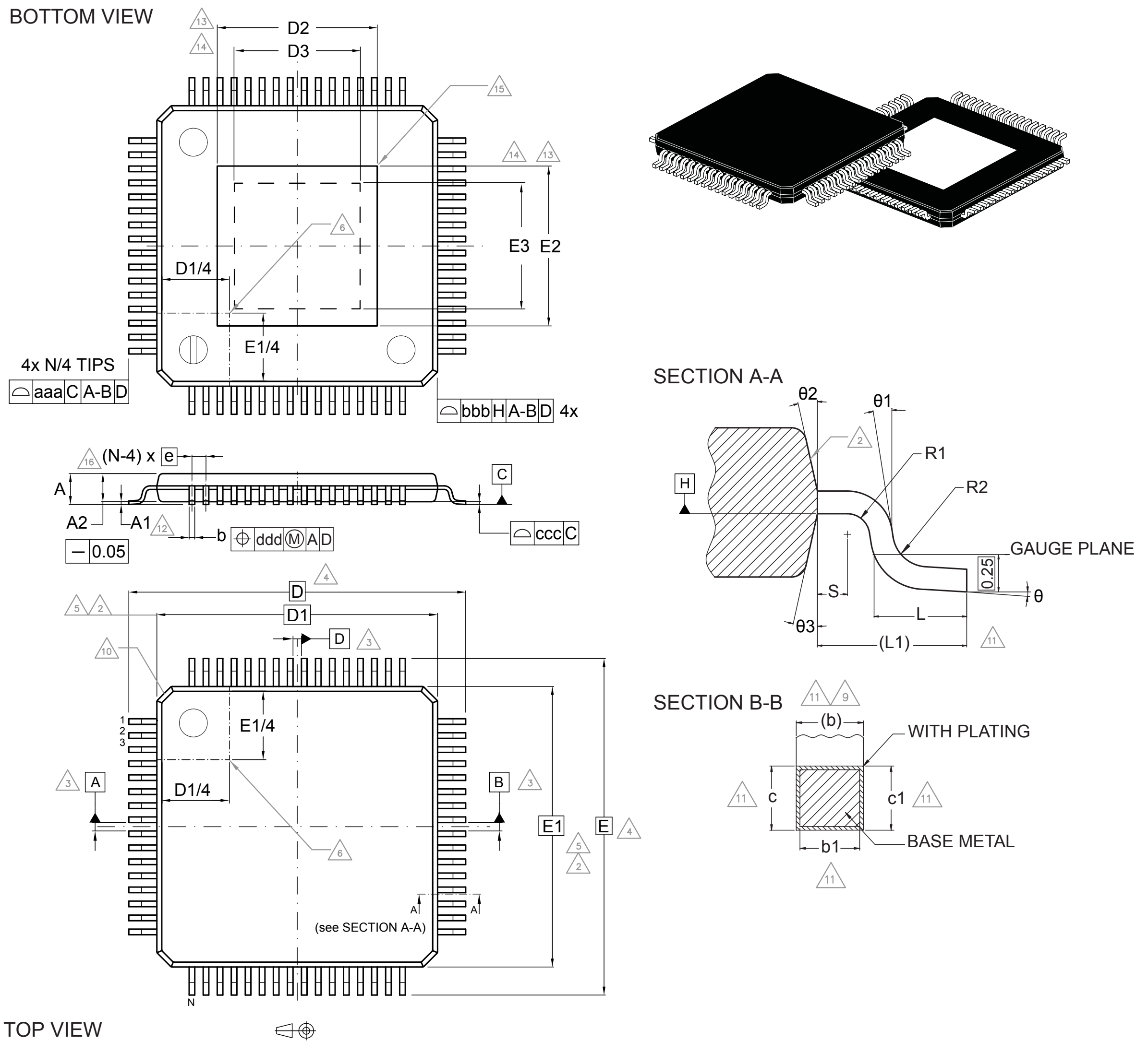


Table 1. **TQFP64 (10x10x1 mm exp. pad down) package mechanical data**

Ref	Min.	Typ.	Max.	Note (see # in Notes below)
Θ	0°	3.5°	7°	-
Θ1	0°	-	-	-
Θ2	11°	12°	13°	-
Θ3	11°	12°	13°	-
A	-	-	1.2	15
A1	0.05	-	0.15	12
A2	0.95	1	1.05	15
b	0.17	0.22	0.27	9, 11
b1	0.17	0.2	0.23	11
c	0.09	-	0.2	11
c1	0.09	-	0.16	11
D	-	12.00 BSC	-	4
D1	-	10.00 BSC	-	5, 2
D2	-	-	6.4	13
D3	4.8	-	-	14
e	-	0.50 BSC	-	-
E	-	12.00 BSC	-	4
E1(*)	-	10.00 BSC	-	5, 2
E2	-	-	6.4	13
E3	4.8	-	-	14
L	0.45	0.6	0.75	-
L1	-	1.00 REF	-	-
N	-	64	-	16
R1	0.08	-	-	-
R2	0.08	-	0.2	-
S	0.2	-	-	-
Tolerance of form and position				
aaa	-	0.2	-	1, 7
bbb	-	0.2	-	
ccc	-	0.08	-	
ddd	-	0.08	-	

Notes

1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994.
2. The Top package body size may be smaller than the bottom package size up to 0.15 mm.
3. Datum A-B and D to be determined at datum plane H.
4. To be determined at seating datum plane C.
5. Dimensions D1 and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is “0.25 mm” per side. D1 and E1 are Maximum plastic body size dimensions including mold mismatch.
6. Details of pin 1 identifier are optional but must be located within the zone indicated.
7. All Dimensions are in millimeters.

8. No intrusion allowed inwards the leads.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum “b” dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.
10. Exact shape of each corner is optional.
11. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
12. A1 is defined as the distance from the seating plane to the lowest point on the package body.
13. Dimensions D2 and E2 show the maximum exposed metal area on the package surface where the exposed pad is located (if present). It includes all metal protrusions from exposed pad itself.
14. Dimensions D3 and E3 show the minimum solderable area, defined as the portion of exposed pad which is guaranteed to be free from resin flashes/bleeds, bordered by internal edge of inner groove.
15. The optional exposed pad is generally coincident with the top or bottom side of the package and not allowed to protrude beyond that surface.
16. “N” is the number of terminal positions for the specified body size.

Revision history

Table 2. **Document revision history**

Date	Revision	Changes
05-Nov-2024	1	Initial release.

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