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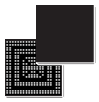
# SR6P3C4

Data brief

# Stellar SR6 P3 line—32-bit Arm® Cortex®-R52+ automotive integration MCU 3× Cortex®-R52+ cores, 8 MB NVM (2× 7.5 MB “OTA X2”) 1.3 MB RAM, with embedded virtualization, safety, and security



FPBGA292

(17 × 17 mm)

Stellar

| Product summary | |
|---|---|
| **Part number** | **Package** |
| SR6P3C4 | FPBGA292 |

## Features

- AEC-Q100
- SR6 integration *MCU*s:
  - Have superior real-time and safe performance (with highest *ASIL*-D capability)
  - Bring hardware-based virtualization technology to *MCU*s for simplified multiple software integrations at optimized performance
  - Have built-in fast and cost-effective *OTA* reprogramming capability (with built-in dual-image storage)
  - Offer high-speed security cryptographic services, for example for network authentication

### Cores

- 3 × 32-bit Cortex®-R52+ cores (all of them in lockstep configuration):
  - Arm® v8-R compliant
  - Single precision floating-point unit (*FPU*)
  - New privilege level for real-time virtualization
- 2 Cortex®-M4 multipurpose accelerators, one in lockstep configuration
- 4 *eDMA* engines in lockstep configuration

### Memories

- Up to 8 MB on-chip nonvolatile memory (NVM):
  - PCM (phase-change memory) as nonvolatile memory
  - 7.5 MB code NVM, with embedded memory replication for OTA (over-the-air) reprogramming with up to 2× 7.5 MB
  - 512 KB HSM-dedicated code NVM
- 256 KB data NVM (128 KB + 128 KB dedicated to HSM)
- Up to 1328 KB on-chip general-purpose SRAM

**Security: 2nd generation hardware security module**

- Cybersecurity: ISO/SAE 21434 compliance (refer to the cybersecurity reference manual for details)
- On-chip high-performance security module with full support for e-safety vehicle intrusion protected applications (EVITA)
- Symmetric and asymmetric cryptography processor
- High-performance lock-stepped AES-light security subsystem for fast ASIL-D cryptographic services

**Safety: comprehensive new-generation ASIL-D safety concept**

- New state-of-the-art safety measures at all levels of the architecture for most efficient implementation of ISO 26262 ASIL-D functionalities
- Complete hardware virtualization architecture built on Cortex®-R52+ new privilege mode (best-in-class software isolation, real-time support for multiple virtual machines/applications)

**Peripheral, I/O, and communication interfaces**

- 16 LINFlexD modules
- 1 dual-channel FlexRay controller
- 10 queued serial peripheral interface (SPIQ) modules
- 2 microsecond channels (MSC) and 1 microsecond plus (MSC-Plus) channel
- 2 I²C interfaces
- 2 SENT modules (10 channels each)
- 2 PSI5 modules (1 channel each)
- Enhanced analog-to-digital converter system with:
  - 6 separate 12-bit SAR analog converters (including one supervisor/safety ADC).
  - 4 separate 9-bit SAR analog converters (2 channels each) with fast comparator mode
  - 6 separate 16-bit sigma-delta analog converters with embedded DSP processor on each SD ADC
  - Enhanced interconnection with GTM timer for autonomous ADC/GTM subsystem operation
- Advanced timed I/O capability:
  - Generic timer module (GTM4124)
  - High-resolution timer
- Communication interfaces:
  - One 10/100/1000 Mbit/s Ethernet controller compliant with IEEE 802.3-2008: IPv4 and IPv6 checksum modules, AVB, VLAN
  - 7 modular controller area network (MCAN) modules, and 1 time-triggered controller area network (M_TTCAN), all supporting flexible data rate (ISO CAN FD®)
  - 2 CAN XL® interfaces

# 1 Introduction

## 1.1 Document overview

This document provides a summary of the target specification and features of the SR6P3C4 devices. For detailed information, refer to the device Datasheet and device Reference manual.

*Note: For information on the Cortex®-R52+ and Cortex®-M4 cores, refer to the technical reference manuals, available from the www.arm.com website.*

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## 1.2 Description

Stellar integration MCUs have been designed to meet the requirements of domain controllers and ECUs with high integration requested in the architectures of connected updatable automated and electrified cars. They have superior real-time and safe performance (with highest ASIL-D capability). Bringing hardware-based virtualization technology to MCUs, they ease the development and integration of multiple source software onto the same hardware while maximizing the resulting software performance. They offer high-efficiency OTA reprogramming capability with fast new image download and activation at almost no memory overhead thanks to SR6 unique built-in dual-image storage tailored to OTA reprogramming needs. They also provide high-speed security cryptographic services, for instance for network authentication.

**Table 1. SR6P3C4 overview**

| Feature | | SR6P3C4 |
|---|---|---|
| Cortex®-R52+ cores (+ checker cores) | | 3 cores (+3 checkers) |
| Neon™ (with SIMD, dual precision floating point) | | No |
| Cache (instruction/data) per core in Kbyte | | 16/8 |
| Core memory protection unit (regions), several additional protection mechanisms in the architecture, for example: NOC firewalls | Hypervisor (EL2) | 24 |
| | OS (EL1) | 24 |
| Code NVM | Overall including HSM in Mbytes | 8 |
| | Cluster code NVM in Mbytes | 7.5 |
| | HSM code NVM in Kbytes | 512 |
| Code NVM built-in memory replication for OTA reprogramming (not supported by HSM) in Mbytes | | Up to 2× 7.5 |
| Data NVM in Kbytes | | 256 |
| RAM in Kbytes | | 1328 |
| Hardware security module (HSM) - 2nd generation | | Yes |
| AES-Light (cryptographic services) | | 2 |
| Arm® Cortex®-M4 | Multipurpose accelerator (DSPH) | 1 |
| | Multi-purpose accelerator in lockstep (DME) | 1 |
| eDMA engines (number of channels, more channels through muxes/channel) | Engine | 4 |
| | Channel | 4× 32 |
| LIN and UART (LINFlexD) | | 16 |
| CAN_FD | | 8 |
| CAN_XL | | 2 |
| SPIQ (with LVDS channel) | | 10 (2) |
| Microsecond channel (MSC) | | 2 |

| Feature | | SR6P3C4 |
|---|---|---|
| SENT | Unit | 2 |
| | Channel/unit | 10 |
| I²C | | 2 |
| PSI5 | Unit | 2 |
| | Channel/unit | 1 channel |
| FlexRay™ (dual channel) | | 1 |
| Gigabit ethernet IEEE 802.3-2008 compliant | Total | 1 |
| | With MII, RMII, RGMII, and SGMII | 0 |
| | With MII, RMII, and RGMII | 1 |
| | With RMII and SGMII | 0 |
| SIPI/LFAST interprocessor bus | | 1 |
| Generic timer modules (GTM4) | | GTM4124 |
| High-resolution timer | | 2 × 8 ch |
| 12-bit SAR analog converters | | 6 |
| 16-bit sigma-delta analog converters (units with DSPL) | | 6 |
| 9-bit SAR analog comparators | | 8 |
| Octo-SPI (support HyperBus™ memory devices) | | No |
| Debug port | Main debug port (JTAG+SWD) | Yes |
| | Secondary debug port (SWD) | Yes |
| High-speed off-chip trace lane (multi GBit/s, Aurora™ protocol) | | 2 |
| Max temperature (target) | Junction temperature | 165 °C(1) |
| Packages | FPBGA516 | — |
| | FPBGA476 | — |
| | FPBGA292 | X |

1. *Nominal specification up to 150 °C. Delta specification up to 165 °C.*

## 1.3 Block diagram

The figure below shows the top-level block diagram.

**Figure 1. Block diagram**

## Revision history

Table 2. **Document revision history**

| Date | Version | Changes |
|---|---|---|
| 22-Oct-2024 | 1 | Initial release. |

## Glossary

**ADC** Analog-to-digital converter

**AEC** Automotive Electronics Council. Also known as CDF-AEC for Chrysler-Delco-Ford Automotive Electronics Council. Shortened to AEC.

**AES** Advanced encryption standard. Cryptographic algorithm.

**ASIL** Automotive safety integrity level

It is a risk classification system defined by the ISO 26262 standard for the functional safety of road vehicles. There are four ASILs identified by ISO 26262—A, B, C, and D. ASIL A represents the lowest degree and ASIL D represents the highest degree of automotive hazard.

**AVB** Audio-video bridging

**BCS** Boot code sector

**BSC** Basic (dimension)

**CAN** Controller area network

**CAN FD®** Controller area network flexible data rate

**CAN XL®** Controller area network extra long

**CBC** Cipher block chaining

**CDM** Charged device model

**CFB** Cipher feedback

**CGM** Clock generation module

**CMAC** Cipher-based message authentication code

**CMD** Command

**CMOS** Complementary metal-oxide-semiconductor

**COL** Collision detect

Asynchronous receiver signal of the media-independent interface (MII).

**CPHA** Clock phase bit. Selects the clock phase.

**CPOL** Clock polarity bit. Selects the clock polarity.

**CPU** Central processing unit

**CRC** Cyclic redundancy check

**CRS** Carrier sense

Asynchronous receiver signal of the media-independent interface (MII).

**CTI** Arm® CoreSight™ cross-trigger interface

**CTM** Cross-trigger matrix

**CTR** Counter mode

**CXPI** Clock extension peripheral interface

**DAC** Digital-to-analog converter

**DC** Direct current

**DCF** Device configuration format

**DDR** Double data rate

**DMA** Direct memory access

**DME** Data movement engine

**DNL** Differential nonlinearity

**DSP** Digital signal processing

**eDMA** Enhanced direct memory access

**EMC** Electromagnetic compatibility

**EVITA** e-safety vehicle intrusion protected applications

**FCCU** Fault collection and control unit

**FPBGA** Fine-pitch-ball-grid-array

**FPU** Floating-point unit

**GB** Gigabyte

**GPIO** General-purpose input/output

**GTM** Generic timer module

**HSM** Hardware security module

**HSSTP** High-speed serial trace probe

**I/O** Input/output

**IEC** International Electrotechnical Commission

**IEEE** Institute of Electrical and Electronics Engineers

**IPv4** Internet protocol version 4

**IPv6** Internet protocol version 6

**ISO** International Organization for Standardization

**I²C** Inter-integrated circuit

**JEDEC** Joint Electron Device Engineering Council

**JTAG** Joint Test Action Group

**KB** Kilobyte

**LFAST** LVDS fast asynchronous serial transmit interface

**LIN** Local interconnect network

**LVDS** Low-voltage differential signaling

**M_TTCAN** Time-triggered controller area network

**MB** Megabyte

**MCAN** Modular controller area network

**MCU** Microcontroller unit

**MEMU** Memory error management unit

**MII** Media-independent interface

**MSC** Microsecond channel

**NoC** Network on chip

**NVM** Nonvolatile memory

**OS** Operating system

**OSR** Oversampling ratio

**OTA** Over the air

**PHY** Physical layer

**PLL** Phase-locked loop

**PSI5** Peripheral sensor interface (PSI5). An interface for automotive sensor applications.

**RAM** Random access memory

**RGMII** Reduced gigabit media-independent interface

**RMII** Reduced media-independent interface

**SAR** Successive approximation register

**SENT** Single-edge nibble transmission for automotive applications

**SeooC** Safety element out of context

**SIMD** Single-instruction multiple data

**SIPI** Serial interprocessor interface

**SPI** Serial peripheral interface

**SPIQ** Queued serial peripheral interface

**SRAM** Static random-access memory

**SRC** Sample rate converter

**ST** STMicroelectronics

**STLA** Signal tap logic analyzer

**SWD** Secondary debug port

**UART** Universal asynchronous receiver/transmitter

**VLAN** Virtual local area network

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