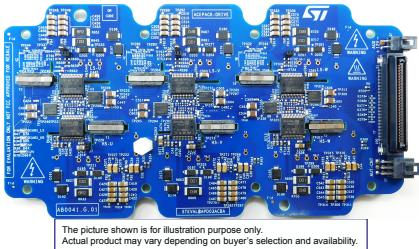


## ASIL D gate driver board for traction inverter in EV/HEV applications



### Features

- 12 V input voltage
- Motor control connector (34 pin) for hardware compatibility with all the ST power board for motor control applications
- Galvanically isolated driving stage with L9502E for ASIL D applications
- Fully optimized for ACEPACK SiC power modules
- Protection functions: miller clamp, desaturation detection, hybrid turn-off (HTO) UVLO, and OVLO
- Compatible with all ACEPACK DRIVE SiC module family (750V and 1200V)
- Press fit connections for high reliable and long lasting connection
- Layout optimized with minimized stray inductances
- High reliability and robustness

Product summary	
ASIL D gate driver board for traction inverter in EV/HEV applications	STEVAL-APD03ACB
Control board for automotive motor control applications based on SR5E1E3 and PMIC SPSB100	STEVAL-TTM007A
SR5 E1 line of Stellar electrification MCUs, 32-bit Arm Cortex M7 automotive MCU 2x cores, 2 MB Flash, rich analog, high-resolution timer, HSM, ASIL-D	SR5E1E370C30F01X
Application	Automotive Motor Control

### Description

The **STEVAL-APD03ACB** is an evaluation board aimed at evaluating the ACEPACK DRIVE power module (compatible with both 750 and 1200 V) for automotive powertrain applications.

The evaluation is schematized in the following main blocks:

Driving section, hosting mainly the driver L9502E with flyback controller integrated to generate the driving voltages (+18/-5V) with high current capability (up to 15A).

Diagnostic of the driving circuitry and the connectors towards the power supply section. This board can be connected to the power module by a press fit insertion tool (design available).

The control section is not included but can be separately ordered, choosing the **STEVAL-TTM007A**.

The **STEVAL-TTM007A** hosts the **SR5E1E3** (eTQFP100) which is a 2x 32-bit Arm® Cortex® -M7 with double precision FPU, L1 cache and DSP instructions with 2 cores in parallel or 1 core in lockstep configuration.

The **PMIC SPSB100** is available for a configurable multioutput voltage for highly integrated processors.

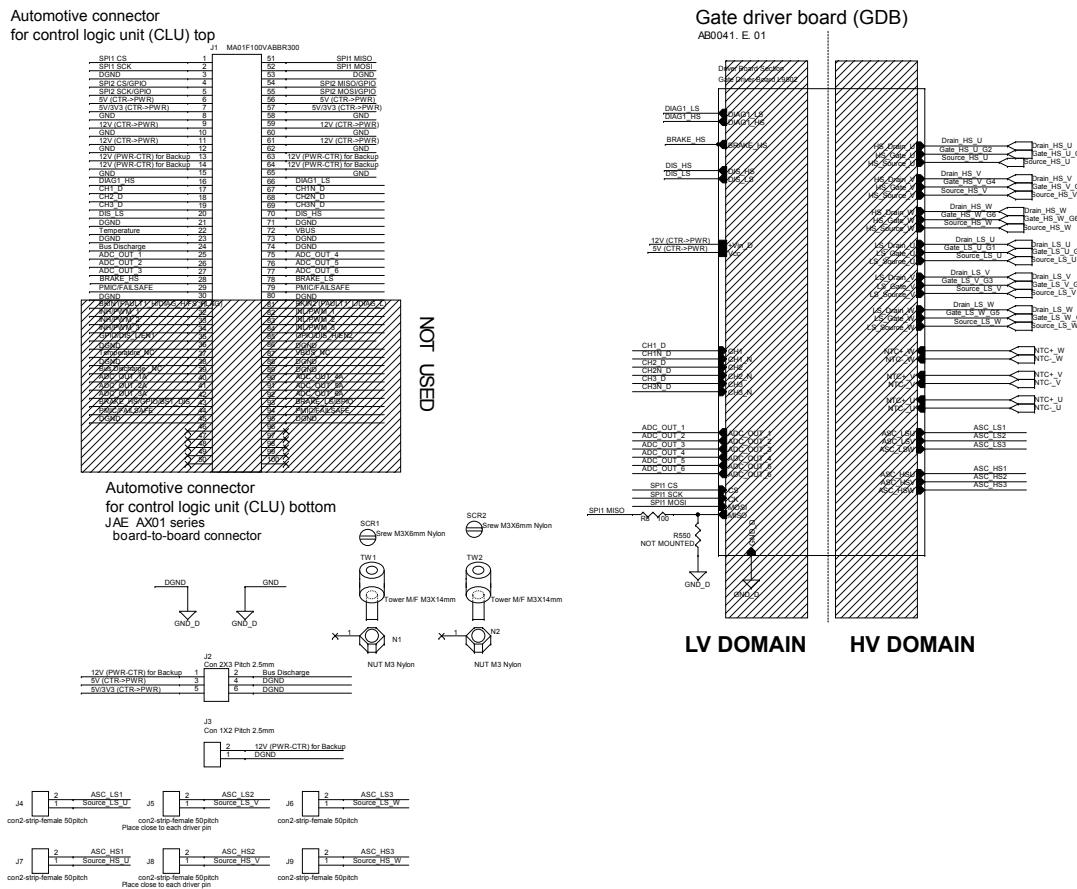
The **SR5E1E3** and the **SPSB100** offer the best performance thanks to dedicated peripherals for motor control.

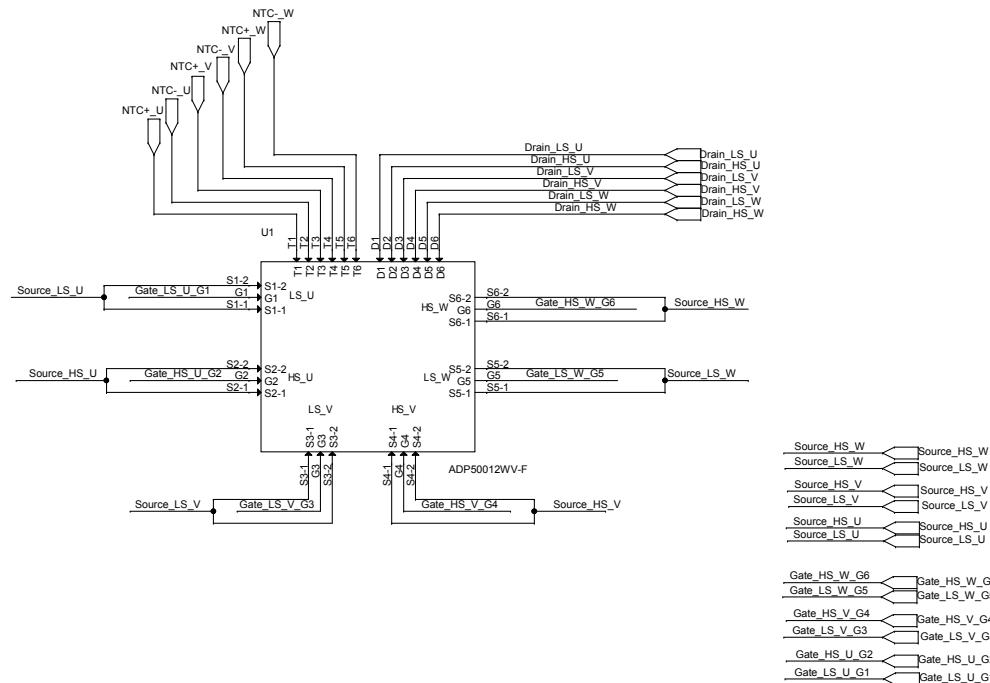
A double and redundant signal conditioning, for reading the resolver feedback, has been included to guarantee the implementation of the most advanced field-oriented control algorithms.

# 1 Schematic diagrams

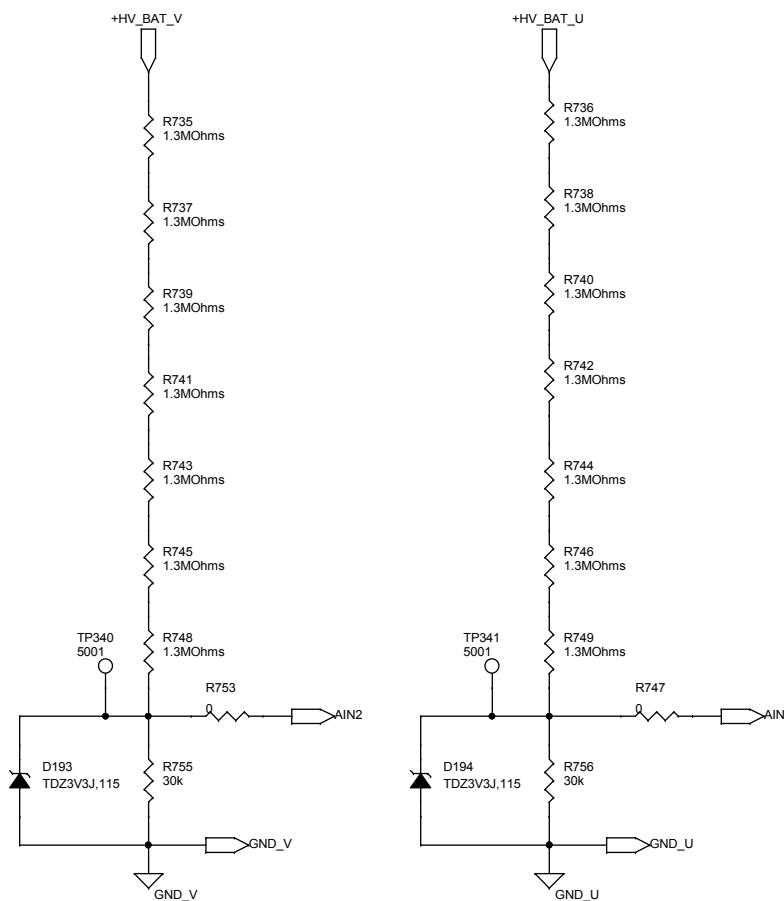
**Notice:** These schematics are for illustration purpose only. Actual product may vary depending on buyer's selection and availability.

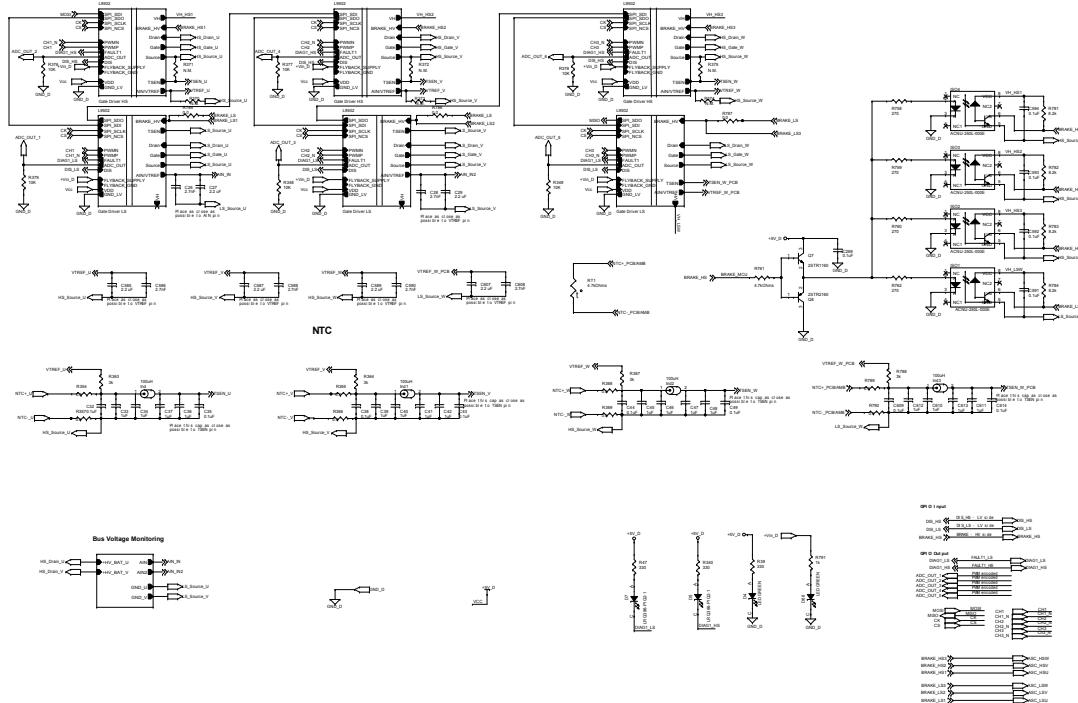
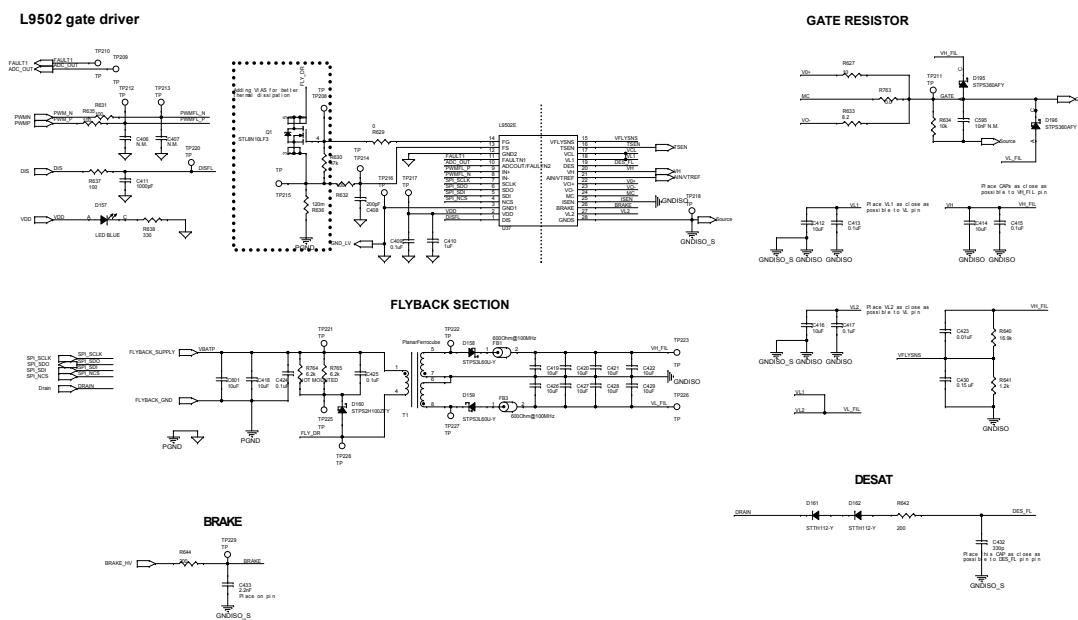
**Figure 1. STEVAL-APD03ACB circuit schematic (1 of 10)**



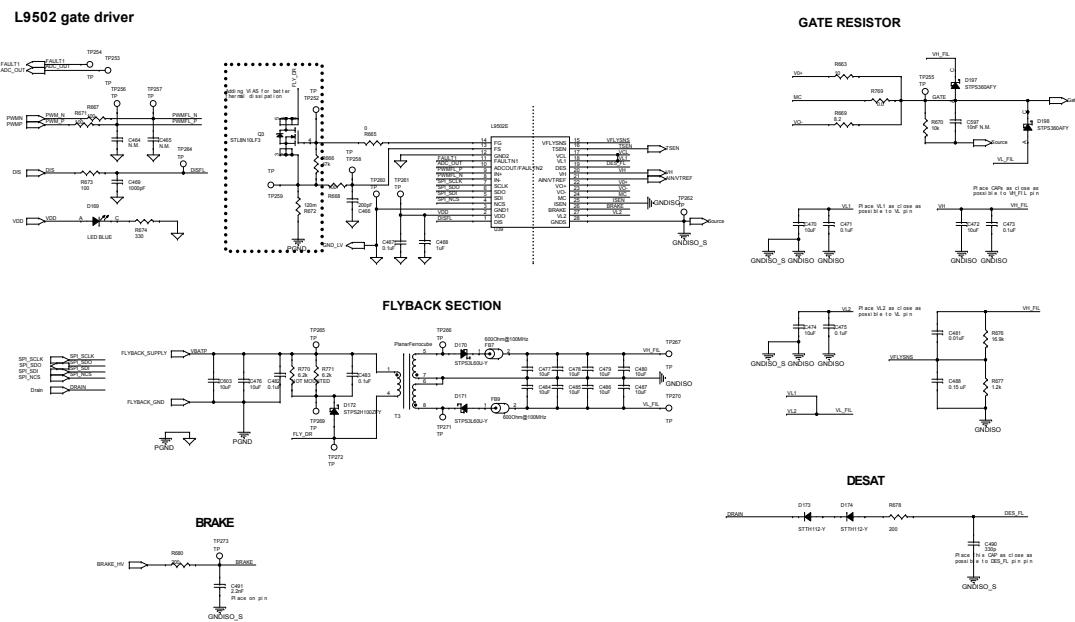
**Figure 2. STEVAL-APD03ACB circuit schematic (2 of 10)**


PLEASE TAKE CARE ABOUT POSITION OF COMPONENTS FAR FROM ACEPACK MODULE PIN ON TOP AND BOTTOM SIDE

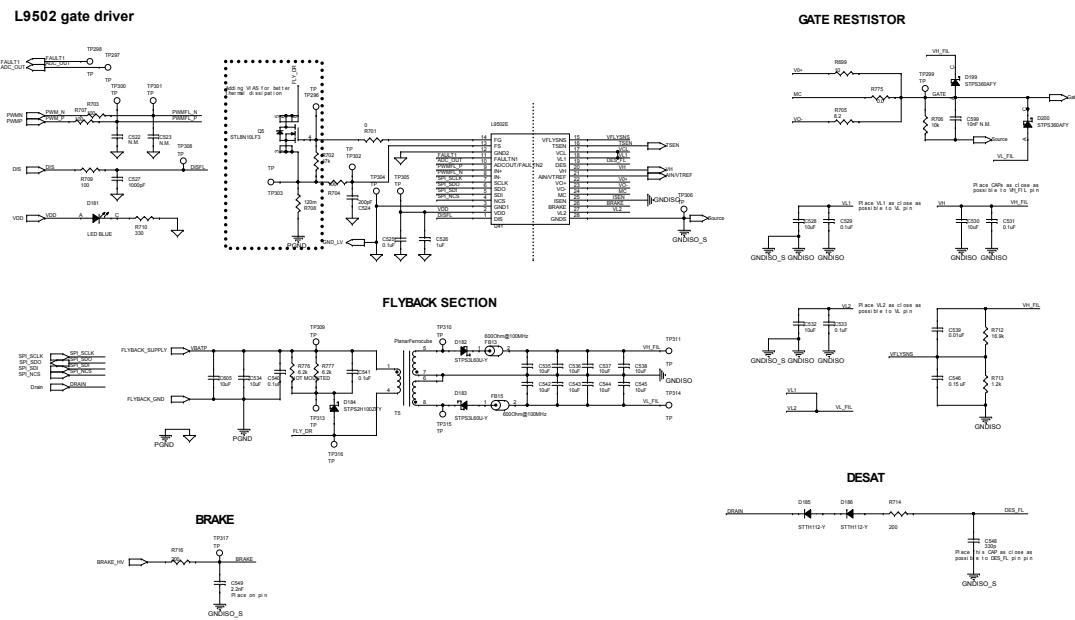
**Figure 3. STEVAL-APD03ACB circuit schematic (3 of 10)**


**Figure 4. STEVAL-APD03ACB circuit schematic (4 of 10)**

**Figure 5. STEVAL-APD03ACB circuit schematic (5 of 10)**


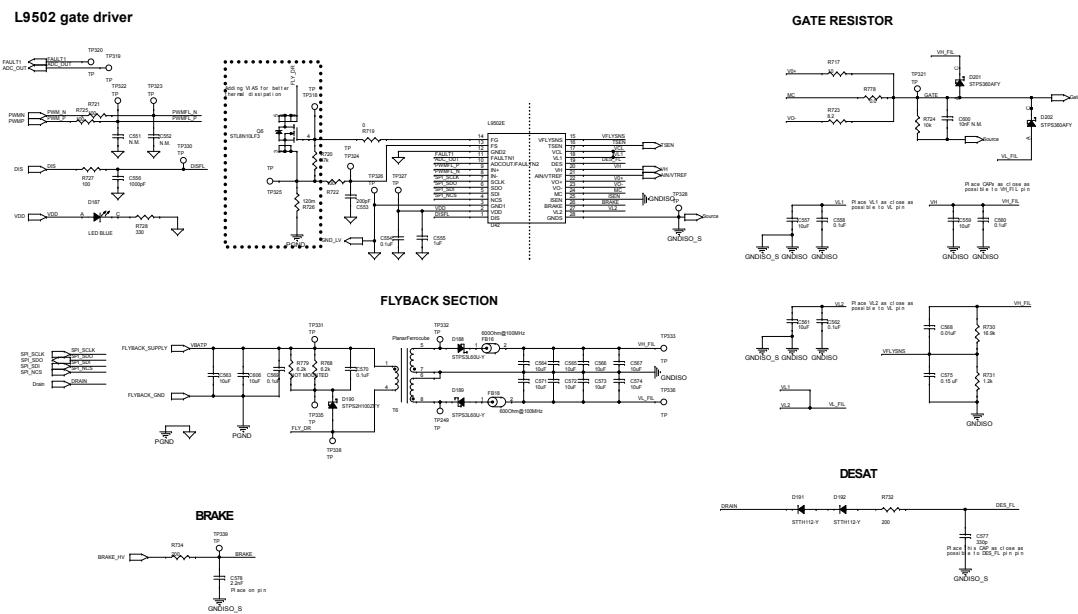
**Figure 6. STEVAL-APD03ACB circuit schematic (6 of 10)**



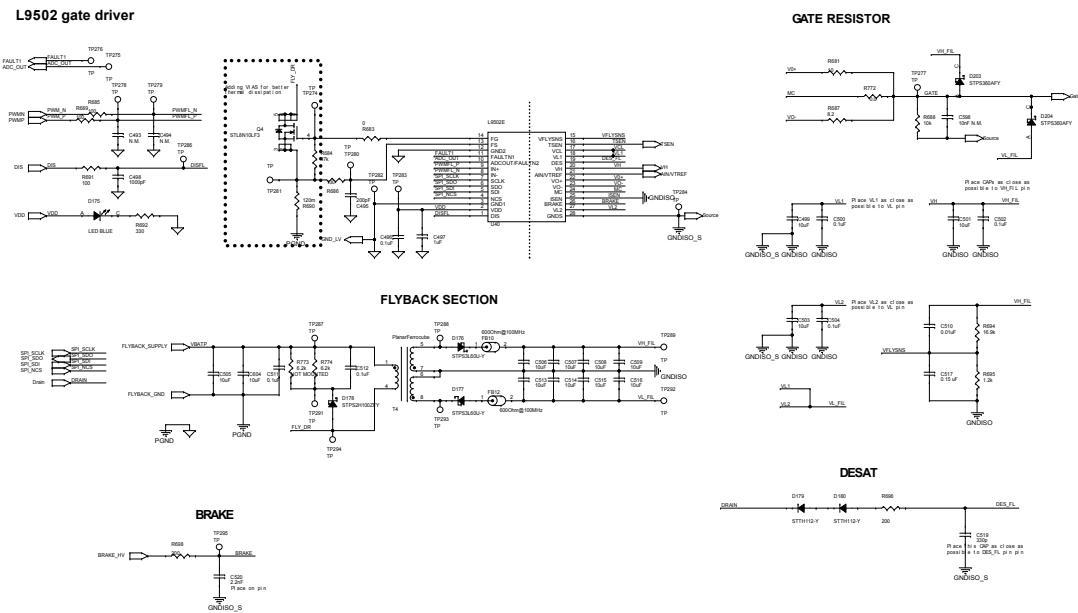
**Figure 7. STEVAL-APD03ACB circuit schematic (7 of 10)**



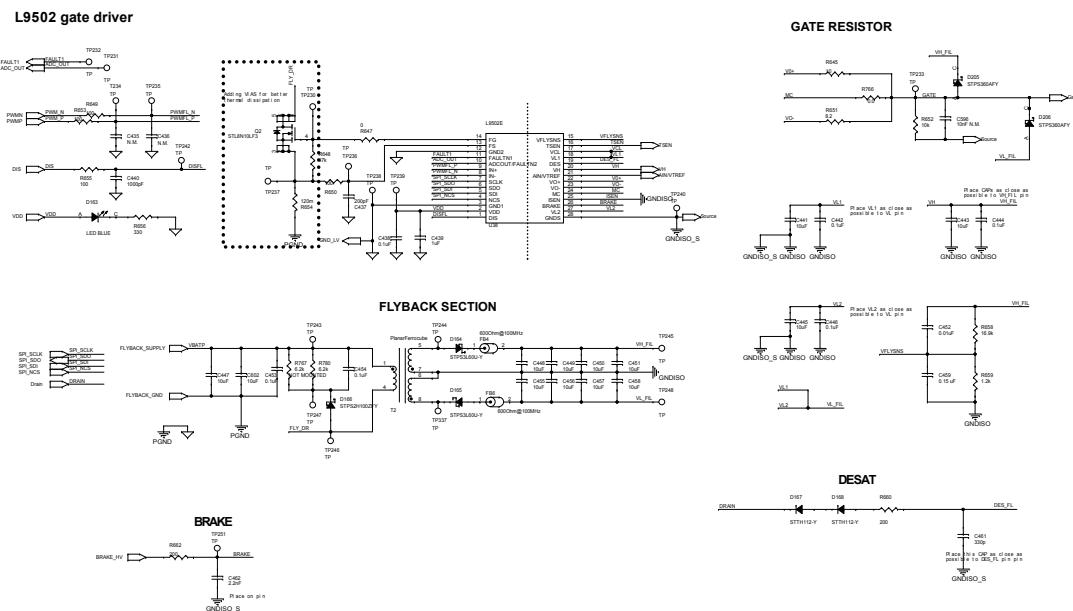
**Figure 8. STEVAL-APD03ACB circuit schematic (8 of 10)**



**Figure 9. STEVAL-APD03ACB circuit schematic (9 of 10)**



**Figure 10. STEVAL-APD03ACB circuit schematic (10 of 10)**



## 2 Custom evaluation boards information

**Notice:** *These evaluation boards are custom designed and built, in small quantities, according to specific requests from customers and are destined for evaluation and testing of ST products in a research and development setting. Please contact ST to provide your specific requests and get your custom built board(s).*

## Revision history

**Table 1. Document revision history**

Date	Revision	Changes
12-Sep-2024	1	Initial release.

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