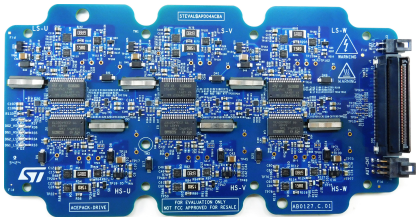
STEVAL-APD04ACB

Data brief

Gate driver board for traction inverter in EV/HEV applications



The picture shown is for illustration purpose only.
Actual product may vary depending on buyer's selection and availability.

Product summary	
Gate driver board for traction inverter in EV/ HEV applications	STEVAL-APD04ACB
SR5 E1 line of Stellar electrification MCUs, 32-bit Arm Cortex M7 automotive MCU 2x cores, 2 MB Flash, rich analog, high-resolution timer, HSM, ASIL-D	SR5E1E3
Applications	Automotive Motor Control

Features

- 12 V input voltage
- New motor control connector for supporting 3-phase motors or six phases and EESM
- Galvanically isolated driving stage with STGAP4S
- Fully optimized for ACEPACK DRIVE SiC module family (750 and 1200 V)
- Integrated controller for isolated flyback power supply allows to generate positive and negative gate driver supply voltages with few external components, enabling PCB space saving
- Protection functions such as the Miller clamp driver, desaturation and overcurrent detection, UVLO and OVLO are included to easily design high reliability systems
- Press fit connections for a high reliable and long-lasting connection
- Layout optimized with minimized stray inductances
- High reliability and robust

Description

The STEVAL-APD04ACB is an evaluation board evaluating the driving capabilities of the STGAP4S for ACEPACK DRIVE power module (compatible with both 750 and 1200 V) for automotive powertrain applications.

The driving section, hosting mainly the driver STGAP4S with flyback controller integrated to generate the driving voltages (+18/-5V).

This stage also hosts the planar transformer with embedded windings in the PCB layers to provide benefits in terms of mechanical dimensions, efficiency, and cost.

This board can be connected to the power module by means of a press fit insertion tool (design available on demand).

ST can offer a companion kit including HV DC bus cap, cooler for ACEPACK DRIVE with O ring, a three phase isolated current sensor with PCB adapter and flat cable based on customer needs and the relative selection of the ACEPACK DRIVE. Please contact ST office asking for STEVAL-APD001K2 custom-built solution.

The control section, not included in this board but available on www.st.com, should be separately ordered. This gate driver is compatible with the STEVAL-TTM007A hosting the SR5E1E3 (eTQFP100) which is a 2x 32-bit Arm® Cortex® -M7 with double precision FPU, L1 cache and DSP instructions with two cores in parallel or one core in lockstep configuration and the PMIC SPSB100. This microcontroller offers the best performance thanks to dedicated peripherals for motor control.

1 Schematic diagrams

Notice: These schematics are for illustration purpose only. Actual product may vary depending on buyer's selection and availability.

Figure 1. STEVAL-APD04ACB circuit schematic (1 of 10)

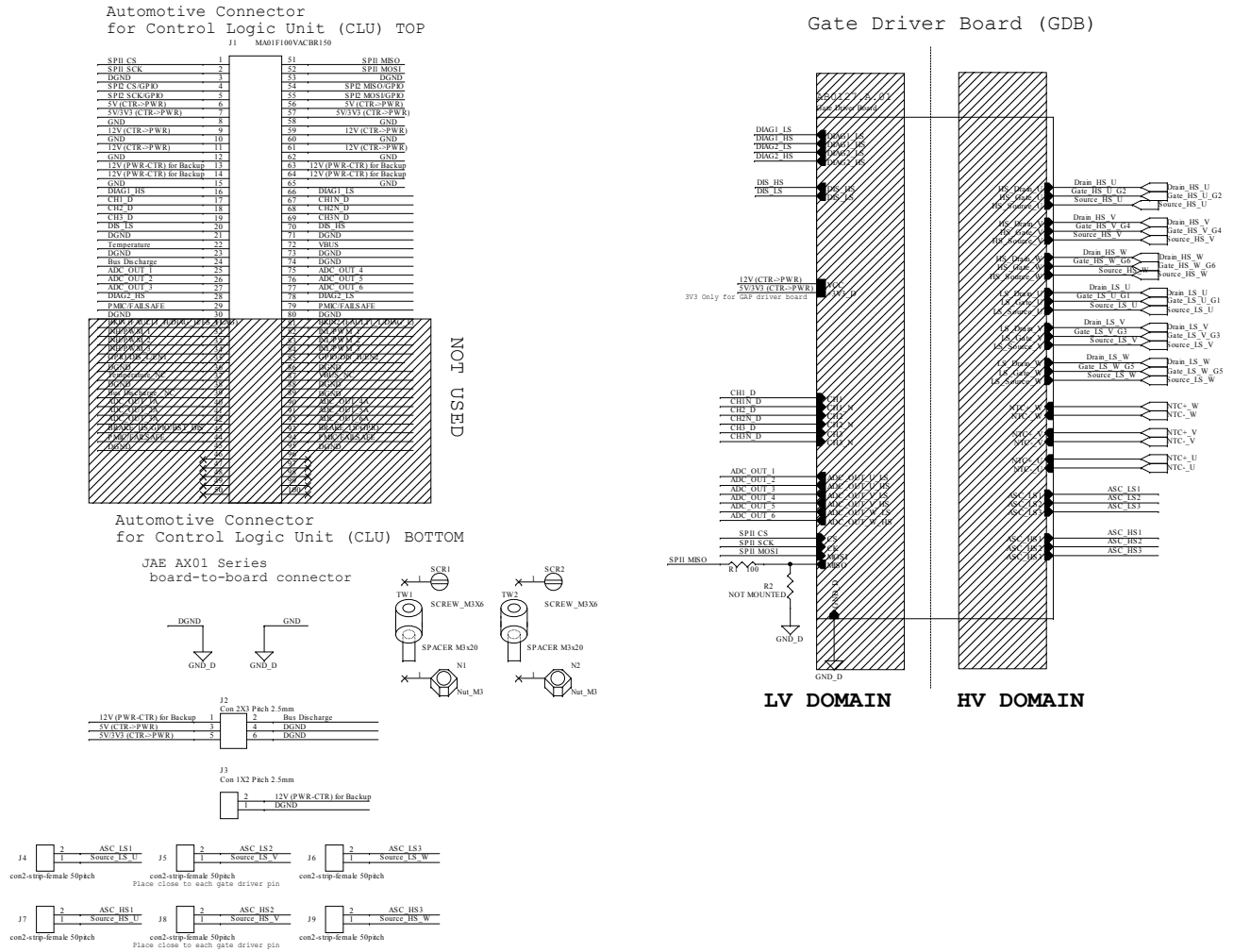
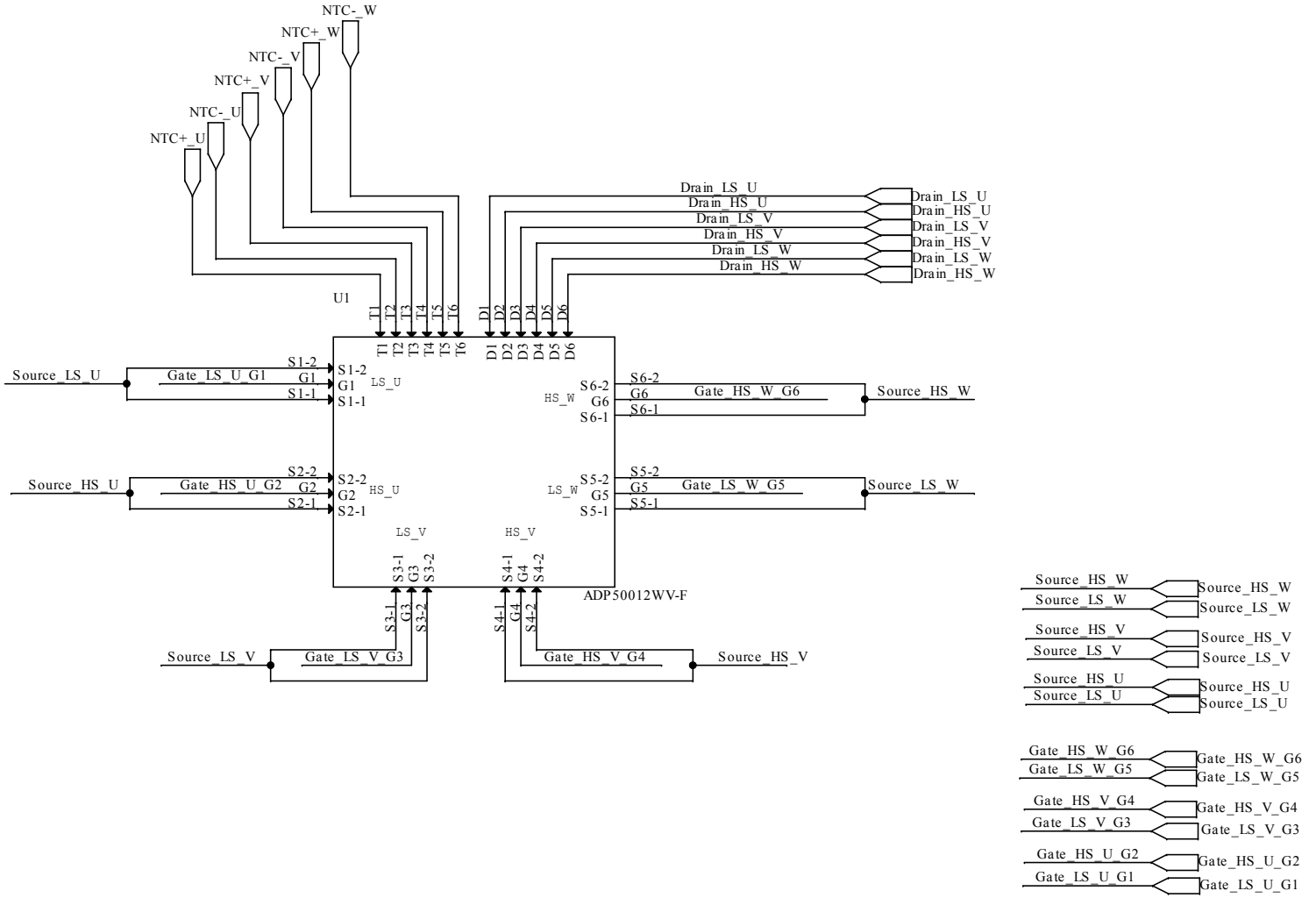


Figure 2. STEVAL-APD04ACB circuit schematic (2 of 10)



PLEASE TAKE CARE ABOUT POSITION OF COMPONENTS FAR FROM ACEPACK MODULE PIN ON TOP AN BOTTOM SIDE

Figure 3. STEVAL-APD04ACB circuit schematic (3 of 10)

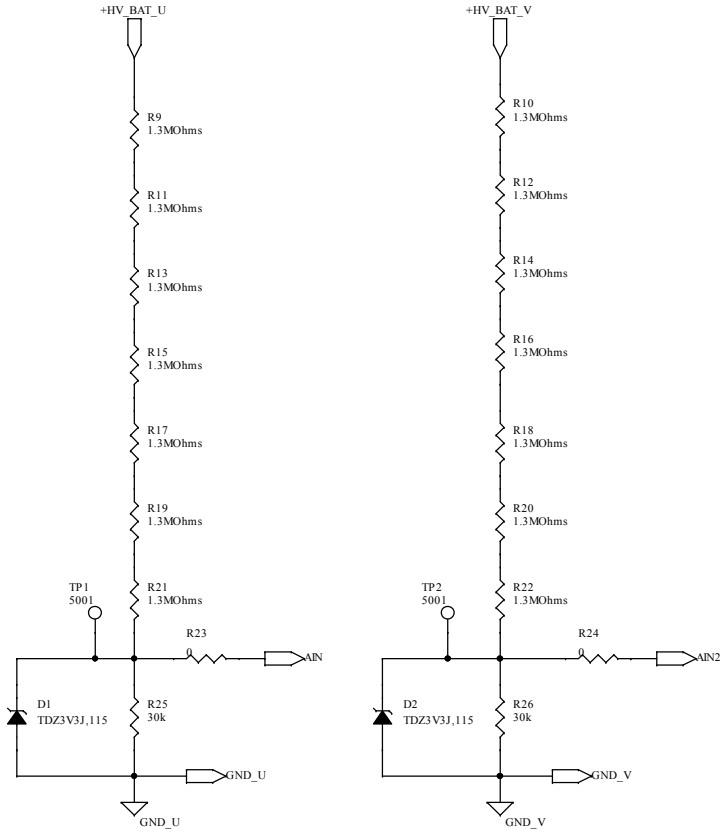


Figure 4. STEVAL-APD04ACB circuit schematic (4 of 10)

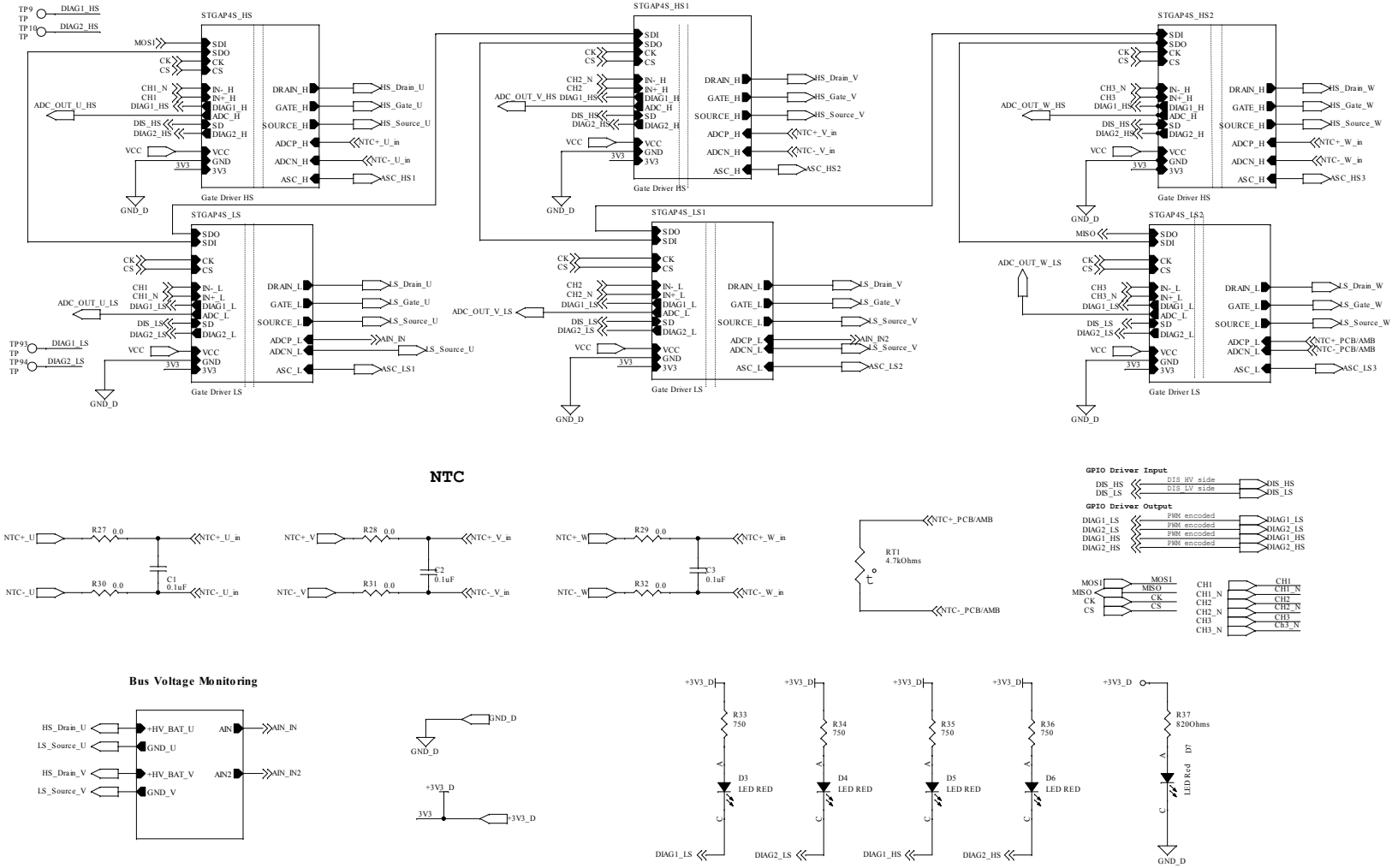


Figure 5. STEVAL-APD04ACB circuit schematic (5 of 10)

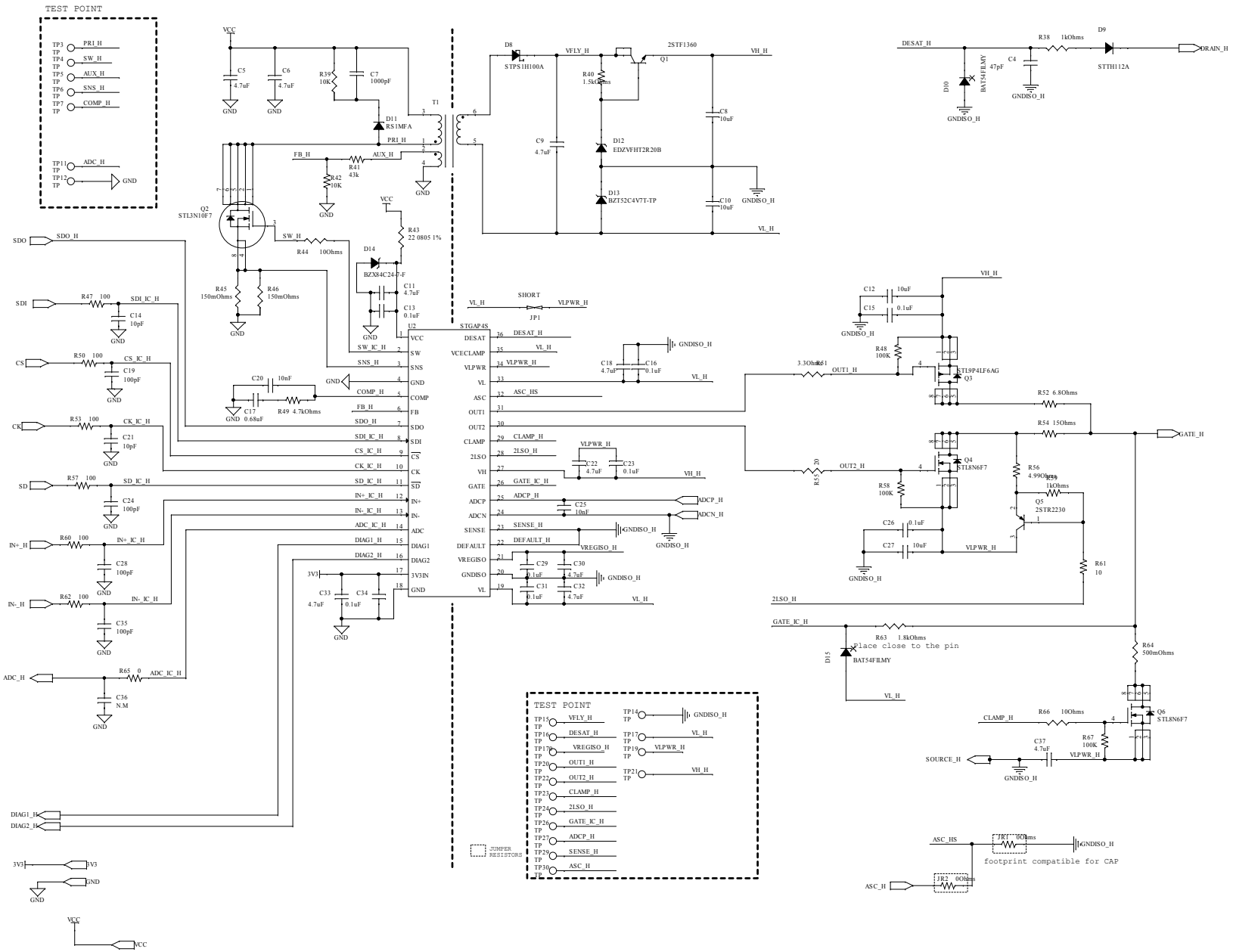


Figure 6. STEVAL-APD04ACB circuit schematic (6 of 10)

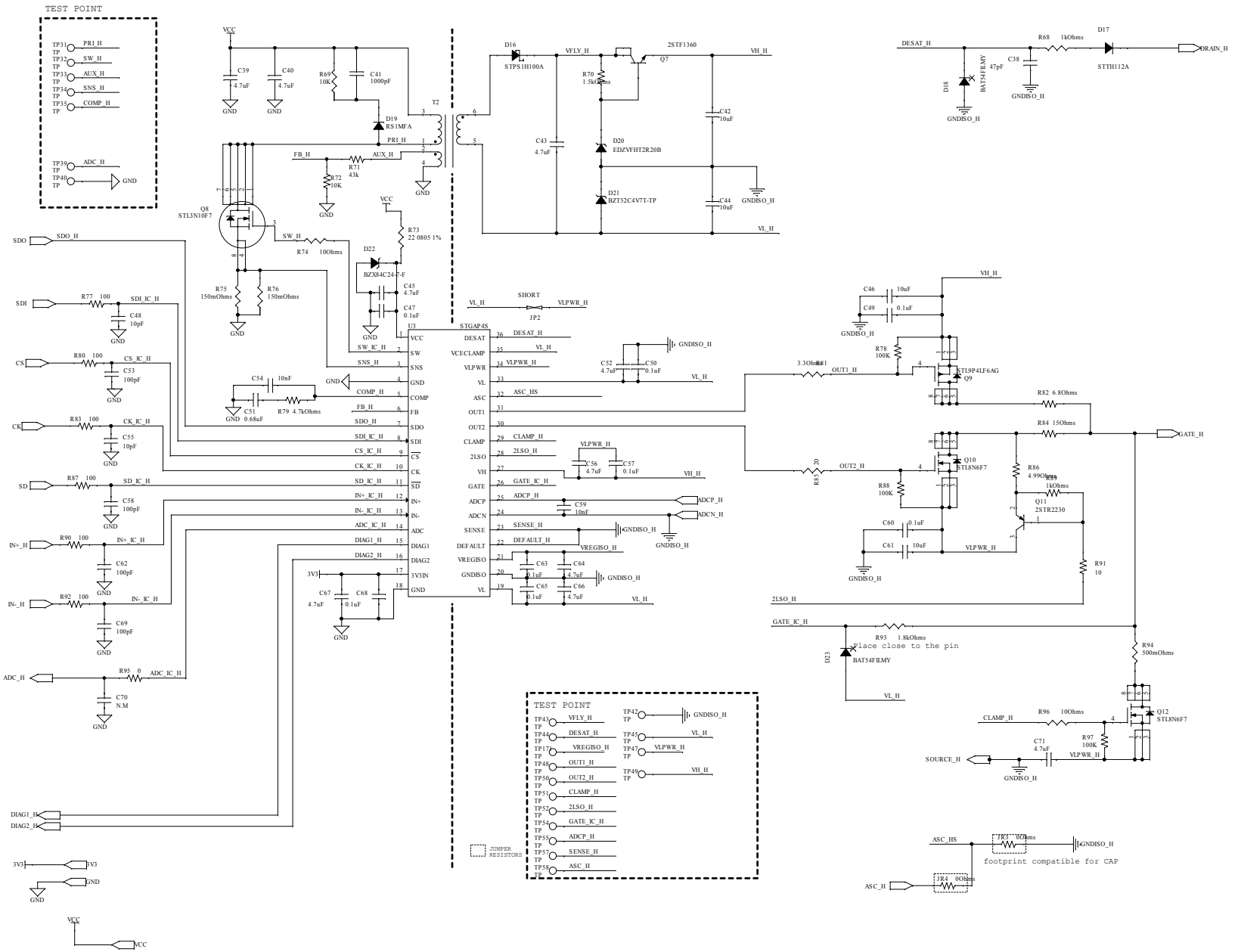


Figure 7. STEVAL-APD04ACB circuit schematic (7 of 10)

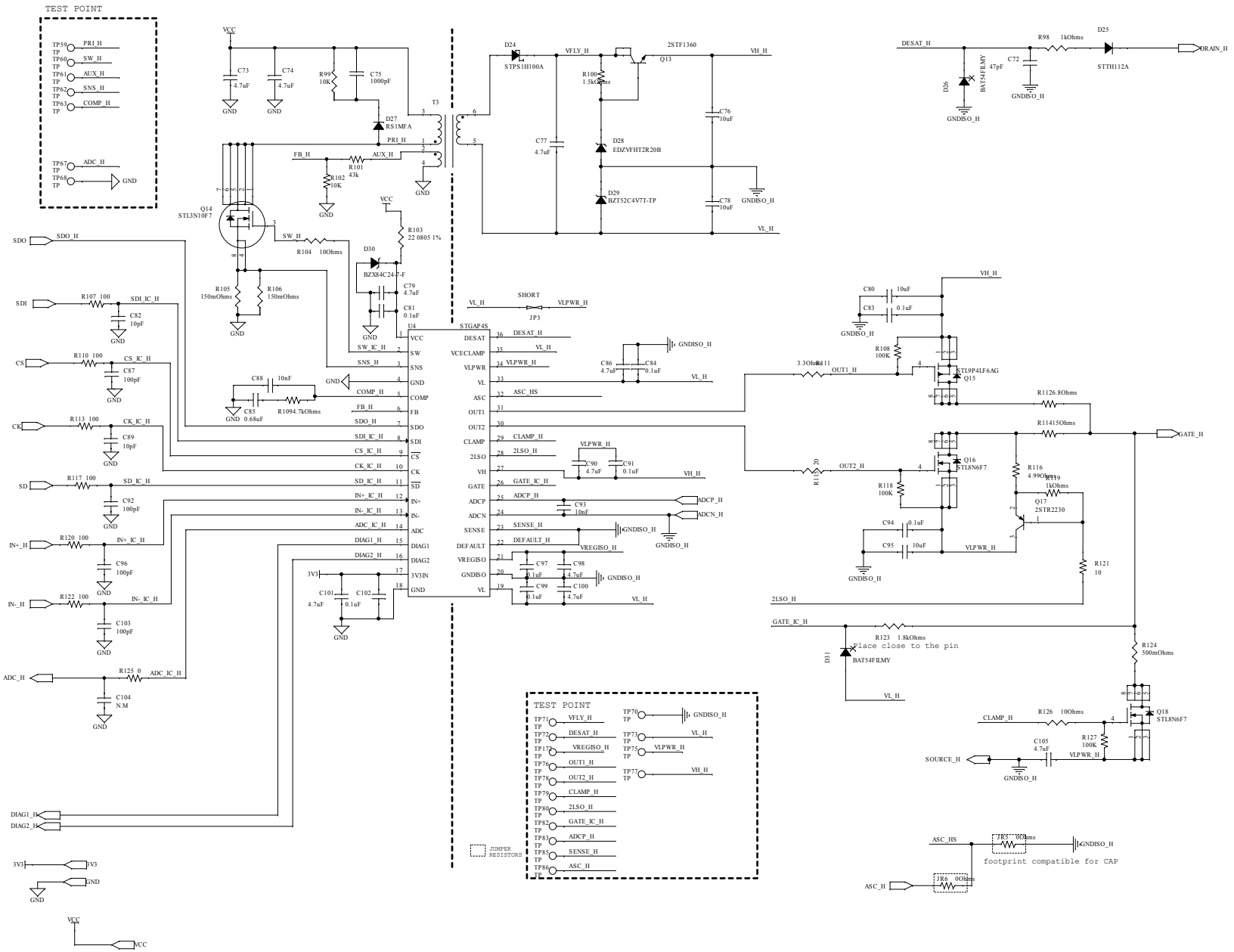


Figure 8. STEVAL-APD04ACB circuit schematic (8 of 10)

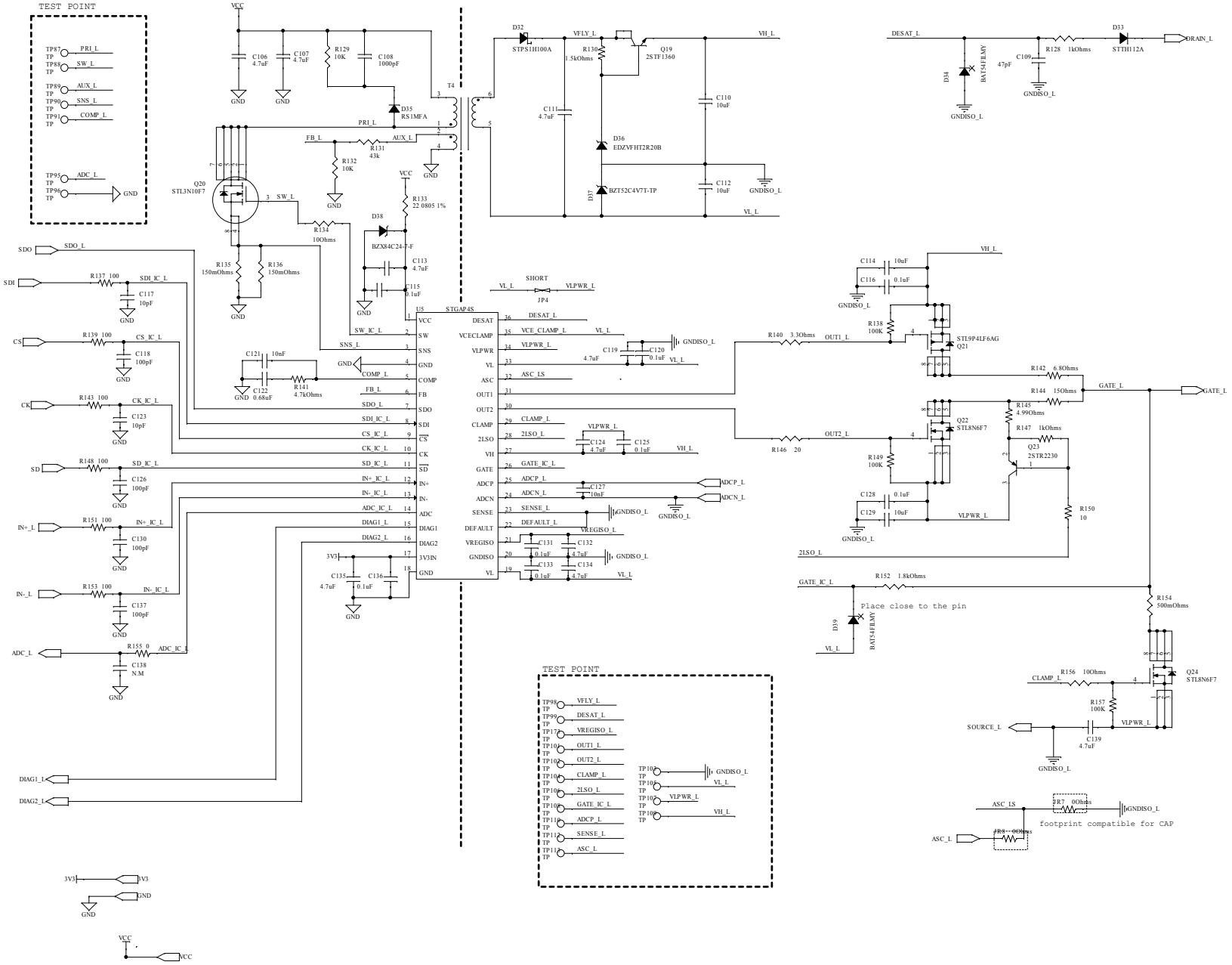


Figure 9. STEVAL-APD04ACB circuit schematic (9 of 10)

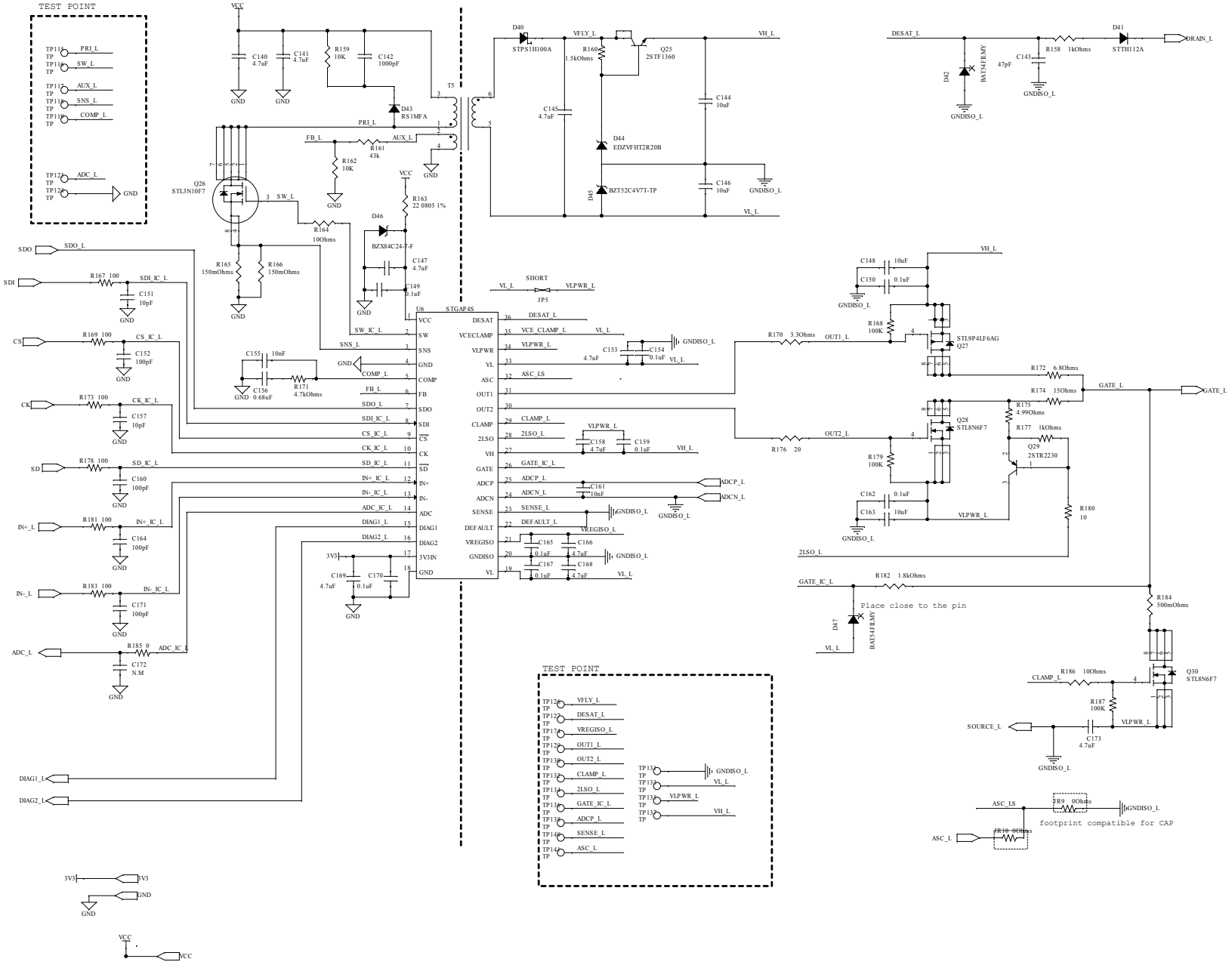
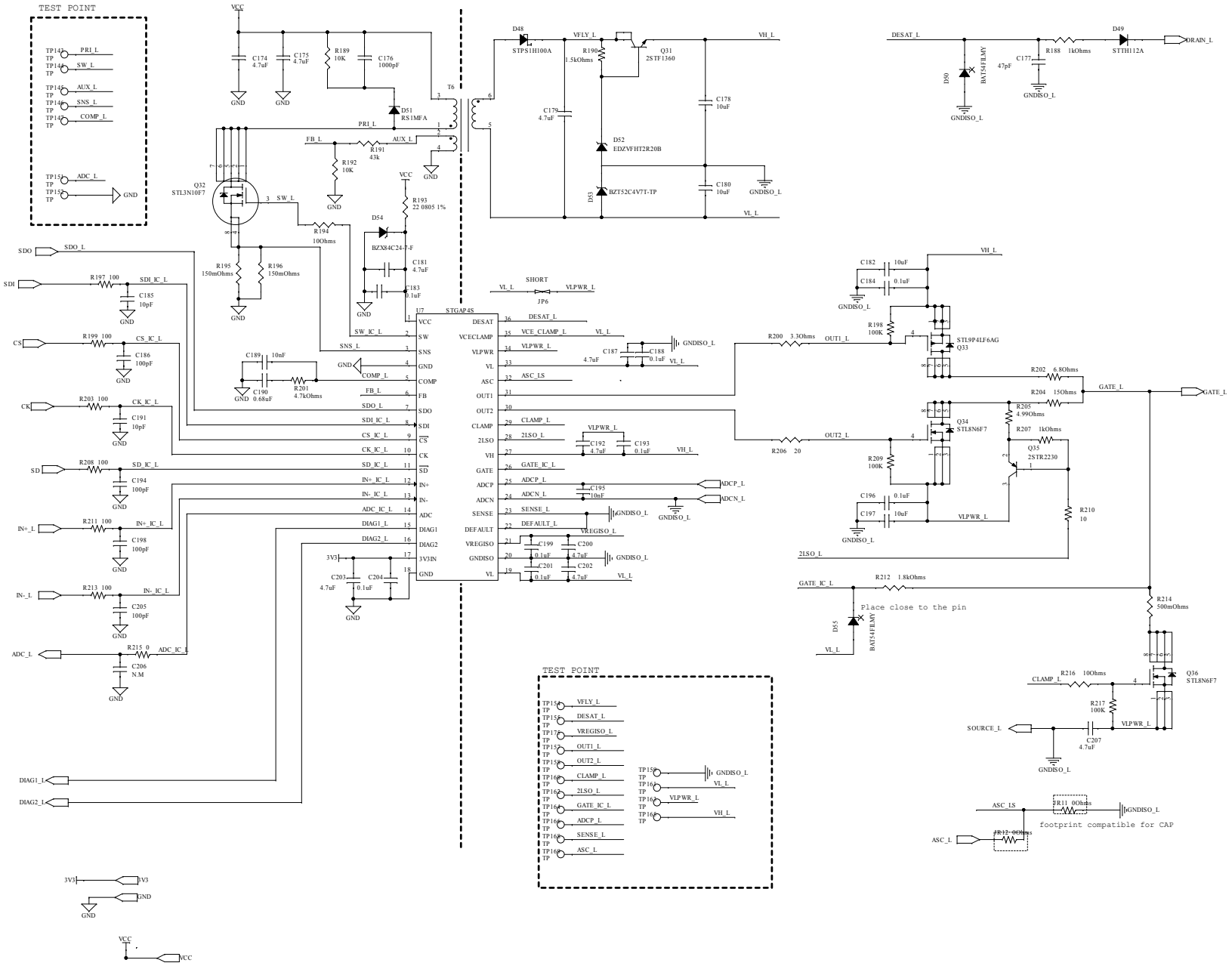


Figure 10. STEVAL-APD04ACB circuit schematic (10 of 10)



2 Custom evaluation boards information

Notice: *These evaluation boards are custom designed and built, in small quantities, according to specific requests from customers and are destined for evaluation and testing of ST products in a research and development setting. Please contact ST to provide your specific requests and get your custom built board(s).*

Revision history

Table 1. **Document revision history**

Date	Revision	Changes
30-Sep-2024	1	Initial release.

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