Embedded FW for three-phase full shunt electricity meter evaluation board based on STPMS2, STISO621 and STM32F413RH
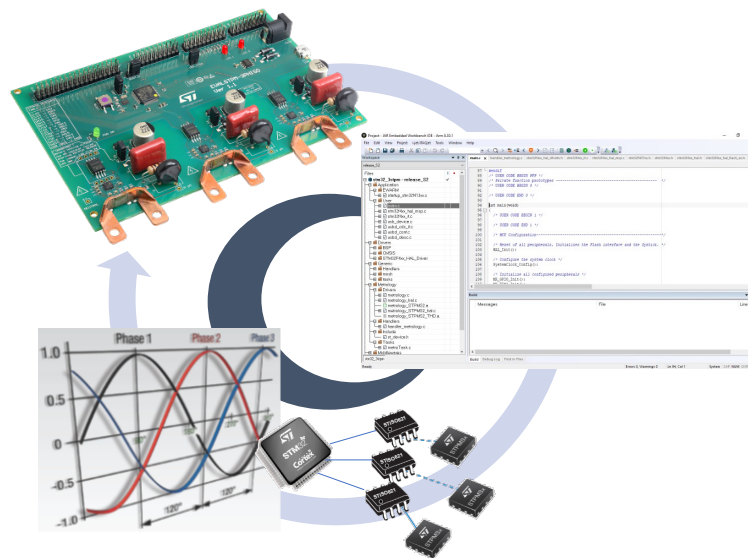

Product status link / summary

Product status link
STSW-STPM004
EVALSTPM-3PHISO
STPMS2
STISO621W
STM32F413RH

Features

- Three-phase metrology FW for STPMS2 sigma-delta modulator
- Implements hardware access layer to STPMS2 devices for signal acquisition of up to six channels (three-phases, each with voltage and current monitoring) @200 us
- Processing kernel implementing digital filtering of signals and data processing
- Provided full set of metrology registers, containing metrology measurements and calibration/configuration data
- Basic metrology application for a three-phase meter with scalable topology
- Active wideband, active fundamental, reactive and apparent power/energy calculation for each phase and cumulative
- Voltage and current channels decimated samples available
- 2.5 kHz measurement bandwidth
- RMS and THD (optional) calculation of each voltage and current signal
- Selectable high-pass filter for DC measurement
- Line period and phase shift measurement for each phase
- Phase voltage delays
- USB communication available through virtual com port mode

DB4340 - Rev 1 - December 2020
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Description

The STSW-STPM004 is embedded in the EVALSTPM-3PHISO evaluation board to implement a complete 3-phase energy meter with low-cost shunt current sensors.

The FW library implements a virtual six-channel STPM3x metrology device with:

- signal acquisition from up to six channels (three phases, each with voltage and current monitoring),

- a processing kernel implementing digital filtering of signals and data processing,

- a set of registers, containing metrology measurements and calibration/configuration data.

The FW exploits the DFSDM filters of the STM32F413RH to convert the six bitstreams into 24-bit voltage and current data, at 200 us rate. All the metrology parameters are computed in real time on a 200 us basis.

The STPM3x-like registers allow the application access to the virtual device (as 3xSTPM32 devices), which can be read/ configured by the hardware interface layer.

The FW also implements a virtual com port communication to easily access the internal parameters to read metrology data, to modify the internal configuration for a high flexibility of the application, and to calibrate the board.

Figure 1. FW architecture
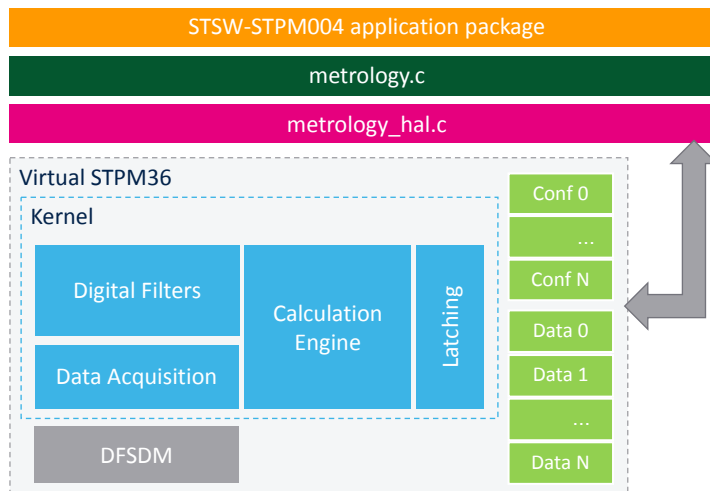
Revision history

Table 1. Document revision history

Date	Version	Changes
02-Dec-2020	1	Initial release.

IMPORTANT NOTICE – PLEASE READ CAREFULLY