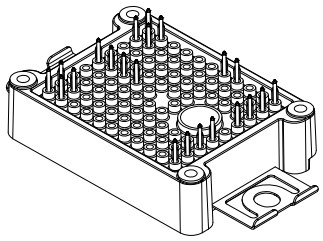
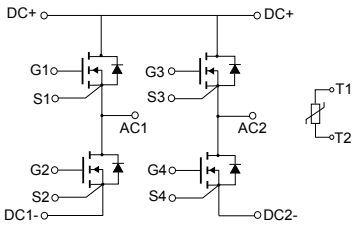
A1F25M12W2-F1

Datasheet

ACEPACK 1 power module, fourpack topology, 1200 V, 25 mΩ typ. SiC MOSFET gen.2 with NTC



ACEPACK 1



Features

- ACEPACK 1 power module:
  - DBC Cu-Al_2O_3-Cu based
  - Insulation voltage UL certified of 2.5 kVrms
  - Press-fit contact pins
- Fourpack topology:
  - 1200 V SiC MOSFET
  - $R_{DS(on)}$ typical 25 mΩ
  - Very high-power density
  - Very low switching energies
  - Switching characteristic almost independent from temperature
- Integrated NTC temperature sensor

Applications

- DC/DC converter
- High frequency switching application
- Welding

Description

This power module features a fourpack topology in an ACEPACK 1 module with NTC and integrates the most advanced silicon carbide MOSFETs of STMicroelectronics which are represented by the gen.2 technology. This modular solution can be used to realize complex topologies characterized by very high power density in order to meet the higest efficiency requirements.

Product status link
A1F25M12W2-F1

Product summary	
Order code	A1F25M12W2-F1
Marking	A1F25M12W2-F1
Package	ACEPACK 1
Packing	Tray
Leads type	Press-fit

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	1200	V
V_{GS}	Gate-source voltage	-10 to 22	V
	Gate-source voltage, recommended operating values	-5 to 18	V
I_D	Drain current (continuous) at T_H = 25 °C	50	A
I_{DP}(1)	Pulsed drain current	100	A
T_J	Maximum junction temperature	175	°C
	Operating junction temperature range under switching conditions	-40 to 150	°C

1. *Pulse width limited by maximum junction temperature.*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJH}	Thermal resistance, junction-to-heat sink, each MOSFET, λ = 3 W · m^{-1} · $°C^{-1}$	1.18	°C/W

2 Electrical characteristics

T_J = 25 °C unless otherwise specified.

Table 3. Electrical characteristics per switch

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$R_{DS(on)}$ (1)	Static drain-source on resistance	V_{GS} = 18 V , I_D = 50 A		25	34	mΩ
		V_{GS} = 18 V , I_D = 50 A,T_J = 150 °C		45		
$V_{GS(th)}$	Gate threshold voltage	I_D = 5 mA, V_{DS} = V_{GS}	1.9	3	4.9	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 1200 V, V_{GS} = 0 V			100	µA
I_{GSS}	Gate-body leakage current	V_{DS} = 0, V_{GS} = 22 V			500	nA
C_{iss}	Input capacitance	f = 1 MHz, V_{DS} = 800 V, V_{GS} = 0 V		3500		pF
C_{oss}	Output capacitance			180		pF
C_{rss}	Reverse transfer capacitance			30		pF
R_g	Intrinsic gate resistance	f = 1 MHz, I_D = 0 A		2		Ω
Q_g	Total gate charge	V_{DD} = 800 V, V_{GS} = -5 to 18 V, I_D = 50 A		147		nC
Q_{gs}	Gate charge gate-source			33		nC
Q_{gd}	Gate charge gate drain			54		nC

1. *The $R_{DS(on)}$ value does not take into account the additional lead resistance R_S, refer to Table 7. ACEPACK 1 package for details.*

Table 4. Switching energy

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t_{on}	Turn-on time	V_{DD} = 600 V, I_D = 50 A, V_{GS} = -5 to 18 V, di/dt = 4.4 A/ns, $R_{g(on)}$ = 4.7 Ω, $R_{g(off)}$ = 1 Ω	-	24	-	ns
$t_{c(on)}$	Crossover time on		-	26	-	ns
E_{on} (1)	Turn-on switching energy		-	0.554	-	mJ
t_{off}	Turn-off time	V_{DD} = 600 V, I_D = 50 A, V_{GS} = -5 to 18 V, dv/dt = 64 V/ns, $R_{g(on)}$ = 4.7 Ω, $R_{g(off)}$ = 1 Ω	-	32	-	ns
$t_{c(off)}$	Crossover time off		-	11	-	ns
E_{off} (1)	Turn-off switching energy		-	0.095	-	mJ
t_{on}	Turn-on time	V_{DD} = 600 V, I_D = 50 A, V_{GS} = -5 to 18 V, di/dt = 4.7 A/ns, $R_{g(on)}$ = 4.7 Ω, $R_{g(off)}$ = 1 Ω, T_J = 150 °C	-	25	-	ns
$t_{c(on)}$	Crossover time on		-	25	-	ns
E_{on} (1)	Turn-on switching energy		-	0.548	-	mJ
t_{off}	Turn-off time	V_{DD} = 600 V, I_D = 50 A,V_{GS} = -5 to 18 V, dv/dt = 70 V/ns, $R_{g(on)}$ = 4.7 Ω, $R_{g(off)}$ = 1 Ω, T_J = 150 °C	-	34	-	ns
$t_{c(off)}$	Crossover time off		-	11	-	ns
E_{off} (1)	Turn-off switching energy		-	0.081	-	mJ

1. *Using active miller clamp circuit.*

Table 5. Electrical characteristics, source drain diode per switch

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{SD}	Forward on voltage drop	V_{GS} = 0 V, I_{SD} = 50 A	-	2.9	-	V
t_{rr}	Reverse recovery time	V_{DD}=600 V, I_F=50 A, $R_{g(on)}$=4.7 Ω, $R_{g\ (passive)}$=0 Ω, V_{GS} = -5 to 18 V	-	21.9	-	ns
Q_{rr}	Reverse recovery energy		-	1034	-	nC
I_{RRM}	Reverse recovery current		-	80	-	A
E_{rec}	Reverse recovery energy		-	367	-	µJ

2.1 Electrical characteristics (curves)

Figure 1. Typical output characteristics (T_J = -40 °C)

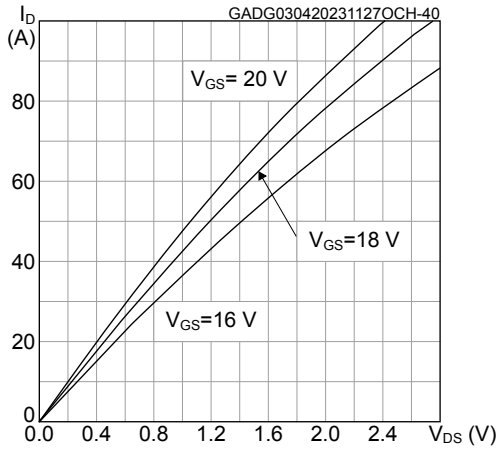


Figure 2. Typical output characteristics (T_J = 25 °C)

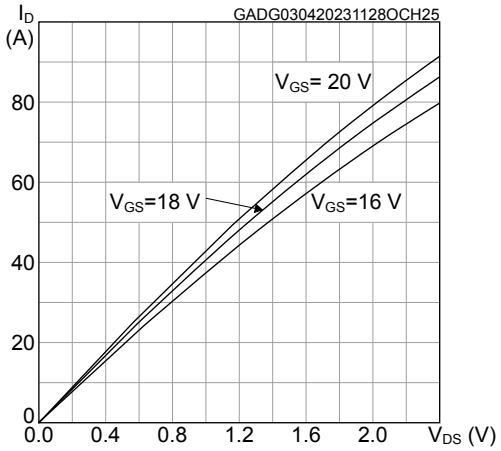


Figure 3. Typical output characteristics (T_J = 150 °C)

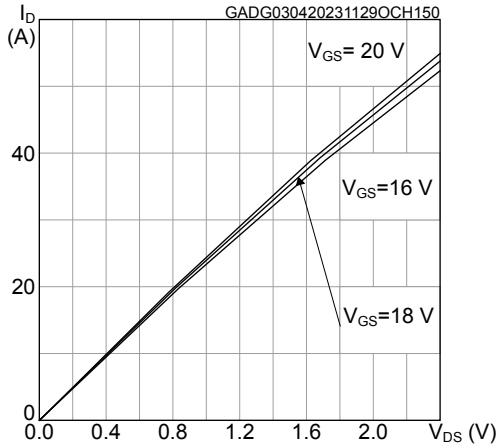


Figure 4. Typical transfer characteristics

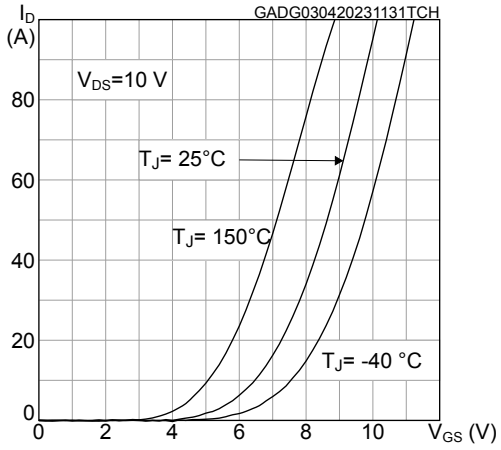


Figure 5. Typical diode foward characteristics (terminal)

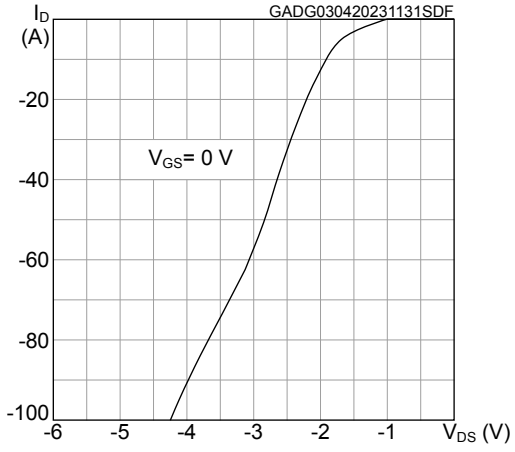


Figure 6. Typical gate charge characteristics

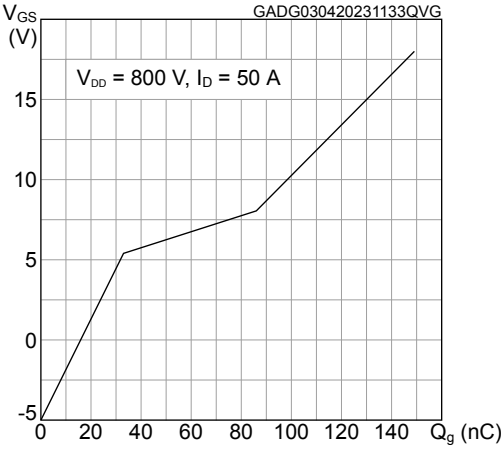


Figure 7. Typical switching energy vs drain current (T_J = 25 °C)

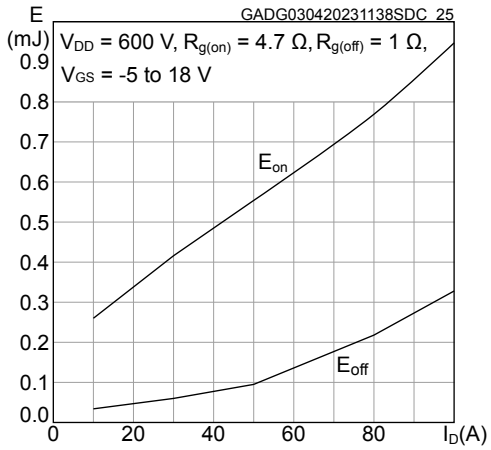


Figure 8. Typical switching energy vs drain current (T_J = 150 °C)

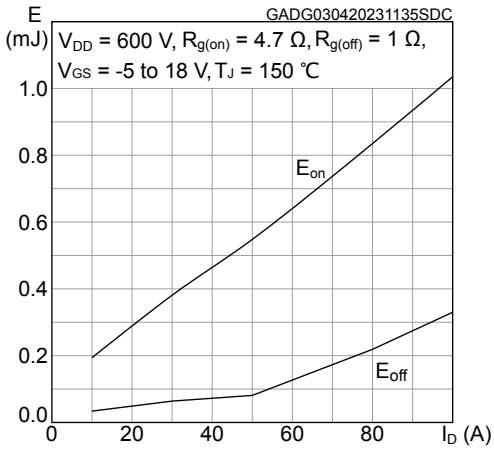


Figure 9. Typical switching energy vs gate resistance (T_J = 25 °C)

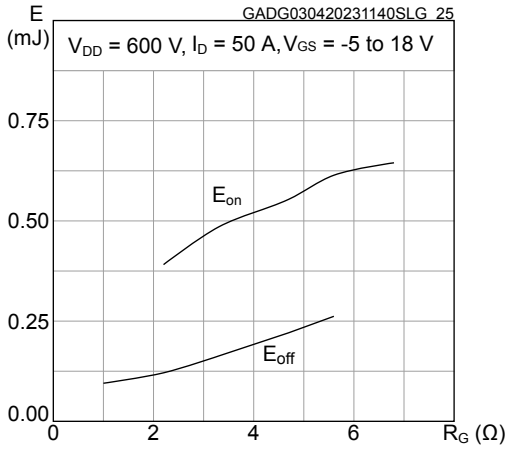


Figure 10. Typical switching energy vs gate resistance (T_J = 150 °C)

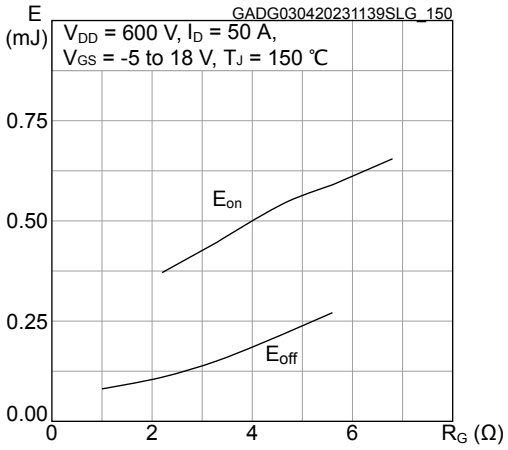


Figure 11. Typical switching energy vs temperature

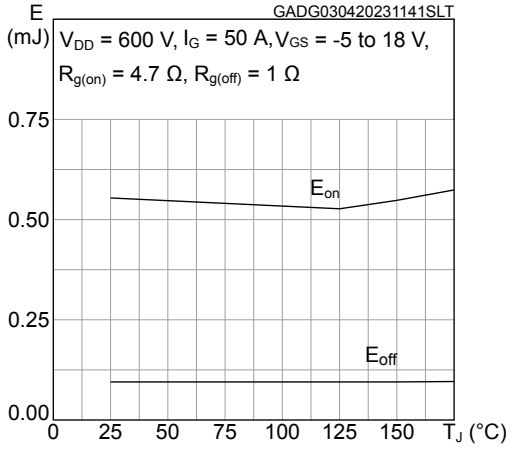


Figure 12. Typical switching energy vs V_{GS} (T_J = 25 °C)

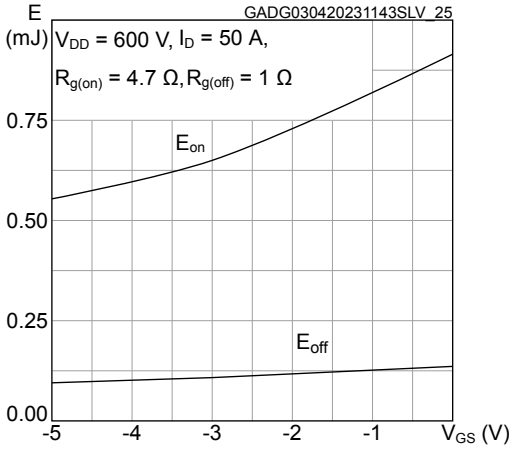


Figure 13. Typical switching energy vs V_{GS} (T_J = 150 °C)

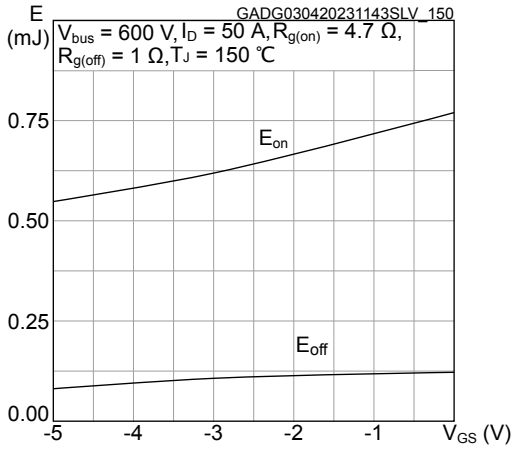
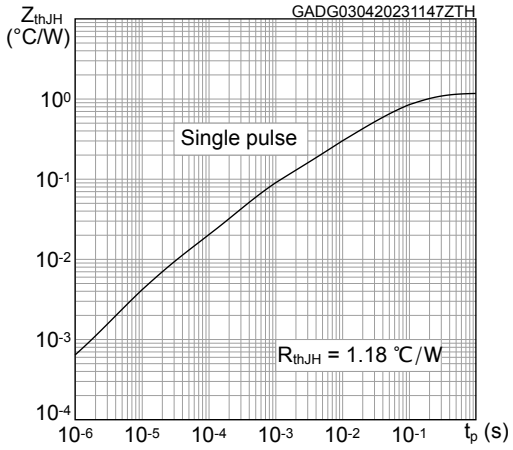


Figure 14. Maximum transient thermal impedance



3 NTC

Table 6. Absolute maximum ratings for NTC temperature sensor, considered as stand-alone

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
R_{25}	Resistance rating	T = 25 °C		5		kΩ
R_{100}	Resistance rating	T = 100 °C		493		Ω
$\Delta R_{100}/R$	Resistance tolerance		-5		5	%
B	B value	T = 25 to 50 °C		3375		K
		T = 25 to 85 °C		3411		
T	Operating temperature range		-40		150	°C

Figure 15. NTC typical resistance vs temperature

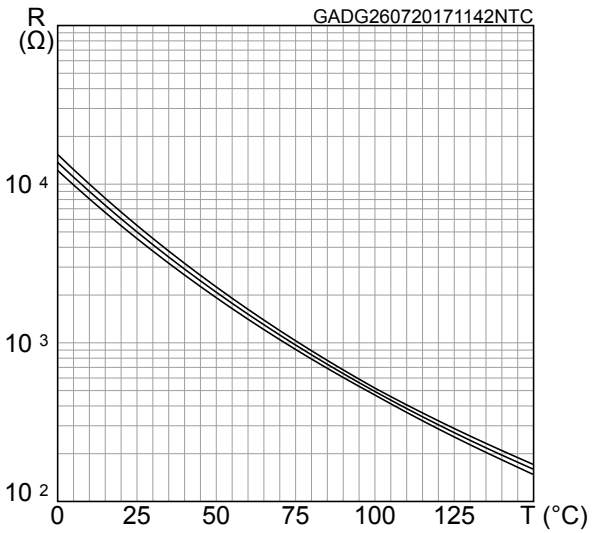
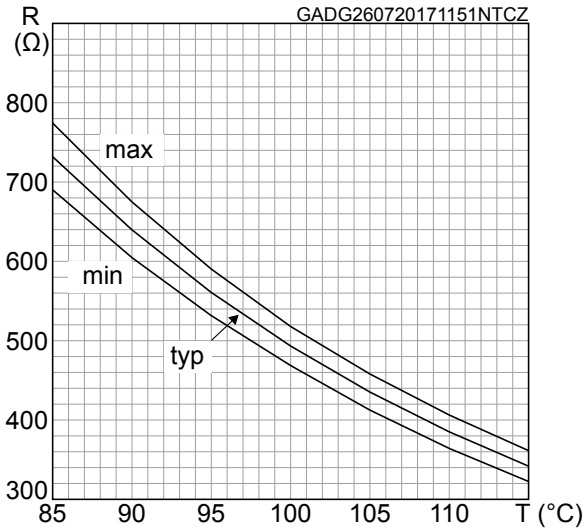


Figure 16. NTC resistance vs temperature, zoom



4 Package

Table 7. **ACEPACK 1 package**

Symbol	Parameter	Value	Unit
V_{ISO}	Isolation withstand voltage applied between each pin and heat sink plate (AC voltage, t = 60 s)	2.5	kV
CTI	Comparative tracking index	200	V
L_s	Stray inductance module loop	10	nH
R_s	Module lead resistance, terminals to chip	1	mΩ
T_{stg}	Storage temperature range	-40 to 125	°C

5 Electrical topology and pin description

Figure 17. **Electrical topology and pin description**

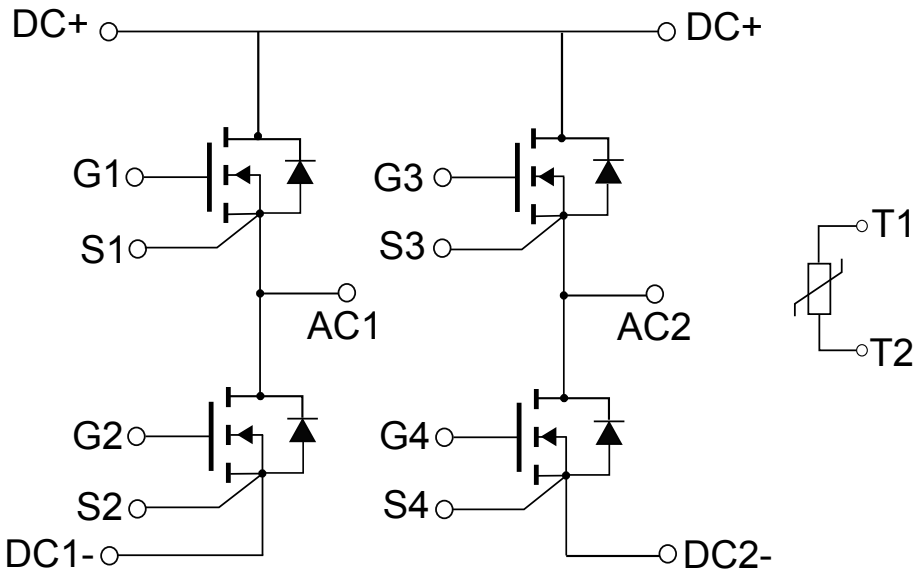
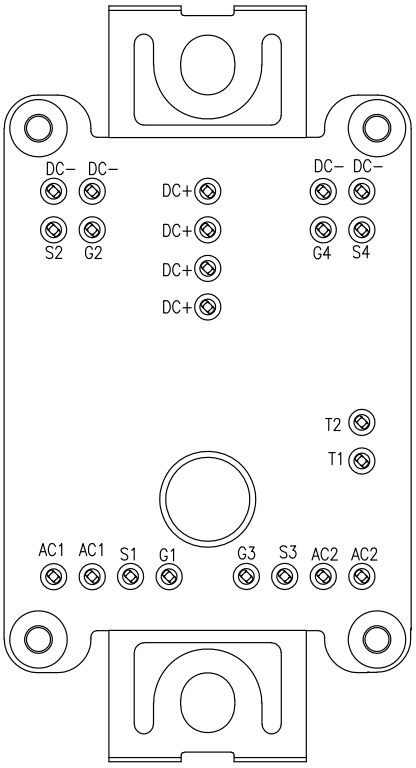


Figure 18. **Package top view with pinout**



8569715_Rev10_fourpack_pinout

6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

6.1 ACEPACK 1 fourpack press-fit package information

Figure 19. ACEPACK 1 fourpack press-fit package outline (dimensions are in mm)

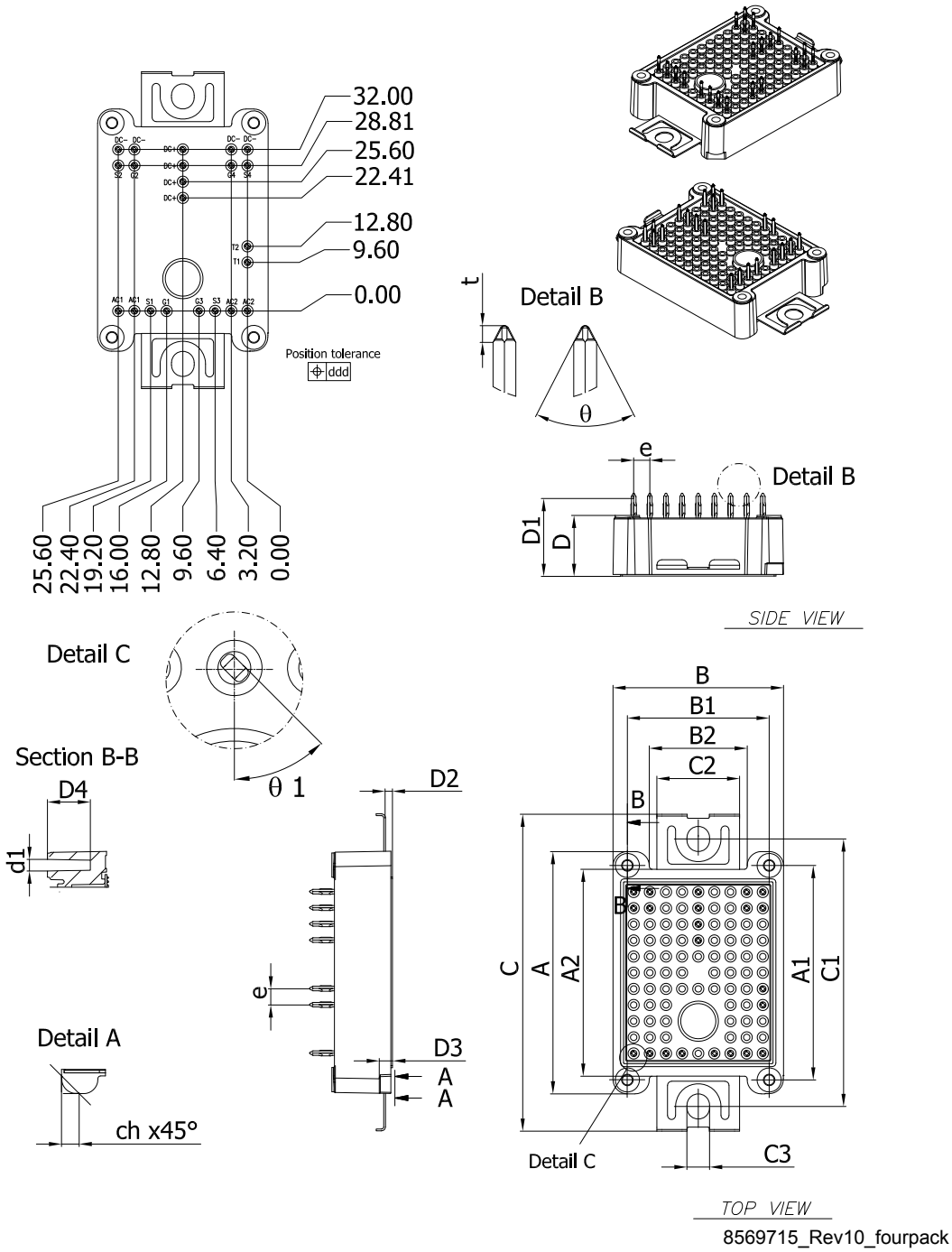
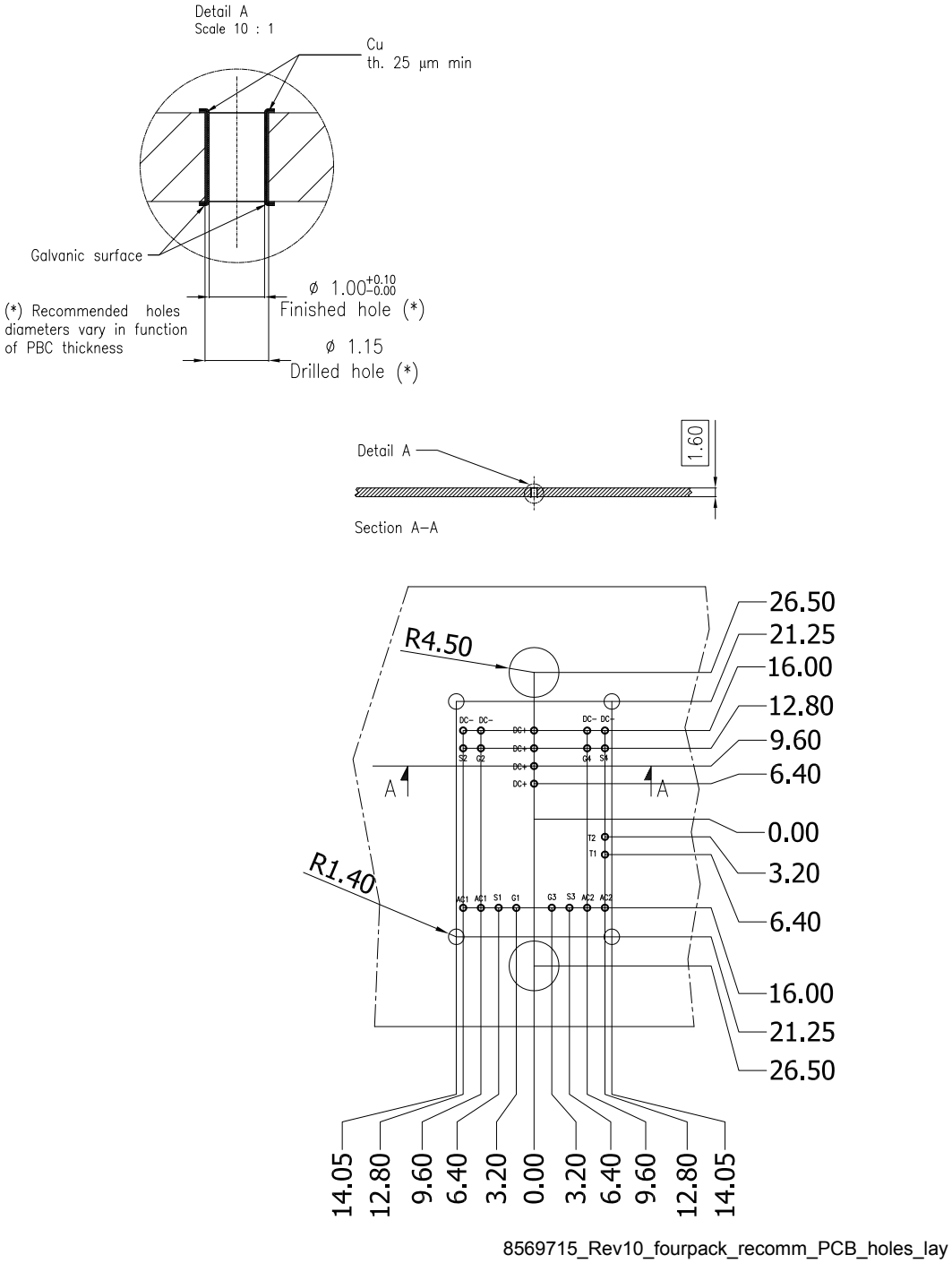


Table 8. ACEPACK 1 fourpack press-fit package mechanical data

Ref.	mm		
	Min.	Typ.	Max.
A	47.70	48.00	48.30
A1	42.30	42.50	42.70
A2	40.80	41.00	41.20
B	33.50	33.80	34.10
B1	27.90	28.10	28.30
B2	19.20	19.40	19.60
C	62.30	62.80	63.30
C1	52.90	53.00	53.10
C2	16.20	16.40	16.60
C3	4.40	4.50	4.60
D	11.65	12.00	12.35
D1	15.90	16.40	16.90
D2	1.10	1.30	1.50
D3	2.30	2.50	2.70
D4			8.50
t	0.30	0.40	0.50
θ	52°	60°	68°
θ1		45°	
ddd	Checked with pin gauge		
e	3.20 BSC		
d1	2.30 REF		
ch	3.50 REF		

Figure 20. ACEPACK 1 fourpack press-fit PCB holes layout (dimensions are in mm)



Revision history

Table 9. **Document revision history**

Date	Version	Changes
13-Oct-2020	1	First release.
04-Nov-2021	2	Updated topology name throughout the document. Updated *Section 1 Electrical ratings*. Updated *Section 3 NTC*. Updated *Figure 5. Package top view with pinout*. Updated *Section 6 Package information*. Minor text changes.
10-Jun-2022	3	Updated *Section 6.1 ACEPACK 1 fourpack press-fit package information.* Minor text changes.
28-Apr-2023	4	Modified $R_{DS(on)}$ typical value in Features Modified Table 2. Thermal data and Table 3. Electrical characteristics per switch Added Table 4. Switching energy Modified Table 5. Electrical characteristics, source drain diode per switch Added Section 2.1 Electrical characteristics (curves) Modified Table 7. ACEPACK 1 package Minor text changes.

Contents

IMPORTANT NOTICE – READ CAREFULLY

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgment.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, refer to www.st.com/trademarks. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.