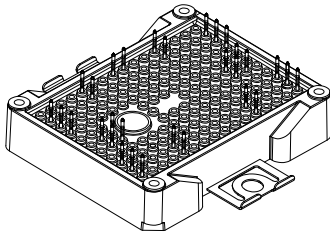
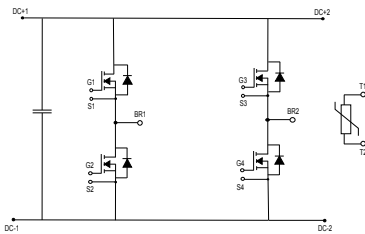


## ACEPACK 2 power module, fourpack topology, 650 V, 23 mΩ typ. SiC Power MOSFET gen.3 with NTC and capacitance


**ACEPACK 2**


### Features

- Fourpack topology
- ACEPACK 2 power module
  - 23 mΩ of typical  $R_{DS(on)}$  each switch
  - Insulation voltage 2.5 kVrms
  - Integrated NTC temperature sensor
  - Integrated DC link capacitor
  - DBC Cu-Al<sub>2</sub>O<sub>3</sub>-Cu based
  - Press-fit contact pins

### Applications

- DC-DC converters
- Solar inverters

### Description

This power module realizes a fourpack topology in an ACEPACK 2 module with NTC and capacitance, integrating the latest advances in silicon carbide MOSFETs from STMicroelectronics, represented by third generation technology. This modular solution is used to realize complex topologies with very high power density and efficiency requirements.



#### Product status link

[A2F20M65W3-FC](#)

#### Product summary

<b>Order code</b>	A2F20M65W3-FC
<b>Marking</b>	A2F20M65W3-FC
<b>Package</b>	ACEPACK 2
<b>Leads type</b>	Press-fit
<b>Packing</b>	Tray

## 1 Electrical rating

$T_J = 25\text{ °C}$  unless otherwise specified.

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	650	V
$V_{GS}$	Gate-source voltage	-10 to 22	V
	Gate-source voltage, recommended operating values	-5 to 18	
$I_D$	Drain current (continuous) at $T_H = 25\text{ °C}$	58	A
$I_{DM}^{(1)}$	Pulsed peak drain current	155	A
$T_J$	Maximum junction temperature	150	°C
	Operating junction temperature range under switching conditions	-40 to 150	

1. Current referred to 1 ms time pulse.

**Table 2. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thJH}$	Thermal resistance, junction-to-heat sink ( $TIM = 120\text{ }\mu\text{m}$ , $\lambda = 3\text{ W}\cdot\text{m}^{-1}\cdot\text{°C}^{-1}$ )	0.98	°C/W

## 2 Electrical characteristics

**Table 3. On/off-state**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 18\text{ V}$ , $I_D = 32\text{ A}$		23	34.5	m $\Omega$
		$V_{GS} = 18\text{ V}$ , $I_D = 32\text{ A}$ , $T_J = 150\text{ }^\circ\text{C}$		28		
$V_{GS(th)}$	Gate threshold voltage	$I_D = 10\text{ mA}$ , $V_{DS} = V_{GS}$	1.8	3.1	4.2	V
$I_{DSS}$	Zero gate voltage drain current	$V_{DS} = 650\text{ V}$ , $V_{GS} = 0\text{ V}$			20	$\mu\text{A}$
$I_{GSS}$	Gate-body leakage current	$V_{DS} = 0$ , $V_{GS} = -10\text{ to }22\text{ V}$			100	nA
$C_{iss}$	Input capacitance			1840		pF
$C_{oss}$	Output capacitance	$f = 1\text{ MHz}$ , $V_{DS} = 400\text{ V}$ , $V_{GS} = 0\text{ V}$		188		pF
$C_{rss}$	Reverse transfer capacitance			26		pF
$Q_g$	Total gate charge	$V_{DD} = 400\text{ V}$ , $V_{GS} = -5\text{ to }18\text{ V}$ , $I_D = 20\text{ A}$		79		nC
$Q_{gs}$	Gate-source charge			23		nC
$Q_{gd}$	Gate-drain charge			29		nC

**Table 4. Switching energy**

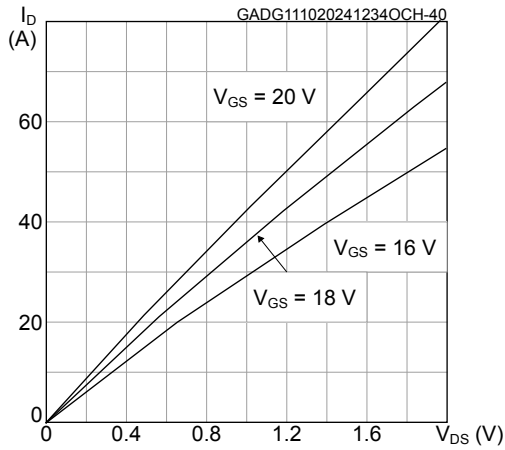
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$dv/dt$	On	$V_{DS} = 400\text{ V}$ , $I_D = 30\text{ A}$ ,	-	16.12	-	V/ns
	Off	$V_{GS} = -5\text{ to }18\text{ V}$ , $R_{G(on)} = 6.8\text{ }\Omega$ $R_{G(off)} = 4.7\text{ }\Omega$	-	25.77	-	

**Table 5. Source-drain diode**

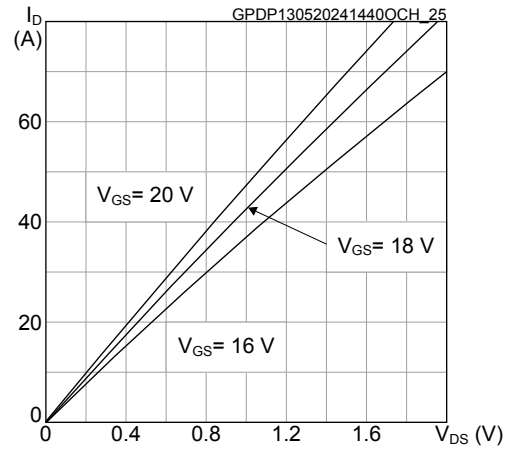
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{SD}$	Forward on voltage drop	$V_{GS} = 0\text{ V}$ , $I_{SD} = 32\text{ A}$	-	2.8	-	V

### 3 Electrical characteristics (curves)

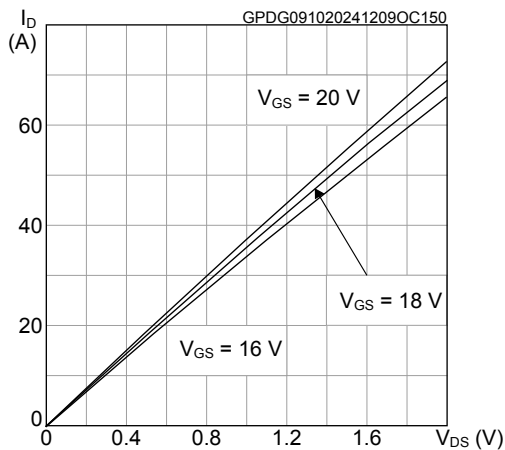
**Figure 1. Typical output characteristics ( $T_J = -40\text{ }^\circ\text{C}$ )**



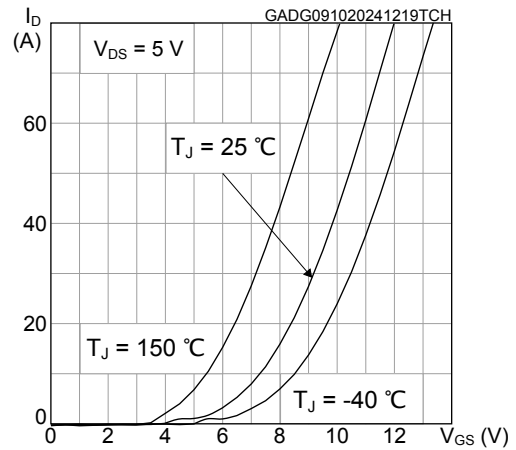
**Figure 2. Typical output characteristics ( $T_J = 25\text{ }^\circ\text{C}$ )**



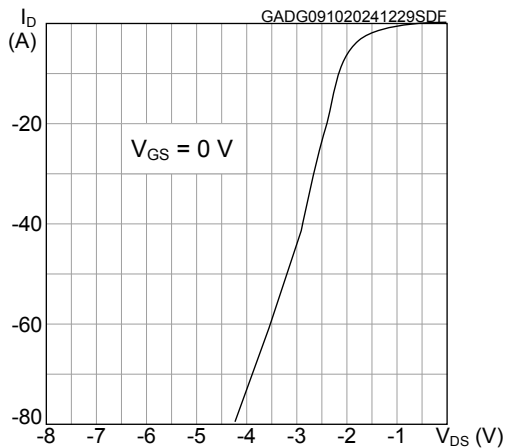
**Figure 3. Typical output characteristics ( $T_J = 150\text{ }^\circ\text{C}$ )**



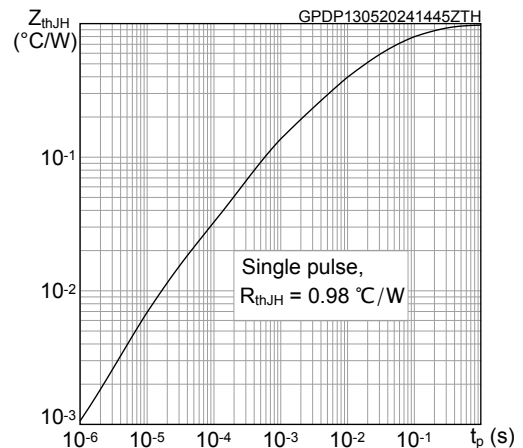
**Figure 4. Typical transfer characteristics**



**Figure 5. Typical diode forward characteristics**



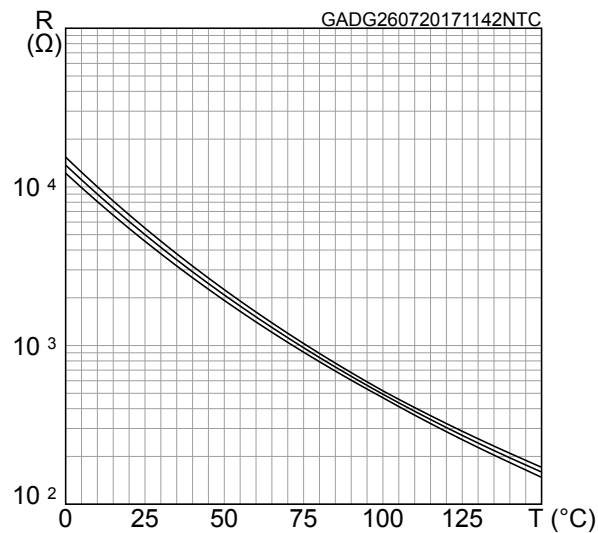
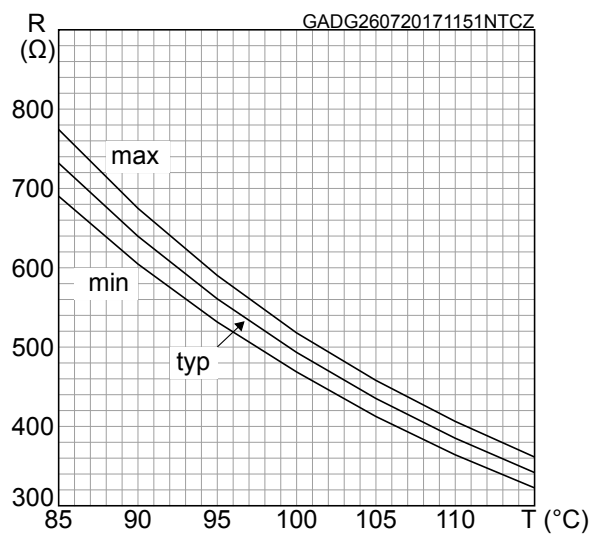
**Figure 6. Maximum transient thermal impedance**



## 4 NTC

**Table 6. NTC temperature sensor, considered as standalone**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
R <sub>25</sub>	Resistance rating	T = 25 °C		5		kΩ
R <sub>100</sub>	Resistance rating	T = 100 °C		493		kΩ
ΔR/R	Deviation of R <sub>100</sub>		-5		+5	%
B <sub>25/50</sub>	B-constant			3375		K
R <sub>25/80</sub>		T = 25 °C to 85 °C		3411		K
T	Operating temperature range		-40		150	°C

**Figure 7. NTC typical resistance vs temperature**

**Figure 8. NTC resistance vs temperature, zoom**


## 5 DC link capacitor (C1812X104KDRACTU)

**Table 7. Absolute maximum rating for capacitor**

Symbol	Parameter	Value	Unit
V <sub>MAX</sub>	Maximum DC voltage	1000	V
C	Capacitance	100	nF
T	Operating temperature range	-40 to 125	°C

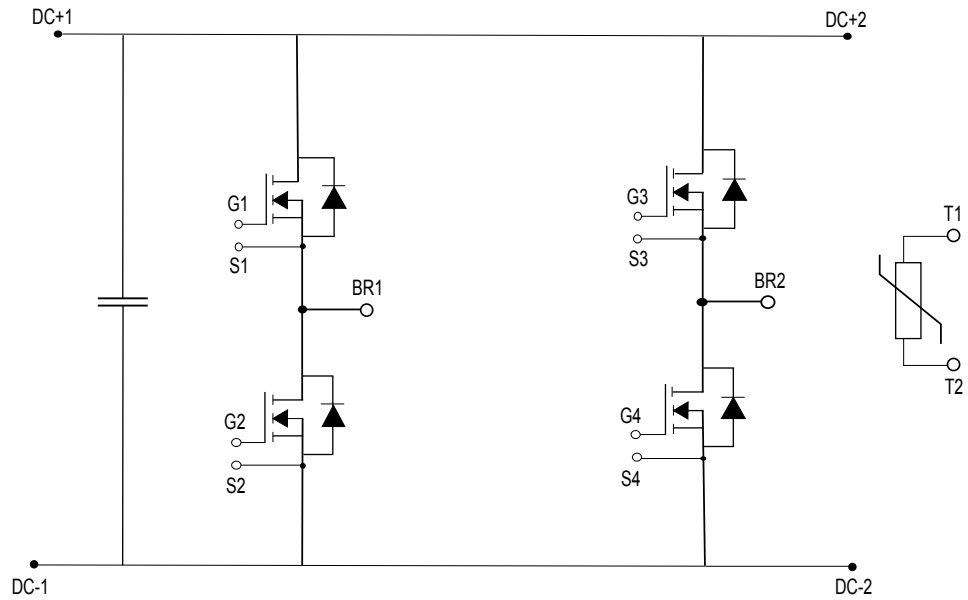
## 6 Package

**Table 8. ACEPACK 2 package**

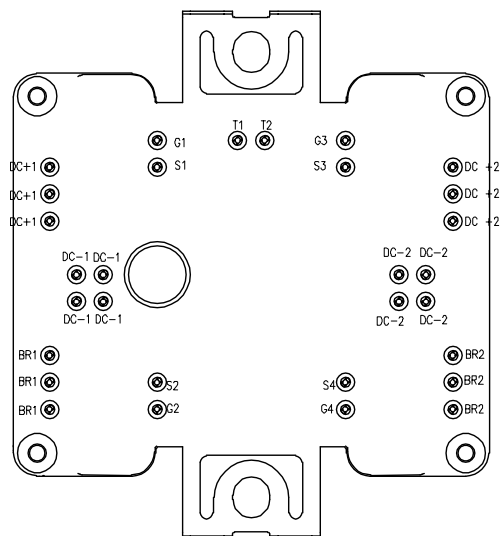
Symbol	Parameter	Value	Unit
V <sub>ISO</sub>	Isolation withstand voltage applied between each pin and heat sink plate (AC voltage, t = 60 s)	2.5	kVrms
CTI	Comparative tracking index	200	V
L <sub>s</sub>	Stray inductance module loop	9.7	nH
T <sub>stg</sub>	Storage temperature range	-40 to 125	°C

## 7 Electrical topology and pin description

**Figure 9. Electrical topology and pin description**



**Figure 10. Package top view with pinout**



GPDP140520241046SA

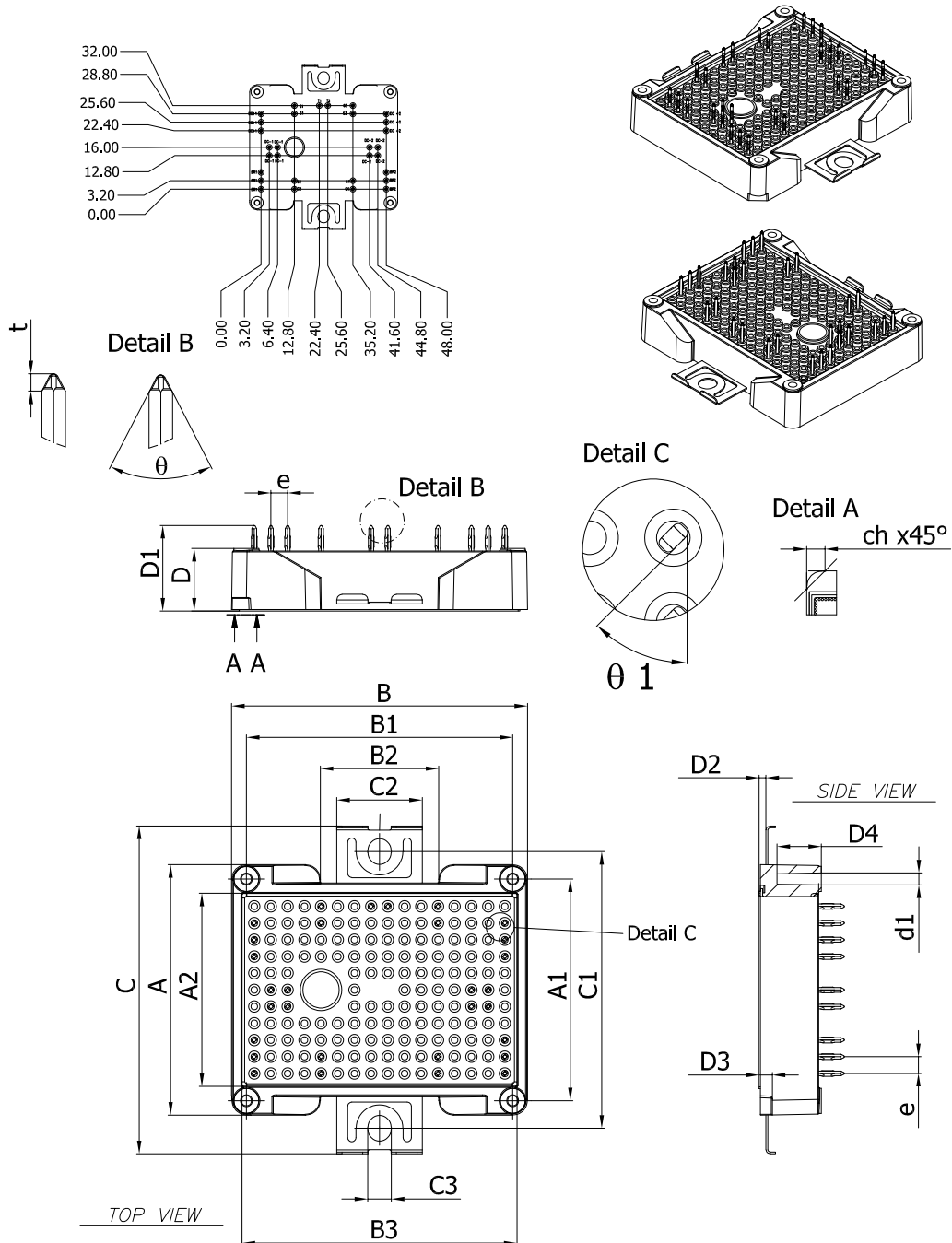


## 8 Package information

To meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

### 8.1 ACEPACK 2 fourpack D2 press-fit package information

Figure 11. ACEPACK 2 fourpack D2 press-fit package outline (dimensions are in mm)

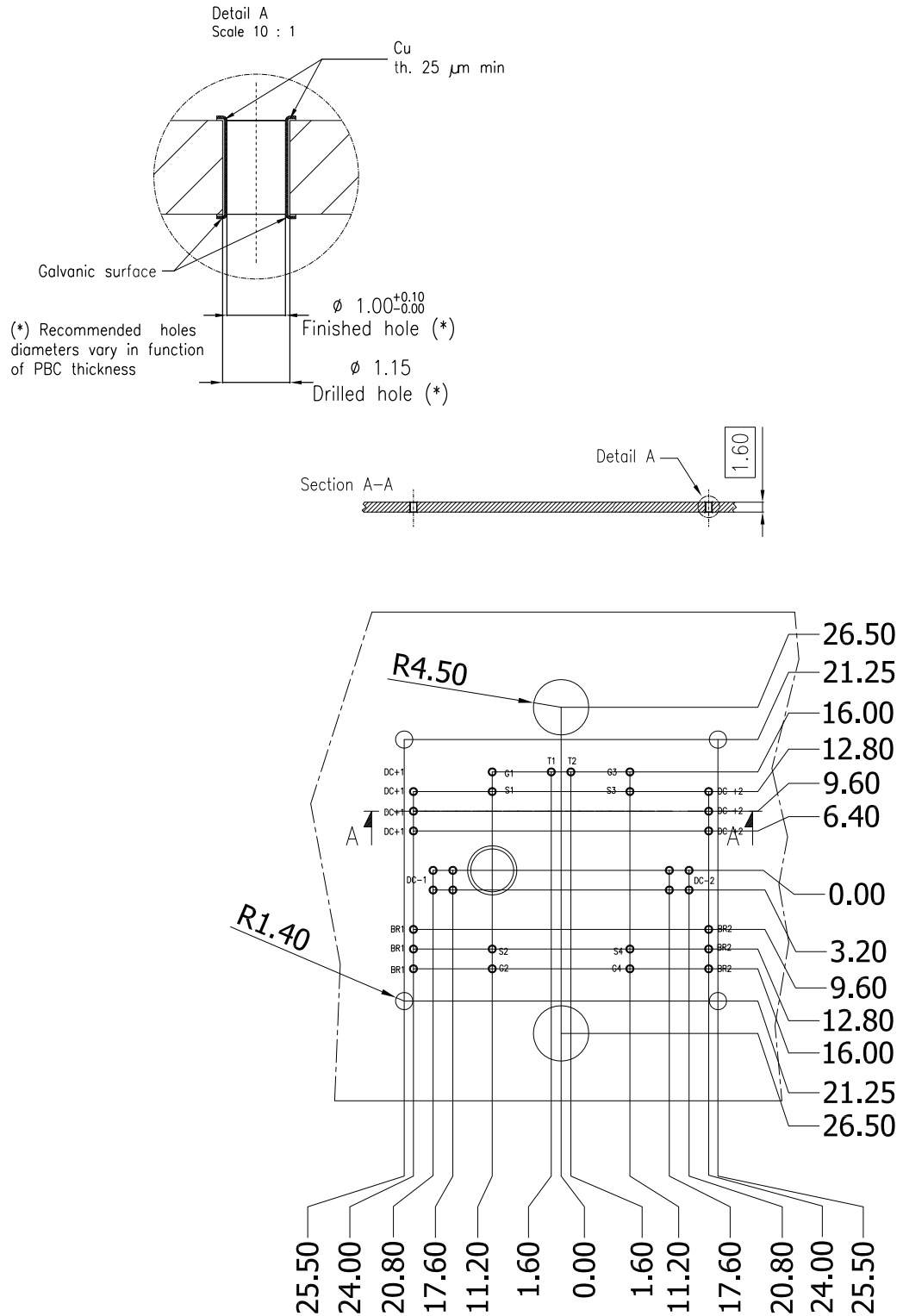


8569722\_15\_fourpack\_press\_fit\_D2

**Table 9. ACEPACK 2 fourpack D2 press-fit mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	47.70	48.00	48.30
A1	42.30	42.50	42.70
A2	37.00 REF		
B	56.40	56.70	57.00
B1	50.85	51.00	51.15
B2	22.40	22.70	23.00
B3	52.70 REF		
C	62.30	62.80	63.30
C1	52.90	53.00	53.10
C2	16.20	16.40	16.60
C3	4.40	4.50	4.60
D	11.65	12.00	12.35
D1	15.90	16.40	16.90
D2	1.10	1.30	1.50
D3	2.30	2.50	2.70
D4			8.50
t	0.30	0.40	0.50
θ	52°	60°	68°
θ1		45°	
e	3.20 BSC		
d1	2.30 REF		
ch	3.50 REF		

**Figure 12. ACEPACK 2 fourpack D2 press-fit recommended PCB holes layout (dimensions are in mm)**



8569722\_15\_fourpack\_press\_fit\_D2\_holes\_layout

## Revision history

**Table 10. Document revision history**

Date	Revision	Changes
07-Nov-2023	1	First release.
08-Jul-2024	2	Modified <i>Table 1. Absolute maximum ratings</i> , <i>Table 2. Thermal data</i> , <i>Table 3. On/off-state</i> , <i>Table 4. Switching energy</i> and <i>Table 5. Source-drain diode</i> . Added <i>Section 3: Electrical characteristics (curves)</i> . Added <i>Section 5: DC link capacitor (C1812X104KDRACTU)</i> . Modified <i>Figure 10. Package top view with pinout</i> . Updated <i>Section 8.1: ACEPACK 2 fourpack D2 press-fit package information</i> . Minor text changes.
14-Oct-2024	3	Updated <i>Table 1. Absolute maximum ratings</i> , <i>Table 3. On/off-state</i> . Updated <i>Section 3: Electrical characteristics (curves)</i> .
28-Oct-2024	4	Updated title, <a href="#">Features</a> , <a href="#">Application</a> and <a href="#">Description</a> in cover page.

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