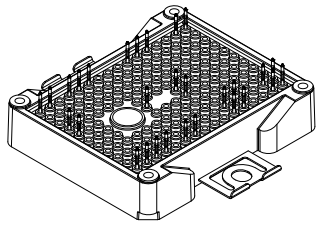
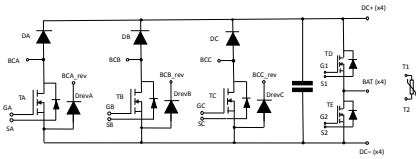
A2TBH45M65W3-FC

Datasheet

ACEPACK 2 power module, triple boost (650 V, 49 mΩ typ.) plus half-bridge topology (650 V, 23.5 mΩ typ.) SiC Power MOSFET gen. 3 with NTC and capacitance



ACEPACK 2



Features

- ACEPACK 2 power module
  - Triple boost switch 49 mΩ of typical $R_{DS(on)}$
  - Half-bridge switch 23.5 mΩ of typical $R_{DS(on)}$
  - Insulation voltage 2.5 kVrms
  - Integrated NTC temperature sensor
  - Integrated DC link capacitor
  - DBC Cu-Al2O3-Cu based
  - Press-fit contact pins

Application

- DC-DC converters
- Solar inverters

Description

This power module realizes a triple boost plus half-bridge topology in an ACEPACK 2 module with NTC and capacitance, integrating the latest advances in silicon carbide MOSFETs from STMicroelectronics, represented by third generation technology. This modular solution is used to realize complex topologies with very high power density and efficiency requirements.

Product status link
A2TBH45M65W3-FC

Product summary	
Order code	A2TBH45M65W3-FC
Marking	A2TBH45M65W3-FC
Package	ACEPACK 2
Leads type	Press-fit
Packing	Tray

1 SiC MOSFET (TA, TB, TC)

T_J = 25 °C unless otherwise specified.

Table 1. Absolute maximum ratings (TA, TB, TC)

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	650	V
V_{GS}	Gate-source voltage	-10 to 22	V
	Gate-source voltage, recommended operating values	-5 to 18	
I_D	Drain current (continuous) at T_H = 25 °C	28	A
I_{DM}	Peak pulsed drain current at t_p = 1 ms	78	A
T_J	Maximum junction temperature	150	°C
	Operating junction temperature range under switching conditions	-40 to 150	

Table 2. Thermal data (TA, TB, TC)

Symbol	Parameter	Value	Unit
R_{thJH}	Thermal resistance, junction-to-heat sink, each switch (TIM = 120 µm, λ = 3 W•m^{-1}•°C^{-1})	1.98	°C/W

Table 3. On/off state (TA, TB, TC)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 18 V , I_D = 15 A		49	72	mΩ
		V_{GS} = 18 V , I_D = 15 A, T_J = 150 °C		64		
$V_{GS(th)}$	Gate threshold voltage	I_D = 5 mA, V_{DS} = V_{GS}	1.85	3.10	4.2	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 650 V, V_{GS} = 0 V			10	µA
I_{GSS}	Gate-body leakage current	V_{DS} = 0, V_{GS} = -10 to 22 V			±100	nA
C_{iss}	Input capacitance	f = 1 MHz, V_{DS} = 400 V, V_{GS} = 0 V		920		pF
C_{oss}	Output capacitance			94		pF
C_{rss}	Reverse transfer capacitance			13		pF
Q_g	Total gate charge	V_{DS} = 400 V, V_{GS} = -5 to 18 V, I_D = 20 A		39.5		nC
Q_{gs}	Gate-source charge			11.5		nC
Q_{gd}	Gate-drain charge			14.5		nC

Table 4. Switching energy (TA, TB, TC)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
dv/dt	On	V_{DS} = 400 V, I_D = 15 A, R_G = 4.7 Ω, V_{GS} = -5 to 18 V	-	42.2	-	V/ns
	Off		-	46	-	

Table 5. Source-drain diode (TA, TB, TC)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{SD}	Forward on voltage drop	V_{GS} = 0 V, I_{SD} = 15 A	-	2.8	-	V

1.1 Electrical characteristics diagrams (TA, TB, TC)

Figure 1. Typical output characteristics, T_J = -40 °C (TA, TB, TC)

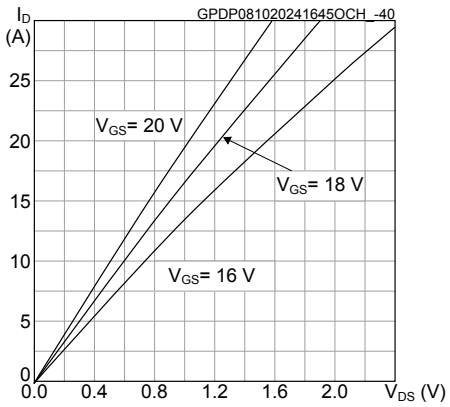


Figure 2. Typical output characteristics, T_J = 25 °C (TA, TB, TC)

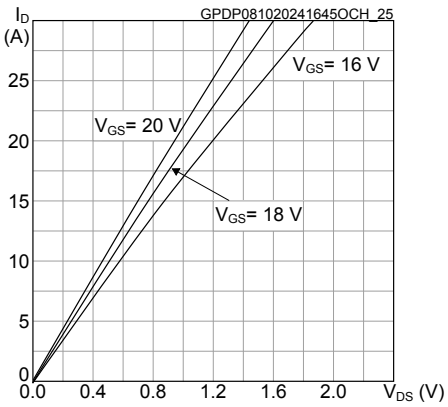


Figure 3. Typical output characteristics, T_J = 150 °C (TA, TB, TC)

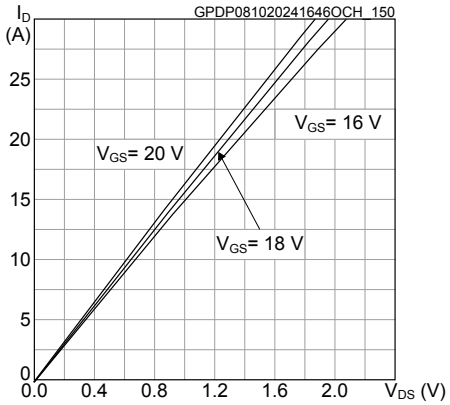


Figure 4. Typical transfer characteristics (TA, TB, TC)

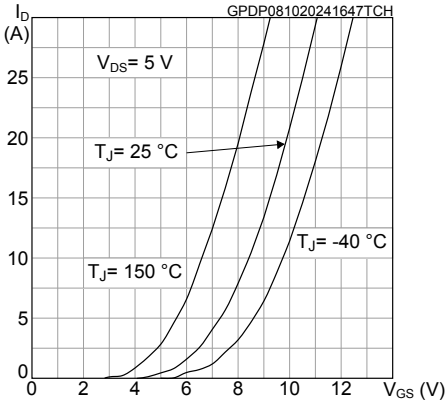


Figure 5. Typical diode charcteristics, terminal (TA, TB, TC)

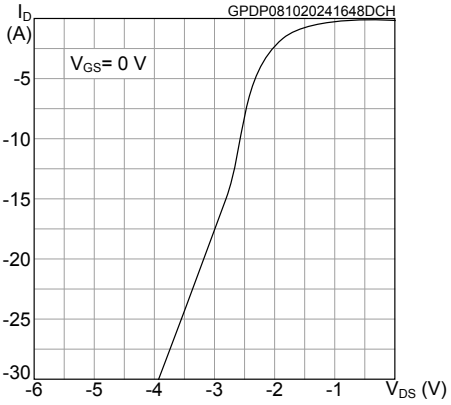
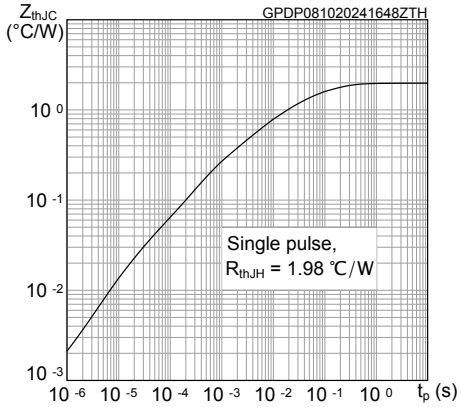


Figure 6. Maximum transient thermal impedence (TA, TB, TC)



2 SiC MOSFET (TD, TE)

T_J = 25 °C unless otherwise specified.

Table 6. Absolute maximum ratings (TD, TE)

Symbol	Parameter	Value	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	650	V
V_{GS}	Gate-source voltage	-10 to 22	V
	Gate-source voltage, recommended operating values	-5 to 18	
I_D	Drain current (continuous) at T_H = 25 °C	52	A
I_{DM}	Peak pulsed drain current at t_p = 1 ms	157	A
T_J	Operating junction temperature range	-55 to 150	°C
T_{stg}	Storage temperature range		°C

Table 7. SiC diode thermal data (TD, TE)

Symbol	Parameter	Value	Unit
R_{thJH}	Thermal resistance, junction-to-heat sink, each switch (TIM = 120 µm, λ = 3 W•m^{-1}•°C^{-1})	1.21	°C/W

Table 8. SiC MOSFET on/off states (TD, TE)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 18 V , I_D = 30 A	-	23.5	35	mΩ
		V_{GS} = 18 V , I_D = 30 A,T_J = 150 °C	-	28		
$V_{GS(th)}$	Gate threshold voltage	I_D = 10 mA, V_{DS} = V_{GS}	1.8	3.1	4.2	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 650 V, V_{GS} = 0 V	-		20	µA
I_{GSS}	Gate-body leakage current	V_{DS} = 0, V_{GS} = -10 to 22 V	-		±100	nA
C_{iss}	Input capacitance	f = 1 MHz, V_{DS} = 400 V, V_{GS} = 0 V	-	1840		pF
C_{oss}	Output capacitance		-	188		pF
C_{rss}	Reverse transfer capacitance		-	26		pF
Q_g	Total gate charge	V_{DD} = 400 V, V_{GS} = -5 to 18 V, I_D = 20 A	-	79		nC
Q_{gs}	Gate-source charge		-	23		nC
Q_{gd}	Gate-drain charge		-	29		nC

Table 9. SiC MOSFET switching energy (TD, TE)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
dv/dt	On	V_{DD} = 400 V, I_D = 15 A, R_G = 4.7 Ω	-	23.8	-	V/ns
	Off	V_{GS} = -5 to 18 V	-	252.1	-	

Table 10. SiC MOSFET source-drain diode (TD, TE)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{SD}	Forward on voltage drop	V_{GS} = 0 V, I_{SD} = 30 A	-	2.8	-	V

2.1 Electrical characteristics diagrams (TD, TE)

Figure 7. Typical output characteristics, T_J = -40 °C (TD, TE)

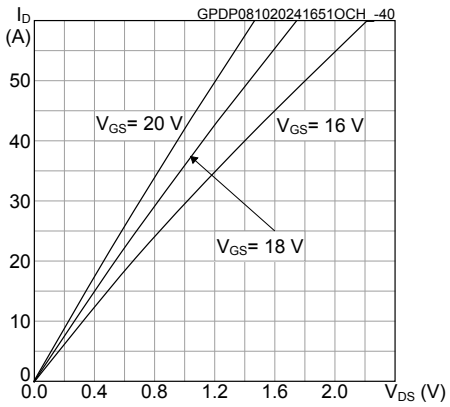


Figure 8. Typical output characteristics, T_J = 25 °C (TD, TE)

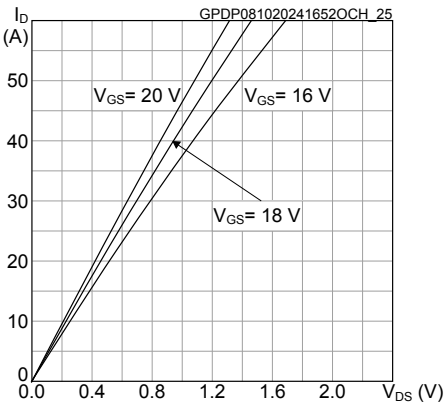


Figure 9. Typical output characteristics, T_J = 150 °C (TD, TE)

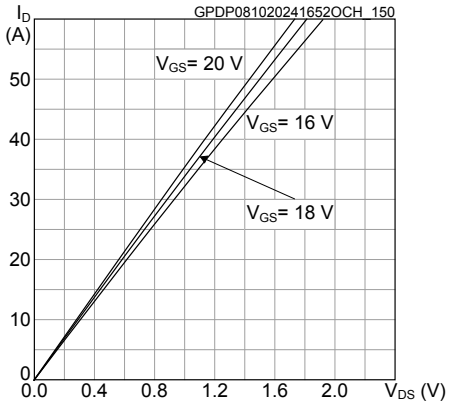


Figure 10. Typical transfer characteristics (TD, TE)

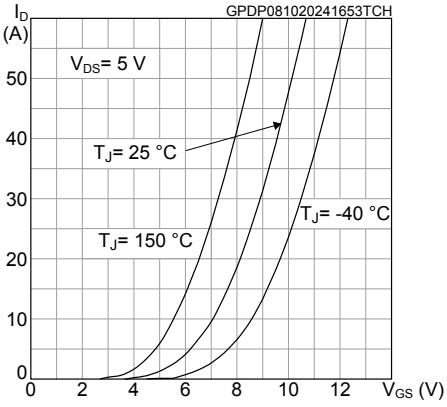


Figure 11. Typical diode charcteristics, terminal (TD, TE)

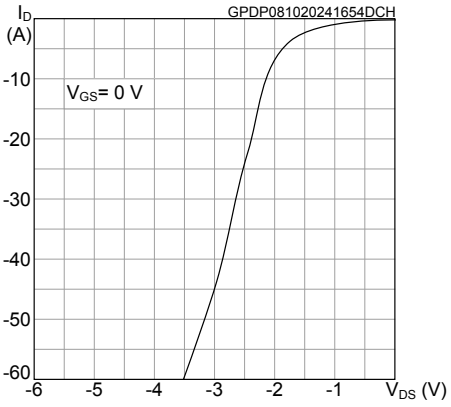
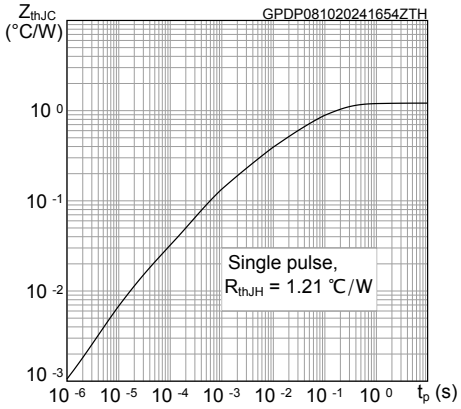


Figure 12. Maximum transient thermal impedence (TD, TE)



3 SiC diode (DA, DB, DC)

T_J = 25 °C unless otherwise specified.

Table 11. Absolute maximum ratings (DA, DB, DC)

Symbol	Parameter	Value	Unit
V_{RRM}	Repetitive peak reverse voltage	650	V
$I_{F(AV)}$	Forward surge current T_H = 85 °C	20	A
T_J	Maximum junction temperature	150	°C
	Operating junction temperature range under switching conditions	-40 to 150	

Table 12. SiC diode thermal data (DA, DB, DC)

Symbol	Parameter	Value	Unit
R_{thJH}	Thermal resistance, junction-to-heat sink, each switch (TIM = 120 µm, λ = 3 W•m^{-1}•°C^{-1})	1.95	°C/W

Table 13. SiC diode electrical characteristic (DA, DB, DC)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_R	Reverse leakage current	$V_R = V_{RRM}$	-	46	224	µA
		$V_R = V_{RRM}$, T_C = 150 °C	-	230		
V_F	Forward voltage drop	I_F = 20 A	-	1.4		V
		I_F = 20 A, T_C = 150 °C	-	1.6		
Q_g	Total capacitive charge	V_R = 400 V	-	70		nC
C_J	Total capacitance	V_R = 0 V, f = 1 MHz	-	1400		pF
		V_R = 400 V, f = 1 MHz	-	90		

3.1 Electrical characteristics diagrams (DA, DB, DC)

Figure 13. Typical forward voltage drop (DA, DB, DC)

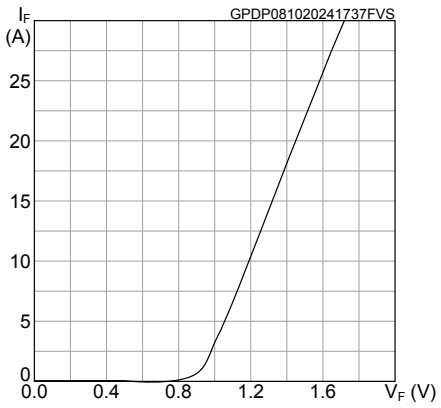
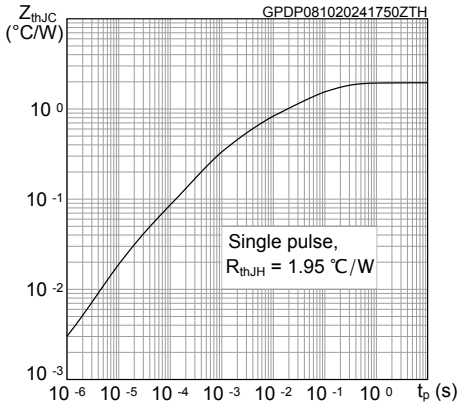


Figure 14. Maximum transient thermal impedence (DA, DB, DC)



4 Rectifier diode (Drev A, B, C)

T_J = 25 °C unless otherwise specified.

Table 14. Rectifier diode absolute maximum ratings (Drev A, B, C)

Symbol	Parameter	Value	Unit
V_{RRM}	Repetitive peak reverse voltage from T = -40 °C to +175 °C	800	V
$I_{F(RMS)}$	Forward RMS current	48	A
T_J	Maximum junction temperature	150	°C
	Operating junction temperature range under switching conditions	-40 to 150	

Table 15. SiC diode thermal data (Drev A, B, C)

Symbol	Parameter	Value	Unit
R_{thJH}	Thermal resistance, junction-to-heat sink, each switch (TIM = 120 µm, λ = 3 $W•m^{-1}•°C^{-1}$)	1.67	°C/W

Table 16. Rectifier diode electrical characteristic (Drev A, B, C)

Symbol	Parameter	Test condition		Min.	Typ.	Max.	Unit
I_R	Reverse leakage current	T_J = 25 °C	$V_R = V_{RRM}$	-		2	µA
		T_J= 150 °C		-	10	100	
V_F	Forward voltage drop	T_J = 25 °C	I_F = 30 A	-	1.1		V
		T_J= 150 °C		-	1		

4.1 Electrical characteristics diagrams (Drev A, B, C)

Figure 15. Typical foward voltage drop (Drev A, B, C)

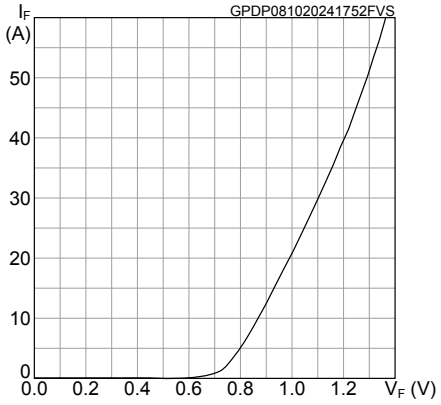
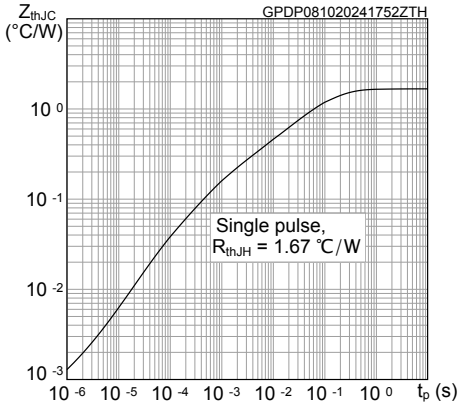


Figure 16. Maximum transient thermal impedence (Drev A, B, C)



5 NTC

Table 17. Absolute maximum ratings for NTC temperature sensor, considered as stand-alone

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
R_{25}	Resistance rating	T = 25 °C		5		kΩ
R_{100}	Resistance rating	T = 100 °C		493		Ω
$\Delta R_{100}/R$	Resistance tolerance		-5		5	%
B	B value	T = 25 to 50 °C		3375		K
		T = 25 to 85 °C		3411		
T	Operating temperature range		-40		150	°C

Figure 17. NTC typical resistance vs temperature

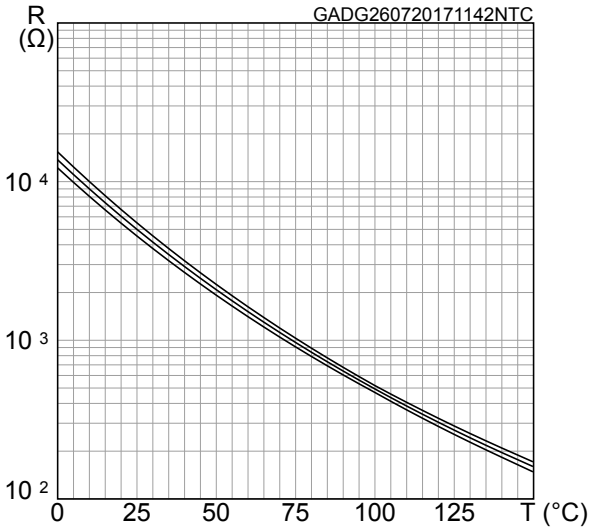
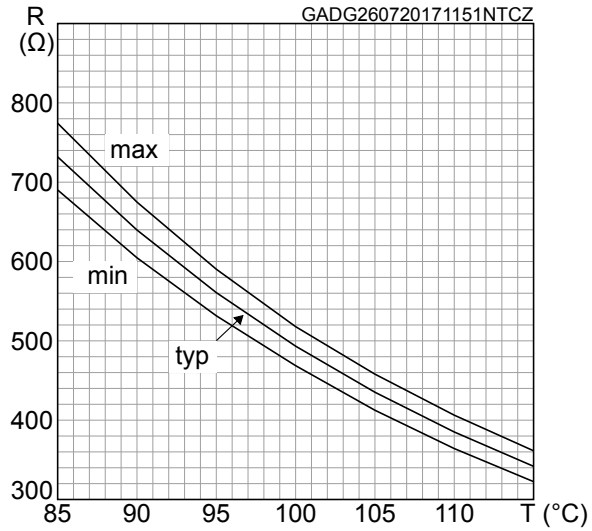


Figure 18. NTC resistance vs temperature, zoom



6 DC link capacitor (two C1210X473KDRACTU in parallel)

Table 18. Absolute maximum rating for capacitor

Symbol	Parameter	Value	Unit
V_{MAX}	Maximum DC voltage	1000	V
C	Capacitance	94 (47x2)	nF
T	Operating temperature range	-40 to 125	°C

7 Package

Table 19. **ACEPACK 2 package**

Symbol	Parameter	Value	Unit
V_{ISO}	Isolation withstand voltage applied between each pin and heat sink plate (AC voltage, t = 60 s)	2.5	kVrms
CTI	Comparative tracking index	200	V
L_s	Stray inductance module loop	10	nH
T_{stg}	Storage temperature range	-40 to 125	°C

8 Electrical topology and pin description

Figure 19. **Electrical topology and pin description**

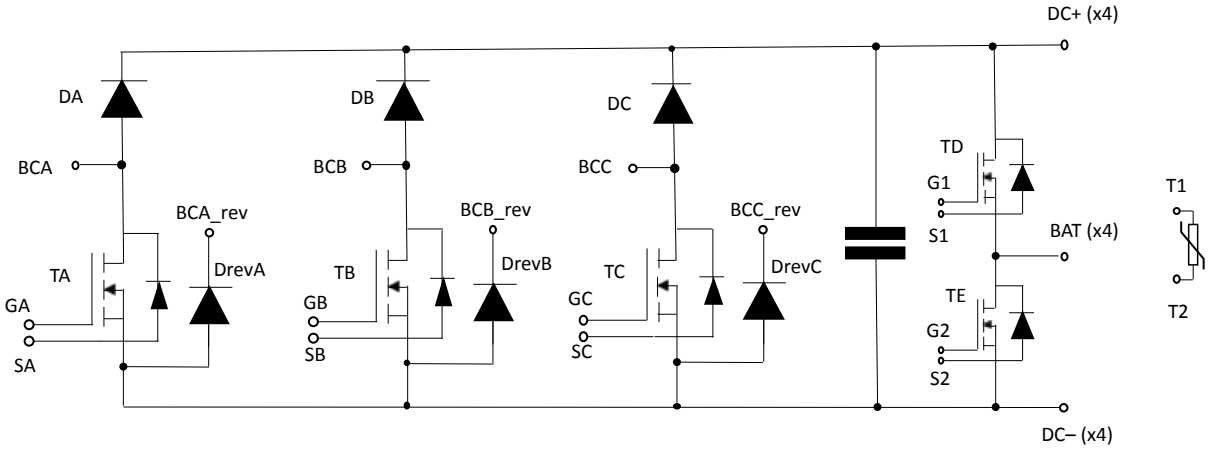
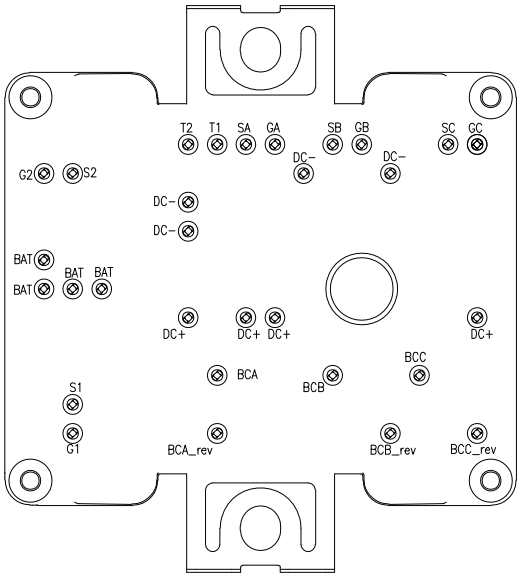


Figure 20. **Package top view with pinout**



9 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

9.1 ACEPACK 2 triple boost plus half-bridge press-fit package information

Figure 21. ACEPACK 2 triple boost plus half-bridge press-fit package outline (dimensions are in mm)

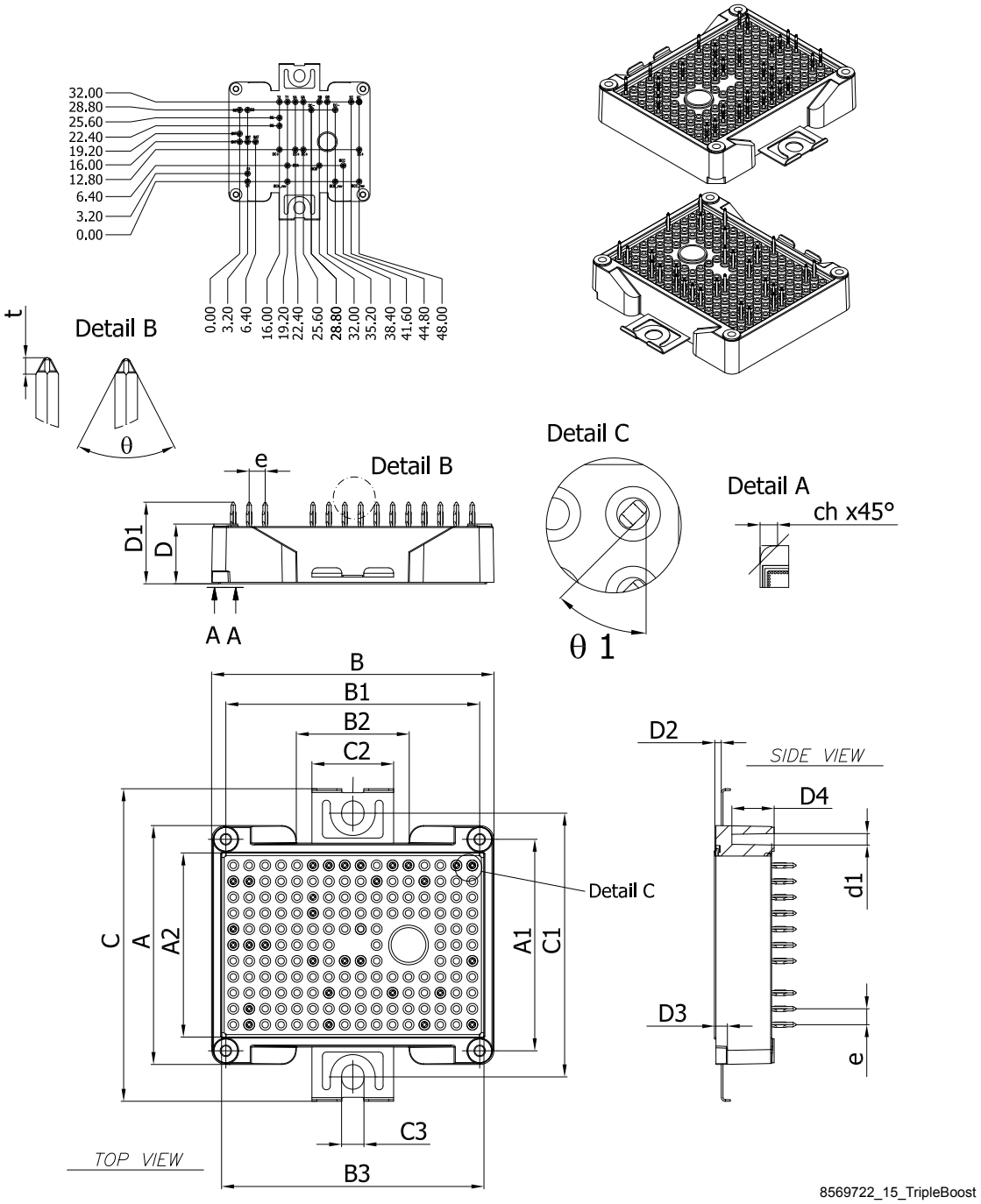
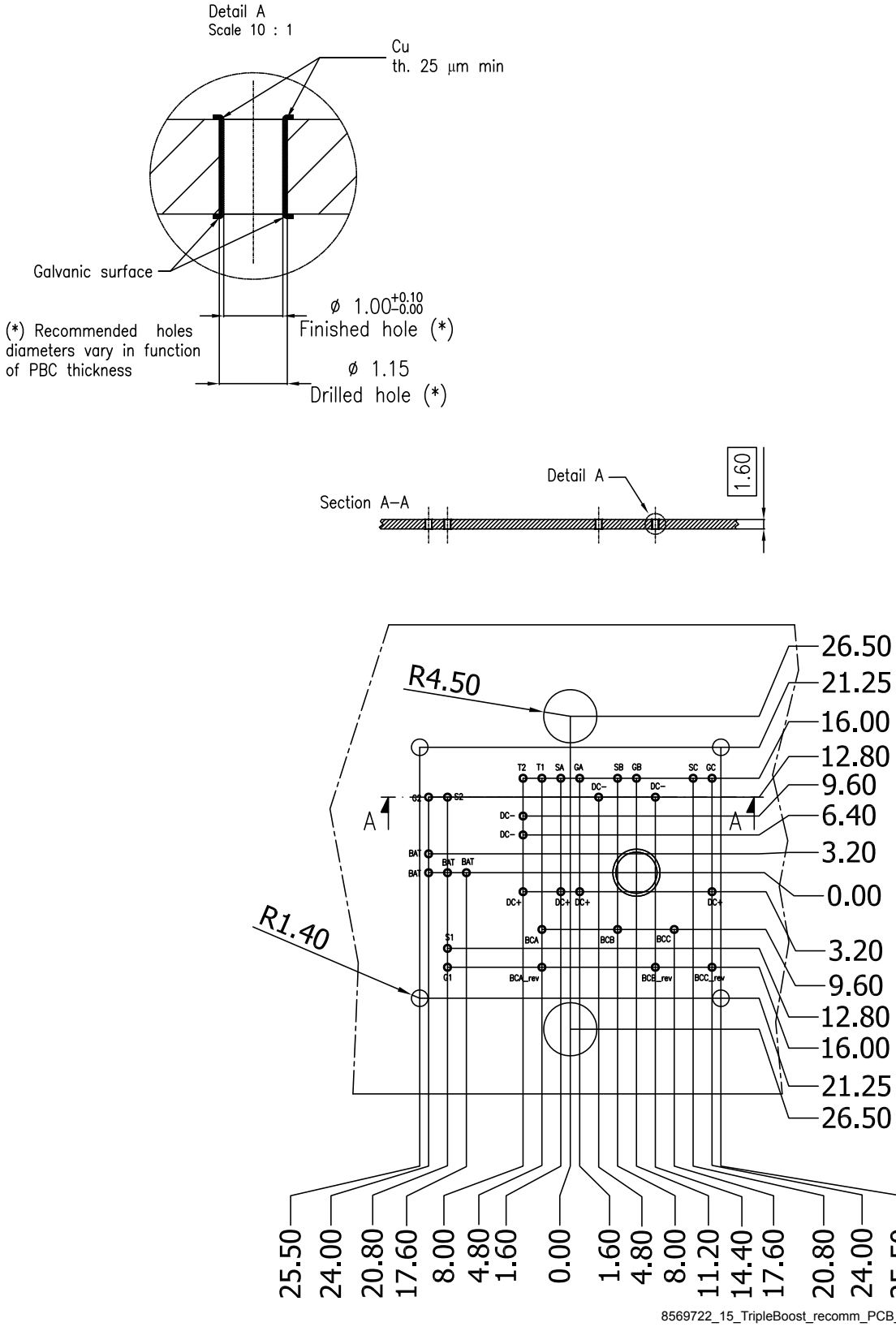


Table 20. **ACEPACK 2 triple boost plus half-bridge press-fit mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	47.70	48.00	48.30
A1	42.30	42.50	42.70
A2		37.00 REF	
B	56.40	56.70	57.00
B1	50.85	51.00	51.15
B2	22.40	22.70	23.00
B3		52.70 REF	
C	62.30	62.80	63.30
C1	52.90	53.00	53.10
C2	16.20	16.40	16.60
C3	4.40	4.50	4.60
D	11.65	12.00	12.35
D1	15.90	16.40	16.90
D2	1.10	1.30	1.50
D3	2.30	2.50	2.70
D4			8.50
t	0.30	0.40	0.50
θ	52°	60°	68°
θ1		45°	
e		3.20 BSC	
d1		2.30 REF	
ch		3.50 REF	

Figure 22. ACEPACK 2 triple boost plus half-bridge press-fit recommended PCB holes layout (dimensions are in mm)



Revision history

Table 21. **Document revision history**

Date	Revision	Changes
26-Jan-2024	1	First release.
15-Oct-2024	2	Modified *Features*, *Section 1: SiC MOSFET (TA, TB, TC)*, *Section 3: SiC diode (DA, DB, DC)*, *Section 4: Rectifier diode (Drev A, B, C)* and *Section 2: SiC MOSFET (TD, TE)*. Added *Section 1.1: Electrical characteristics diagrams (TA, TB, TC)*, *Section 2.1: Electrical characteristics diagrams (TD, TE)*, *Section 3.1: Electrical characteristics diagrams (DA, DB, DC)* and *Section 4.1: Electrical characteristics diagrams (Drev A, B, C)*. Added *Section 6: DC link capacitor (C1210X473KDRACTU)*. Minor text changes.
28-Oct-2024	3	Updated title, *Features*, and *Application* in cover page.
17-Dec-2024	4	Updated *Internal schematic* and *Figure 19*.
18-Dec-2024	5	Updated Table 18. Absolute maximum rating for capacitor.

Contents