DCP3601

Datasheet

36 V, 1 A synchronous step-down converter in SOT23-6L

Maturity status link
DCP3601

Features

- 88% typical efficiency at 600 mA load (V_{IN} = 24 V, V_{OUT} = 5 V)
- 91% typical efficiency at 600 mA load (V_{IN} = 12 V, V_{OUT} = 5 V)
- 3.3 V to 36 V input operating voltage range
- Up to 1 A output current capability
- 110 µA input quiescent current
- 1 MHz fixed switching frequency
- Synchronous rectification
- Internal compensation network
- Peak current mode control
- Two different versions: LCM for high efficiency at light loads and LNM for noise-sensitive applications
- Output overvoltage protection
- Thermal shutdown
- Precision enable
- Switching frequency dithering
- Available in SOT23-6L package

Applications

- Major appliances
- Smart metering
- Industrial 24 V bus conversion

Description

The DCP3601 is a wide-input voltage, easy-to-use synchronous buck converter capable of driving up to 1 A load current. The extended input range from 3.3 V to 36 V makes the device suitable for a wide range of industrial applications.

The DCP3601 operates at 1 MHz fixed switching frequency allowing the use of small inductors for an optimized solution size.

Optional switching frequency dithering is implemented to improve EMI performances.

It is based on a peak current mode architecture, including soft-start circuit, overcurrent protection circuit, overtemperature protection and output overvoltage protection, and is packaged in a SOT23-6L package.

1 Application schematic

Figure 1. **DCP3601 typical application schematic**

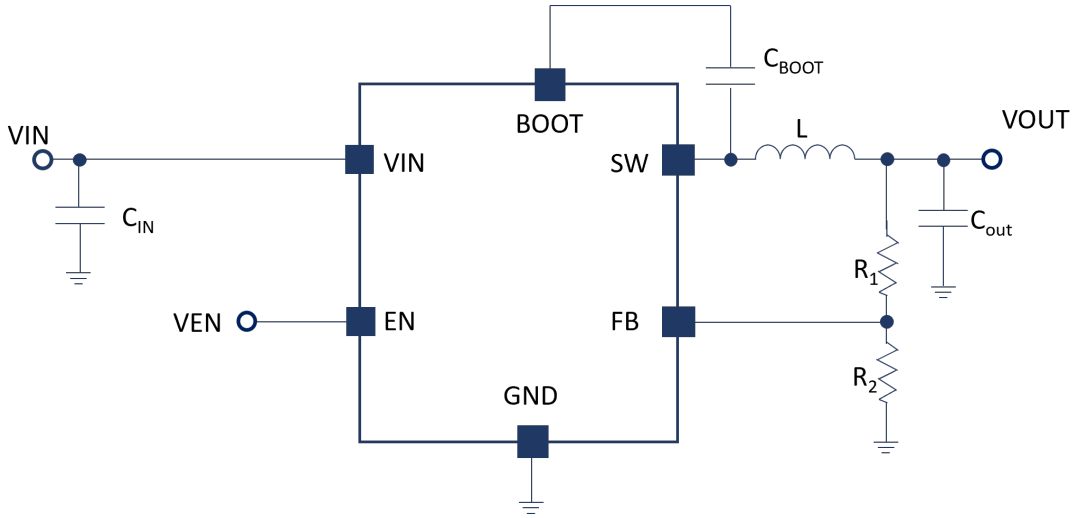


Table 1. **Typical external components**

VOUT	L	CIN (1)	COUT (1)	CBOOT (1)	R1	R2
5.0 V	15 µH	2.2 µF / 50 V	22 µF / 25 V	100 µF / 50 V	73.2 kΩ	15 kΩ
	XGL5050-153 - Coilcraft 744393305150 - Wurth	C2012X7R1H225K125AC - TDK	C2012X5R1E226M125A - TDK	C1608X7R1H104K080AA - TDK	-	-
3.3 V	10 µH	2.2 µF / 50 V	22 µF / 25 V	100 nF / 50 V	86.6 kΩ	30 kΩ
	XGL5050-103 - Coilcraft	C2012X7R1H225K125AC - TDK	C2012X5R1E226M125A - TDK	C1608X7R1H104K080AA - TDK	-	-

1. *Ceramic capacitor.*

2 Pin connections

Figure 2. **Pin configuration (top view)**

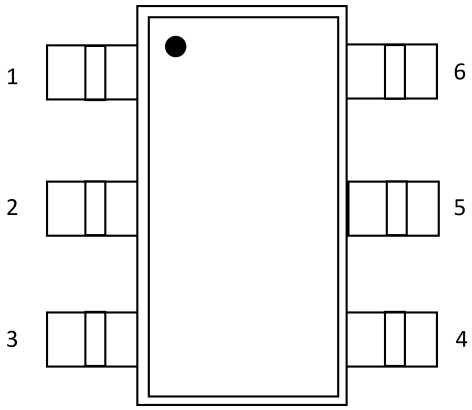


Table 2. **Pin description**

Name	Pin #	Description
BOOT	1	**Bootstrap.** Connect a capacitor between SW and BOOT to form a floating supply across the high-side switch driver.
GND	2	**System ground.** GND is the reference ground of the regulated output voltage. Therefore, care must be taken during PCB layout. Use wide PCB traces to make the connection.
FB	3	**Feedback.** An external resistor divider from the output to GND tapped to FB sets the output voltage. It is recommended to place the resistor divider as close as possible to the FB pin.
EN	4	**Enable.** Precision enable pin. If the EN voltage is below 0.95 V, the converter is in shutdown mode with all functions disabled (cannot be left floating).
VIN	5	**Input voltage.** VIN supplies power for the internal MOSFET, regulator, and the embedded analog circuitry. Input capacitors are needed to decouple the input rail. Use wide PCB traces to make the connection.
SW	6	**Switch output.** Connect SW to the inductor and bootstrap capacitor. SW is driven up to VIN by the high-side switch during the on-time of the PWM duty cycle. The inductor current drives SW low during the off-time. Use wide PCB traces to make the connection.

3 Maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{IN}	Power supply voltage	- 0.3 to + 38	V
V_{EN}	Enable input voltage	- 0.3 to V_{IN} +0.3	V
V_{FB}	Feedback pin voltage	- 0.3 to + 1.5	V
$V_{BOOT-SW}$	Boot to SW differential voltage	- 0.3 to + 5.5	V
SW	Switching node voltage DC	- 0.3 to V_{IN} +0.3	V
T_J	Operating junction temperature	- 40 to 150	°C
T_{STG}	Storage temperature	- 55 to 150	°C

Note: Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

Table 4. Thermal data

Symbol	Parameter	SOT23-6L	Unit
R_{thJA}	Thermal resistance junction-ambient	160	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	106	
$R_{\theta JB}$	Junction-to-board thermal resistance	55	
ψ_{JT}	Junction-to-top characterization parameter	29	
ψ_{JB}	Junction-to-board characterization parameter	61	

Note: These values were calculated in accordance with JESD specification and simulated on a 4-layer JEDEC board.

Table 5. Recommended operating conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IN}	Input supply voltage	3.3		36	V
V_{EN}	Enable supply voltage (1)	0		V_{IN}	V
I_{OUT}	Output current	0		1	A

1. *The voltage on this pin must not exceed the voltage on the V_{IN} pin by more than 0.3 V.*

Table 6. ESD ratings

Symbol	Parameter	Value	Unit
V_{ESD}	Human Body Model (HBM)	±1000	V
	Charged Device Model (CDM)	±500	

4 Electrical characteristics

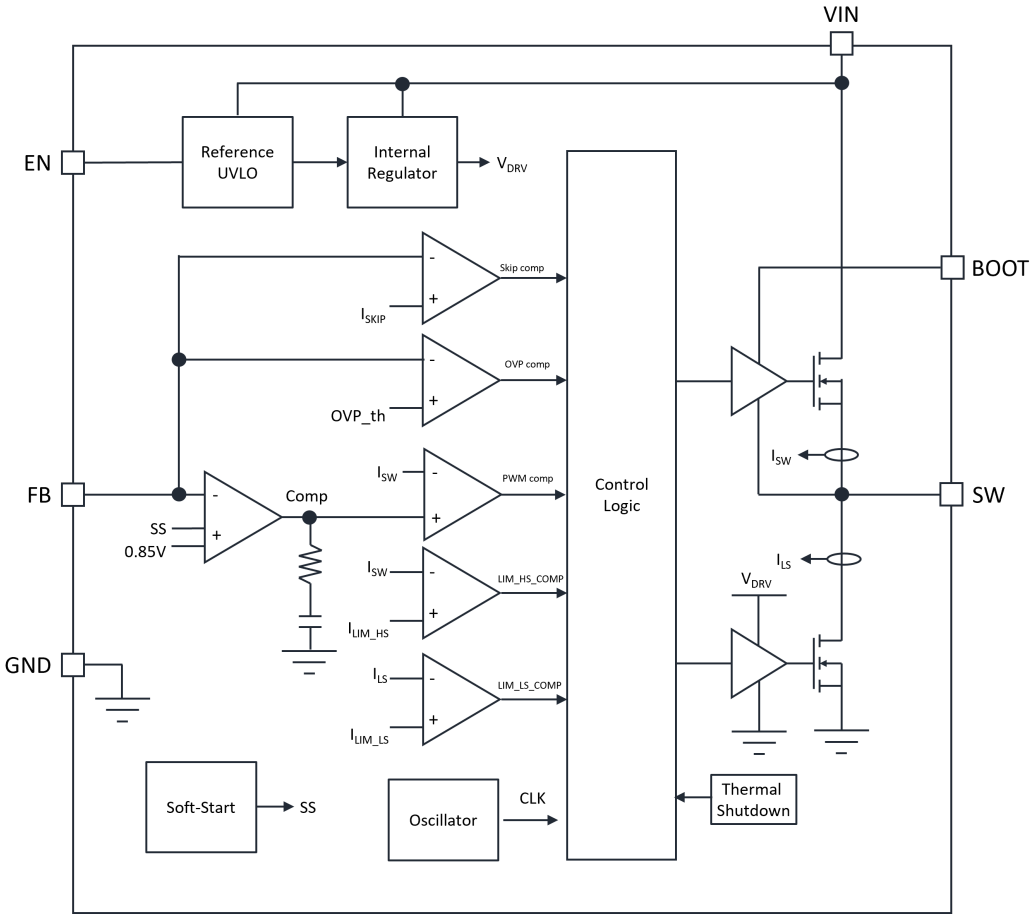
T_J = 25 °C, V_{IN} = 24 V unless otherwise specified.

Table 7. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{FB}	Feedback voltage	T_J = 25 °C	0.833	0.850	0.867	V
I_Q	Quiescent current	LCM version – V_{EN} = 3.3 V, V_{FB} = 0.90 V (No Switching)		110	140	µA
		LNM version – V_{EN} = 3.3 V, V_{FB} = 0.90 V (No Switching)		1.4		mA
I_{SD}	Shutdown current	V_{EN} = 0 V		4	7	µA
I_{SKIP}	Skip current limit			0.25		A
I_{VY_SINK}	Reverse current limit	LNM or VOUT overvoltage	0.80	1.0	1.15	A
V_{UVLO}	Undervoltage lockout threshold	V_{IN} rising	2.85		3.2	V
		V_{IN} falling	2.55		2.9	V
V_{EN}	Enable threshold	V_{EN} rising	1.1	1.23	1.36	V
		V_{EN} falling	0.95	1.1	1.22	V
I_{LKG_EN}	Enable input leakage current	V_{EN} = 3.3 V		10	200	nA
		V_{EN} = 36 V		10		
I_{LKG_FB}	Feedback input leakage current	V_{FB} = 1.2 V		0.2		nA
$R_{DS\_ON\_HS}$	High-side MOSFET on-resistance	I_{SW} = 0.1 A		0.50	0.60	Ω
$R_{DS\_ON\_LS}$	Low-side MOSFET on-resistance	I_{SW} = 0.1 A		0.26	0.40	
I_{LIM_HS}	High-side MOSFET switch current limit	V_{IN} = 24 V	1.4	1.55	1.65	A
I_{LIM_LS}	Low-side MOSFET switch current limit	V_{IN} = 24 V	1.35	1.6	1.75	A
t_{ON_MIN}	Minimum switch-on time	on SW pin		110		ns
t_{OFF_MIN}	Minimum switch-off time	on SW pin		110		ns
t_{SS}	Internal soft-start time	from 10% to 90% of V_{FB}		1.4		ms
F_{SW}	Switching frequency		0.8	1	1.2	MHz
T_{SD}	Thermal shutdown threshold			175		°C
T_{SD_REC}	Thermal recovery threshold			155		°C
V_{OVP}	Overvoltage threshold (V_{OVP}/V_{FB})			120		%
V_{OVP_HYST}	Overvoltage hysteresis			2		%

5 Block diagram

Figure 3. **Block diagram**



6 Functional description

The DCP3601 device is based on a “peak current mode" architecture with constant frequency control. Therefore, the intersection between the error amplifier output and the sensed inductor current generates the PWM control signal to drive the power switch.

The device features LNM (low noise mode) that is forced PWM control, or LCM (low consumption mode) to increase the efficiency at light-load on the selected part number.

The main internal blocks shown in the block diagram are:

- Embedded power elements
- A fully integrated saw tooth oscillator with the ramp for the slope compensation avoiding subharmonic instability
- The transconductance error amplifier with integrated compensation network
- The high-side current sense amplifier to sense the inductor current
- A “pulse width modulator” (PWM) comparator and the driving circuitry of the embedded power elements
- The soft-start blocks to ramp the error amplifier reference voltage and so decrease the inrush current at power-up. The EN pin inhibits the device when driven low
- The EN pin switches the device on and off
- The current limitation circuit to implement the constant current protection, sensing pulse-by-pulse the high-side / low-side switch current
- A circuit to implement the thermal protection function
- Dithering
- The OVP circuitry to discharge the output capacitor in case of overvoltage event

6.1 EN

The EN pin controls the ON/OFF operation of the buck converter. If the voltage is less than 0.95 V, it shuts down the device, while a voltage of greater than 1.36 V is required to start the converter.

The EN pin is an input and cannot be left open or floating. The simplest way to enable the operation of the DCP3601 is to connect the EN to VIN. This allows self-startup when VIN is within the operating range.

6.2 Soft-start

The soft-start (SS) limits the inrush current surge and makes the output voltage increase monotonically. The device implements the soft-start phase ramping the internal reference with very small steps. Once the SS ends, the error amplifier reference is switched to the internal value of 0.85 V coming directly from the bandgap cell.

During normal operation, a new soft-start cycle takes place in case of:

1. Thermal shutdown event
2. UVLO event
3. EN pin rising over V_{EN} threshold

6.3 Light-load operation

The DCP3601 implements two different light-load strategies:

1. Low consumption mode (LCM)
2. Low noise mode (LNM)

Refer to Table 9 to select the part number with the preferred light-load strategy.

6.3.1 Low consumption mode (LCM)

Low consumption mode (LCM) is an advanced feature that enhances the efficiency under light-load conditions.

When the switch peak current request is lower than the I_{SKIP} threshold (see Table 7), the device regulates V_{OUT} by the skip threshold, generating pulses at a variable frequency that is inversely proportional to the load. The duty cycle of the pulses may remain relatively constant, but the interval between pulses increases as the load decreases.

The device intentionally interrupts the switching activities when two conditions happen together:

1. The peak inductor current required is lower than I_{SKIP}
2. The voltage on the FB pin is higher than the reference voltage 0.85 V

A new switching cycle takes place once the voltage on the FB pins becomes lower than 0.85 V. The HS switch is kept on until the inductor current reaches I_{SKIP}. The amount of inductor peak current is independent of the required conversion and component selection.

Once the current on the HS reaches the defined value, the device turns the HS off and turns the LS on. The LS is kept enabled until one of the following conditions occurs:

1. The inductor current sensed by the LS becomes equal to zero
2. The switching period has expired

If, at the end of the switching cycle, the voltage on the FB (Feedback) pin is still above the reference voltage, the LS (low-side switch) remains enabled until the inductor current becomes equal to zero. Otherwise, the device turns on the HS again and starts a new switching pulse.

During the burst pulse, if the energy transferred to C_{OUT} increases the V_{FB} level enough above the reference voltage, the device interrupts the switching activities. The new cycle takes place only when V_{FB} becomes lower than the reference. Otherwise, as soon as the LS is turned off the HS is turned on.

Given the energy stored in the inductor during a burst, the voltage ripple depends on the capacitor value:

$$V_{OUT\_RIPPLE} = \frac{\Delta Q_{IL}}{C_{OUT}} = \frac{\int_0^T BURST(I_L(t))dt}{C_{OUT}} \quad (1)$$

In case of a very light-load condition in LCM, the device can enter into sleep mode with minimized input current absorption.

6.3.2 Low noise mode (LNM)

Low noise mode implements a forced PWM operation over the different loading conditions. The LNM features a constant switching frequency to minimize the noise in the final application and a constant voltage ripple at fixed V_{IN}.

The regulator in steady loading condition operates in continuous conduction mode (CCM) over the different loading conditions.

The triangular shape current ripple (with zero average value) flowing into the output capacitor gives the output voltage ripple, which depends on the capacitor value and the equivalent resistive component (ESR). Consequently, the output capacitor must be selected in order to have a voltage ripple compliant with the application requirements.

$$V_{OUT\ RIPPLE} = ESR \cdot \Delta I_{LMAX} + \frac{\Delta I_{LMAX}}{8 \cdot C_{OUT} \cdot f_{SW}} \quad (2)$$

Usually, the resistive component of the ripple can be neglected if the selected output capacitor is a multilayer ceramic capacitor (MLCC).

6.4 Dithering

The internal dithering circuit changes the switching frequency in a range of ± 5%.

$$\Delta F_{SW} = 5\,\% \cdot F_{SM} \quad (3)$$

The device updates the frequency every clock period by fixed steps:

- Ramps up in 63 steps from minimum to maximum F_{SW}
- Ramps down in 63 steps from maximum to minimum F_{SW}

The modulation shape is almost triangular with a frequency of:

$$F_{Dithering} = F_{SW}/126 \quad (4)$$

6.5 Duty cycle range

Minimum ON-time (t_{ON_MIN}) is the shortest duration of time that the high-side switch can be turned on. t_{ON_MIN} is typically 100 ns.

Minimum OFF-time (t_{OFF_MIN}) is the shortest duration of time that the high-side switch can be off. t_{OFF_MIN} is typically 120 ns. In CCM operation, t_{ON_MIN} and t_{OFF_MIN} limit the voltage conversion range without switching frequency foldback.

The minimum duty cycle without frequency foldback allowed is:

$$D_{MIN} = t_{ON\_min} \cdot F_{SW} \quad (5)$$

The maximum duty cycle without frequency foldback allowed is:

$$D_{MAX} = 1 - (t_{OFF\_min} \cdot F_{SW}) \quad (6)$$

Given a required output voltage, the maximum V_{IN} can be found by:

$$V_{IN\_MAX} = V_{OUT} / t_{ON\_min} \cdot F_{SW}) \quad (7)$$

6.6 Overcurrent protection

The current protection circuitry features a constant current protection, so the device limits the maximum peak current (please refer to Table 7) in overcurrent condition.

The DCP3601 device implements a pulse-by-pulse current sensing on both power elements (high-side and low-side switches) for effective current protection over the duty cycle range. The high-side current sensing is called “peak”, the low-side sensing “valley”.

The internal noise generated during the switching activity makes the current sensing circuitry ineffective for a minimum conduction time of the power element. This time is called “masking time” because the information from the analog circuitry is masked by the logic to prevent an erroneous detection of the overcurrent event. Therefore, the peak current protection is disabled for a masking time after the high-side switch is turned on. The masking time for the valley sensing is activated after the low-side switch is turned on. In other words, the peak current protection can be ineffective at extremely low duty cycles, the valley current protection at extremely high duty cycles.

The DCP3601 device assures an effective overcurrent protection sensing the current flowing in both power elements. In case one of the two current sensing circuitry is ineffective because of the masking time, the device is protected sensing the current on the opposite switch. Thus, the combination of the “peak” and “valley” current limits assure the effectiveness of the overcurrent protection even in extreme duty cycle conditions.

In case the current diverges because of the high-side masking time, the low-side power element is turned on until the switch current level drops below the valley current sense threshold. The low-side operation is able to prevent the high-side turn-on, so the device can skip pulses decreasing the switching frequency.

6.7 Overvoltage protection

The overvoltage protection monitors the FB pin and enables the low-side MOSFET to discharge the output capacitor if the output voltage is 20% over the nominal value.

This is a second-level protection, and it should never be triggered in normal operating conditions if the system is properly dimensioned. In other words, the selection of the external power components and the dynamic performance determined by the compensation network should ensure an output voltage regulation within the overvoltage threshold even during the worst-case scenario in terms of load transitions.

The protection is reliable and able to operate even during normal load transitions for a system whose dynamic performance is not in line with the load dynamic request. Consequently, the output voltage regulation would be affected.

The DCP3601 device implements a negative current limitation (I_{VY_SINK}, refer to Table 7) to limit the maximum reversed switch current during the overvoltage operation.

6.8 Thermal shutdown

The shutdown block disables the switching activity if the junction temperature is higher than a fixed internal threshold (T_{SH}, refer to Table 7). The thermal sensing element is close to the power elements, ensuring fast and accurate temperature detection. A hysteresis of approximately 20 °C prevents the device from turning ON and OFF too fast. After a thermal protection event has expired, the DCP3601 restarts with a new soft-start.

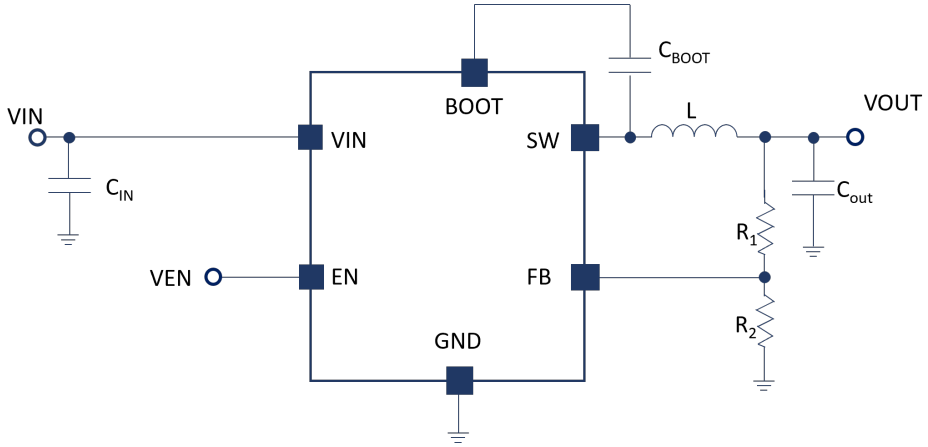
7 Application information

The DCP3601 is a buck DC-to-DC converter. It is typically used to convert a higher input voltage to a lower output DC voltage with a maximum output current of 1 A. The following design procedure can be used to select components for the DCP3601.

7.1 Typical application

The device only requires a few external components to convert from a wide voltage range supply to a fixed output voltage. The figure below shows a basic schematic.

Figure 4. DCP3601 application schematic



7.2 Output voltage setting

The error amplifier reference voltage is 0.85 V typical (refer to Table 7). The output voltage is adjusted accordingly with the following equation:

$$V_{OUT} = 0.85 \cdot \left(1 + \frac{R_1}{R_2}\right) \quad (8)$$

7.3 Input capacitor selection

The input capacitor voltage rating must be higher than the maximum input operating voltage of the application. During the switching activity a pulsed current flows into the input capacitor, and so its RMS current capability must be selected according to the application conditions. Internal losses of the input filter depend on the ESR value, so low ESR capacitors (such as multilayer ceramic capacitors) usually have a higher RMS current capability. On the other hand, given the RMS current value, a lower ESR input filter has lower losses and so contributes to higher conversion efficiency.

The maximum RMS input current, flowing through the capacitor, can be calculated as follows:

$$I_{RMS} = I_{OUT} \cdot \sqrt{\left(\left(1 - \frac{D}{\eta}\right)\frac{D}{\eta}\right)} \quad (9)$$

Where I_{OUT} is the maximum DC output current, D is the duty cycles, η is the efficiency. This function has a maximum at D = 0.5 and, considering η = 1, it is equal to $I_{OUT}/2$. In a specific application, the range of possible duty cycles has to be considered in order to find out the maximum RMS input current. The maximum and minimum duty cycles can be calculated as:

$$D_{MAX} = \frac{V_{OUT} + \Delta V_{LOW\_side}}{V_{IN\_min} + \Delta V_{LOW\_side} - \Delta V_{HIGH\_side}} \quad (10)$$

$$D_{MIN} = \frac{V_{OUT} + \Delta V_{LOW\_side}}{V_{IN\_max} + \Delta V_{LOW\_side} - \Delta V_{HIGH\_side}} \quad (11)$$

Where $\Delta V_{HIGHSIDE}$ and $\Delta V_{LOWSIDE}$ are the voltage drops across the embedded switches. The peak-to-peak voltage across the input filter can be calculated as the equation below:

$$V_{PP} = \frac{I_{OUT}}{C_{IN} \cdot F_{SW}} \cdot \left(1 - \frac{D}{\eta}\right)\frac{D}{\eta} + ESR \cdot (I_{OUT} + \Delta I_L) \quad (12)$$

In case of negligible ESR (MLCC capacitor), the equation of C_{IN} as a function of the target V_{PP} can be written as follows:

$$C_{IN} = \frac{I_{OUT}}{(V_{PP} \cdot F_{SW})} \cdot \left(1 - \frac{D}{\eta}\right)\frac{D}{\eta} \quad (13)$$

Considering η = 1 this function has its maximum in D = 0.5:

$$C_{IN\_min} = \frac{I_{OUT}}{(4 \cdot V_{PP\_max} \cdot F_{SW})} \quad (14)$$

Typically, C_{IN} is dimensioned to keep the maximum peak-to-peak voltage across the input filter in the order of 5% V_{INMAX}.

7.4 Inductor selection

The inductor current ripple flowing into the output capacitor determines the output voltage ripple. The inductor value is usually selected in order to keep the current ripple lower than 20% - 40% of the output current over the input voltage range. The inductance value can be calculated by the following equation:

$$\Delta I_L = \frac{V_{IN} - V_{OUT}}{L} \cdot t_{ON} = \frac{V_{OUT}}{L} \cdot t_{OFF} \quad (15)$$

Where T_{ON} and T_{OFF} are the on and off-time of the internal power switch. The maximum current ripple at fixed V_{OUT} is obtained at maximum T_{OFF}, which is at minimum duty cycle. So fixing ΔI_L = 20% to 40% of the maximum output current, the minimum inductance value can be calculated:

$$L_{min} = \frac{V_{OUT}}{\Delta I_{L\_max}} \cdot \frac{1 - D_{min}}{F_{SW}} \quad (16)$$

The peak current through the inductor is given by:

$$I_{L\_peak} = I_{OUT} + \frac{\Delta I_L}{2} \quad (17)$$

So if the inductor value decreases, the peak current (that has to be lower than the current limit of the device) increases. The higher the inductor value, the higher the average output current that can be delivered, without reaching the current limit.

7.5 Output capacitor selection

The triangular shape current ripple (with zero average value) flowing into the output capacitor gives the output voltage ripple, which depends on the capacitor value and the equivalent resistive component (ESR). Therefore, the output capacitor has to be selected in order to have a voltage ripple compliant with the application requirements.

The voltage ripple equation can be calculated as:

$$\Delta V_{OUT} = ESR \cdot \Delta I_{L\_max} + \frac{\Delta I_{L\_max}}{(8 \cdot C_{OUT} \cdot F_{SW})} \quad (18)$$

For a ceramic (MLCC) capacitor, the capacitive component of the ripple dominates the resistive one. While for an electrolytic capacitor the opposite is true. Neglecting the ESR contribution the minimum value of the output capacitor is given by:

$$C_{OUT\_\min\_RIPPLE} = \frac{\Delta I_{L\_max}}{(8 \cdot \Delta V_{OUT} \cdot F_{SW})} \quad (19)$$

As the compensation network is internal, the output capacitor should be selected in order to have a proper phase margin and then a stable control loop.

7.6 Board layout guidelines

The DC-DC converter area is very sensitive, and it is necessary to pay attention to the layout of this part.

The DC-DC converter generates GND noise that can get coupled on the surrounding ground reducing the sensitivity, and high-frequency components can be coupled onto the RF part. Therefore, to ensure a correct layout, it is necessary to:

- Provide efficient filtering by placing capacitors as close as possible
- Reduce parasitic ensuring wide and short connections.

A two-layer or a four-layer board is strongly recommended. Put the ground layer very close to the top layer to obtain a good ground plane reference. A minimum copper thickness for each layer of 0.035 mm (1 oz) is suggested.

Put a ground plane internally to reduce the coupling between the traces. If it is not possible to use a four-layer board, it is necessary to fill the area under the phase node of the board with ground metal to reduce or eliminate radiation emissions.

Ground plane

Any switch-mode power supply requires a good PCB layout in order to achieve the maximum performance.

Component placement, and GND trace routing and width are the major issues. Basic rules commonly used for DC-DC converters for good PCB layout should be followed. All traces carrying current should be drawn on the PCB as short and as thick as possible. This should be done to minimize resistive and inductive parasitic effects and increase system efficiency.

Connect all the ground metallization and/or layers with as many vias as possible. Ground vias between layers should be added liberally throughout the RF portion of the PCB. This helps prevent the accrual of parasitic ground inductance due to ground-current return paths. The vias also help to prevent cross-coupling from the RF and other signal lines across the PCB.

Capacitor placing

Particular care has to be taken in the placement of the supply voltage filtering capacitors. It is, in fact, important to ensure efficient filtering by placing these capacitors as close as possible from their dedicated pins.

The layout of decoupling capacitors is extremely important to minimize the induction loop formed between the capacitor and the IC power and ground. The vias should be placed on the side of the capacitor lands, not the ends. The vias should be located at the minimum keep-out distance and connected to the capacitor lands with a wide trace - at least as wide as the via pad. Vias of opposite polarity should be placed as close together as possible (minimum keep-out distance) and vias of the same polarity should be kept separated as much as possible. If space allows, a second pair of vias on the opposite side of the capacitor may be added to reduce the inductance further.

Inductor placing

The DC-DC converter inductor has to be placed as close as possible with traces as short and as thick as possible. This should be done to minimize resistive parasitic effects and increase system efficiency.

Feedback resistor placing

It is important to place the resistor divider close to the FB pin to reduce noise sensitivity of the output voltage feedback path. Route the V_{OUT} sense path away from noisy nodes and preferably through a layer on the other side of a shielded layer.

Thermal aspects

The device power dissipation inside the IC is mainly due to the DC-DC integrated MOSFET power loss. The heat generated due to this power dissipation level requires a suitable heat sink to keep the junction temperature below the overtemperature protection threshold (Thermal Shutdown) at the rated ambient temperature. Try, where possible, to increase the number of power planes connected to improve the heat dissipation.

However, different layouts are also possible. Basic principles suggest keeping the IC in the middle of the dissipating area; to provide as many vias as possible; to design a dissipating area having a shape as square as possible and not interrupted by other copper traces.

8 Typical performance characteristics

Figure 5. DCP3601 - Efficiency (V_{IN} = 24 V)

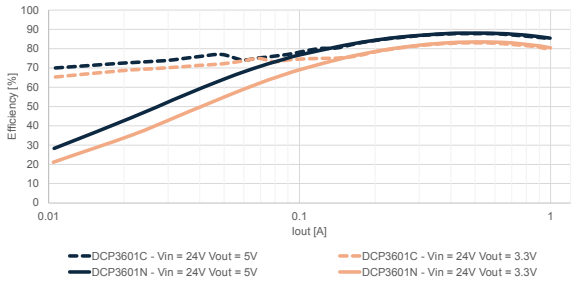


Figure 6. DCP3601 - Efficiency (V_{IN} = 12 V)

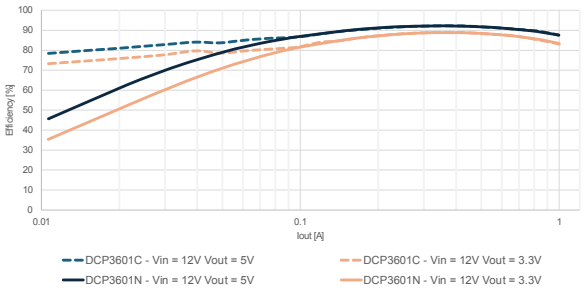


Figure 7. DCP3601C - LCM operation at no load V_{IN} = 24 V, V_{OUT} = 5 V, NO LOAD

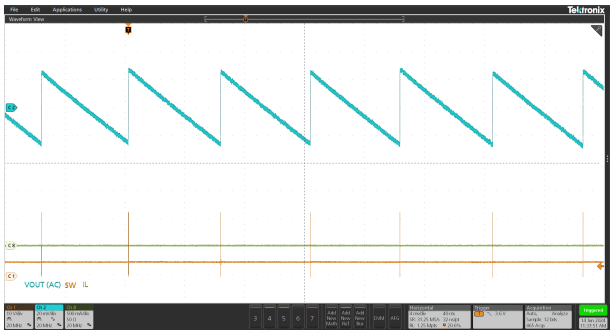


Figure 8. DCP3601C - LCM operation at medium load V_{IN} = 24 V, V_{OUT} = 5 V, I_{OUT} = 500 mA

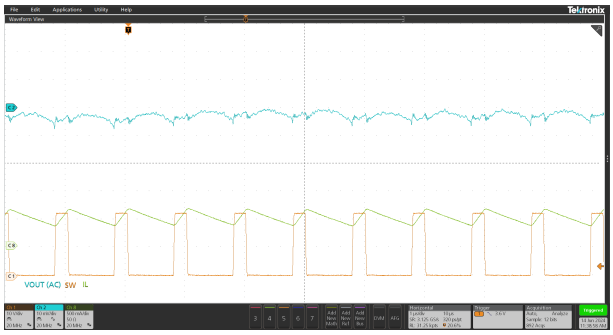


Figure 9. DCP3601C - SOFT-START phase V_{IN} = 24 V, V_{OUT} = 5 V, R_LOAD = 5 Ω

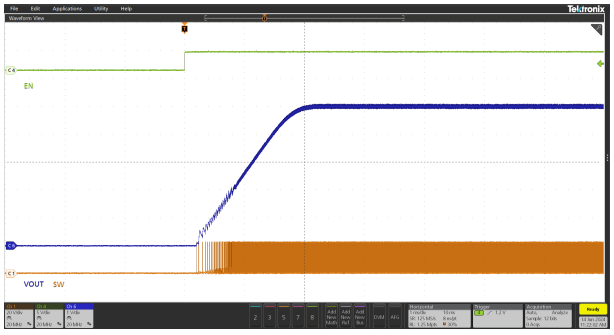
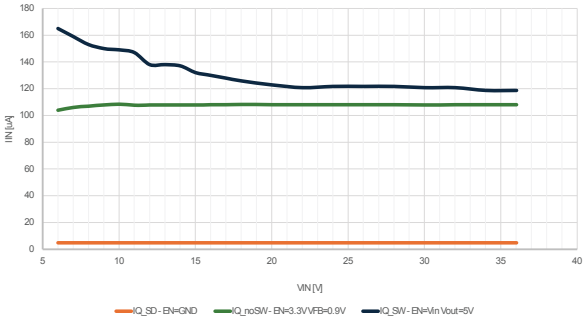


Figure 10. DCP3601C - Supply current vs. V_{IN} - No load



9 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

9.1 SOT23-6L package information

Figure 11. **SOT23-6L package outline**

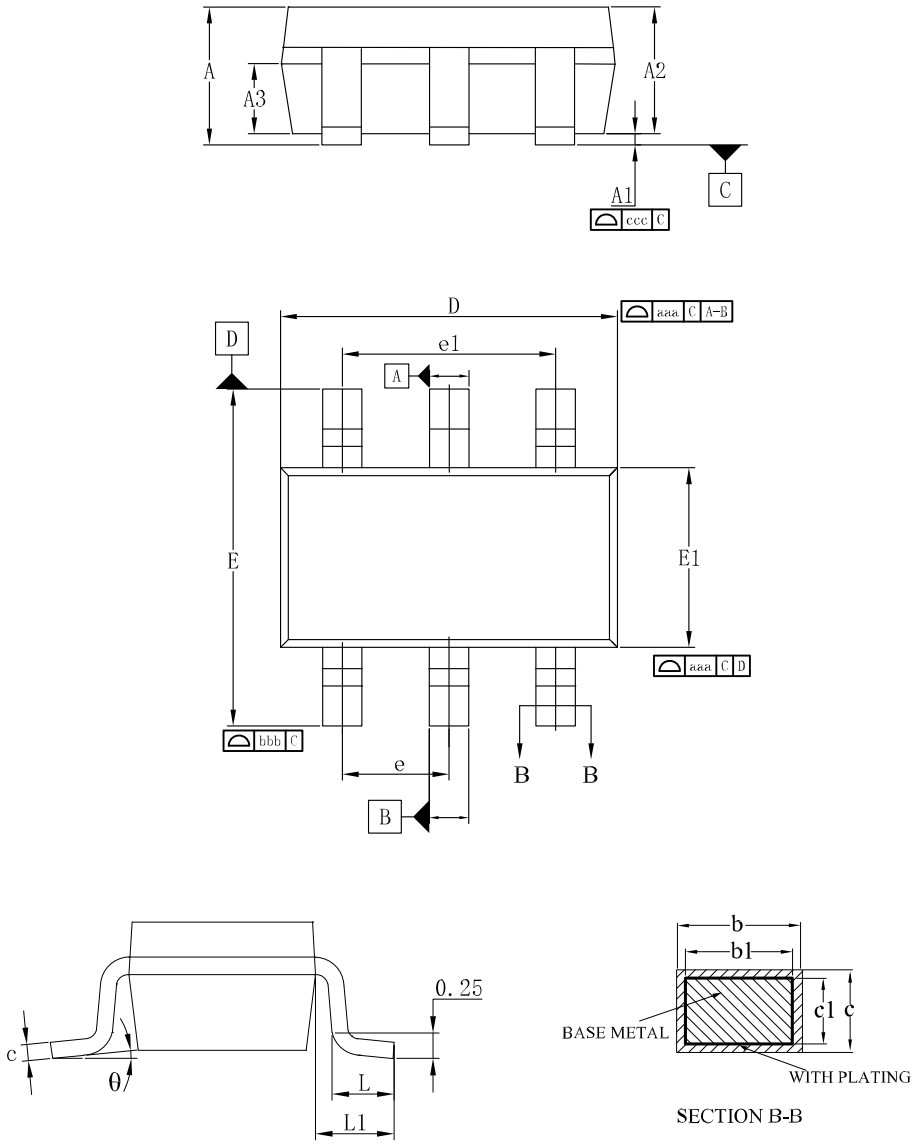
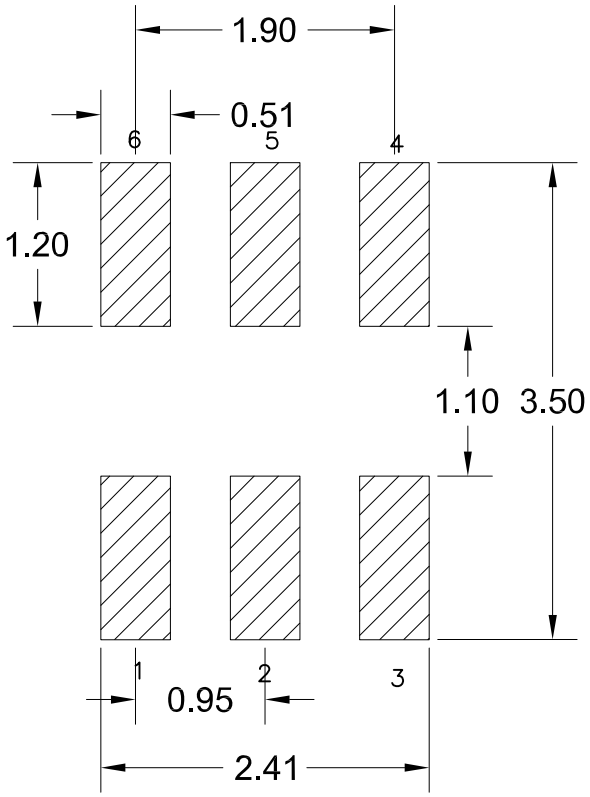


Table 8. **SOT23-6L mechanical data**

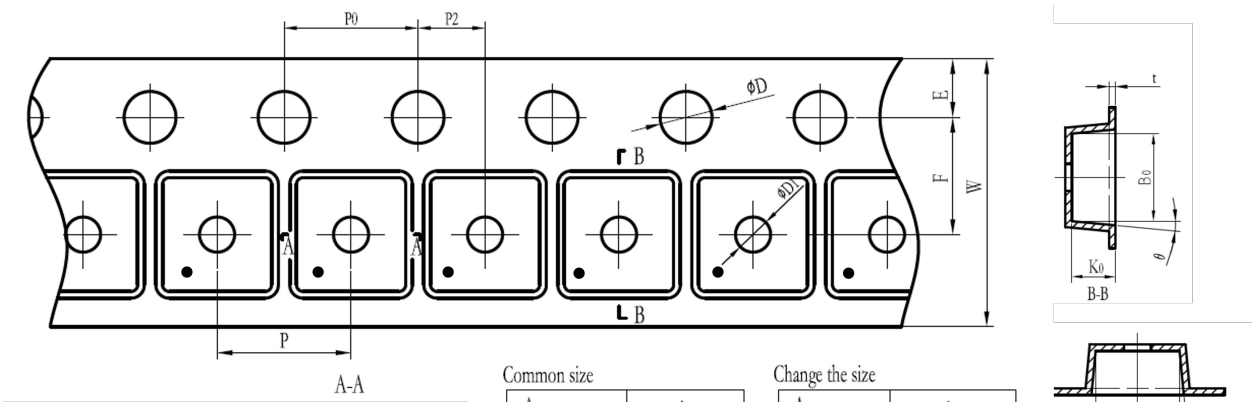
Dimensions			
Symbol	Millimeters		
	Min.	Typ.	Max.
A			1.25
A1	0.02		0.10
A2	1.00	1.10	1.20
A3	0.60	0.65	0.70
b	0.33		0.41
b1	0.32	0.35	0.38
c	0.15		0.19
c1	0.14	0.15	0.16
D	2.82	2.92	3.02
E	2.60	2.80	3.00
E1	1.50	1.60	1.70
e	0.95 BSC		
e1	1.90 BSC		
L	0.30		0.60
L1	0.60 REF		
α	0°		8°
	Tolerance		
aaa	0.15		
bbb	0.20		
ccc	0.10		

Figure 12. **SOT23-6L recommended footprint**



9.2 SOT23-6L package information

Figure 13. **SOT23-6L carrier tape outline**



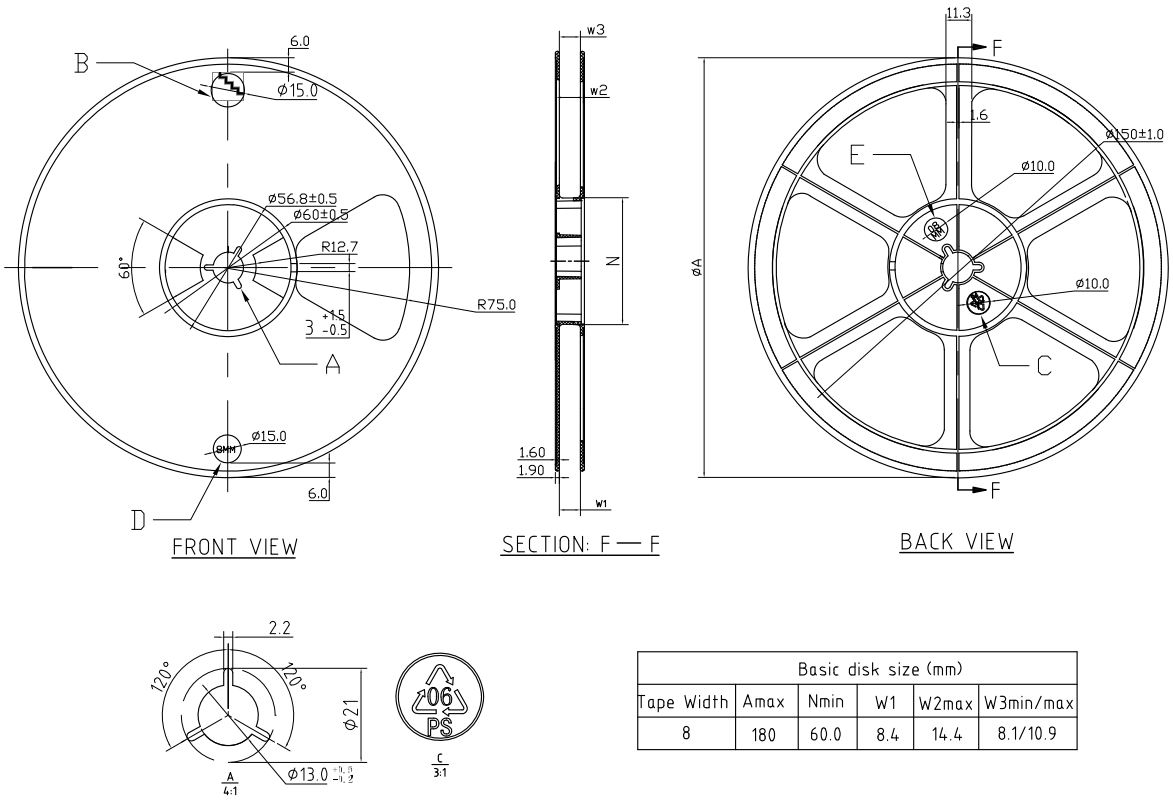
Common size

Appearance	size
E	1.75±0.10
F	3.50±0.05
P2	2.00±0.05
D	$1.50^{+0.10}_{-0}$
D1	1.05±0.05
P0	4.00±0.10
10P0	40.0±0.20

Change the size

Appearance	size
W	8.00±0.10
P	4.00±0.10
A0	3.26±0.10
B0	3.30 ±0.10
K0	1.40±0.10
t	0.20±0.02
θ	3° -5° TYP

Figure 14. **SOT23-6L reel outline**



Basic disk size (mm)					
Tape Width	Amax	Nmin	W1	W2max	W3min/max
8	180	60.0	8.4	14.4	8.1/10.9

10 Ordering information

Table 9. **Order codes**

Order codes	Marking	Light-load behavior	Dithering	Package	Packing
DCP3601CMR	01C	LCM (Low consumption mode)	No	SOT23-6L	Tape and reel
DCP3601NMR	01N	LNM (Low noise mode)	No		
DCP3601CDMR	01CD	LCM (Low consumption mode)	Yes	SOT23-6L	Tape and reel
DCP3601NDMR	01ND	LNM (Low noise mode)	Yes		

Revision history

Table 10. **Document revision history**

Date	Revision	Changes
16-Dec-2024	1	Initial release.

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