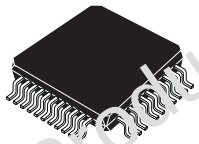
L6246

12V VOICE COIL MOTOR DRIVER

- 12V (±10%) OPERATION
- 3A MAXIMUM CURRENT CAPABILITY
- 0.3Ω MAXIMUM ON RESISTANCE OF EACH POWER DMOS AT A JUNCTION TEMPERATAURE OF 25°C
- CLASS AB POWER AMPLIFIERS
- LOGIC AND POWER SUPPLY MONITOR
- POWER ON RESET
- PARKING FUNCTION WITH SELECTABLE RETRACT VOLTAGE AND DYNAMIC BRAKE BEFORE PARKING
- ENABLE FUNCTION
- GATE DRIVER FOR EXTERNAL BLOCKING N-MOSFET
- OVERTEMPERATURE PROTECTION
- OVERTEMPERATURE WARNING OUTPUT
- PQFP44 PACKAGE

MULTIPOWER BCD TECHNOLOGY



PQFP44 (10x10)

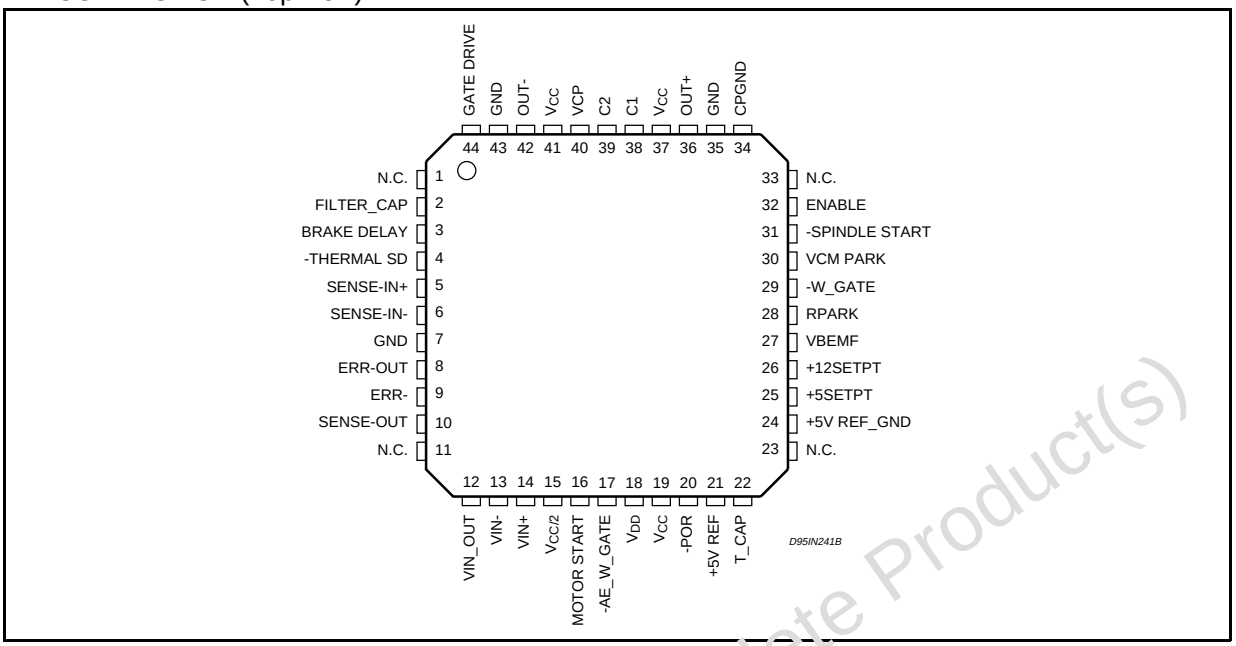
DESCRIPTION

The voice coil driver L6246 is a linear power amplifier designed to drive single phase bipolar DC motors for hard disk drive applications. The device contains a selectable transconductance loop, which allows high precision for head positioning. The power stage is composed of 2 power amplifiers, in AB class, with 4 DMOSs, with Rdson of 0.5Ω (Sink+Source) maximum, in a H-bridge configuration. Drive voltage for the upper DMOS FETs is provided by a charge pump circuit to ensure low Rdson.

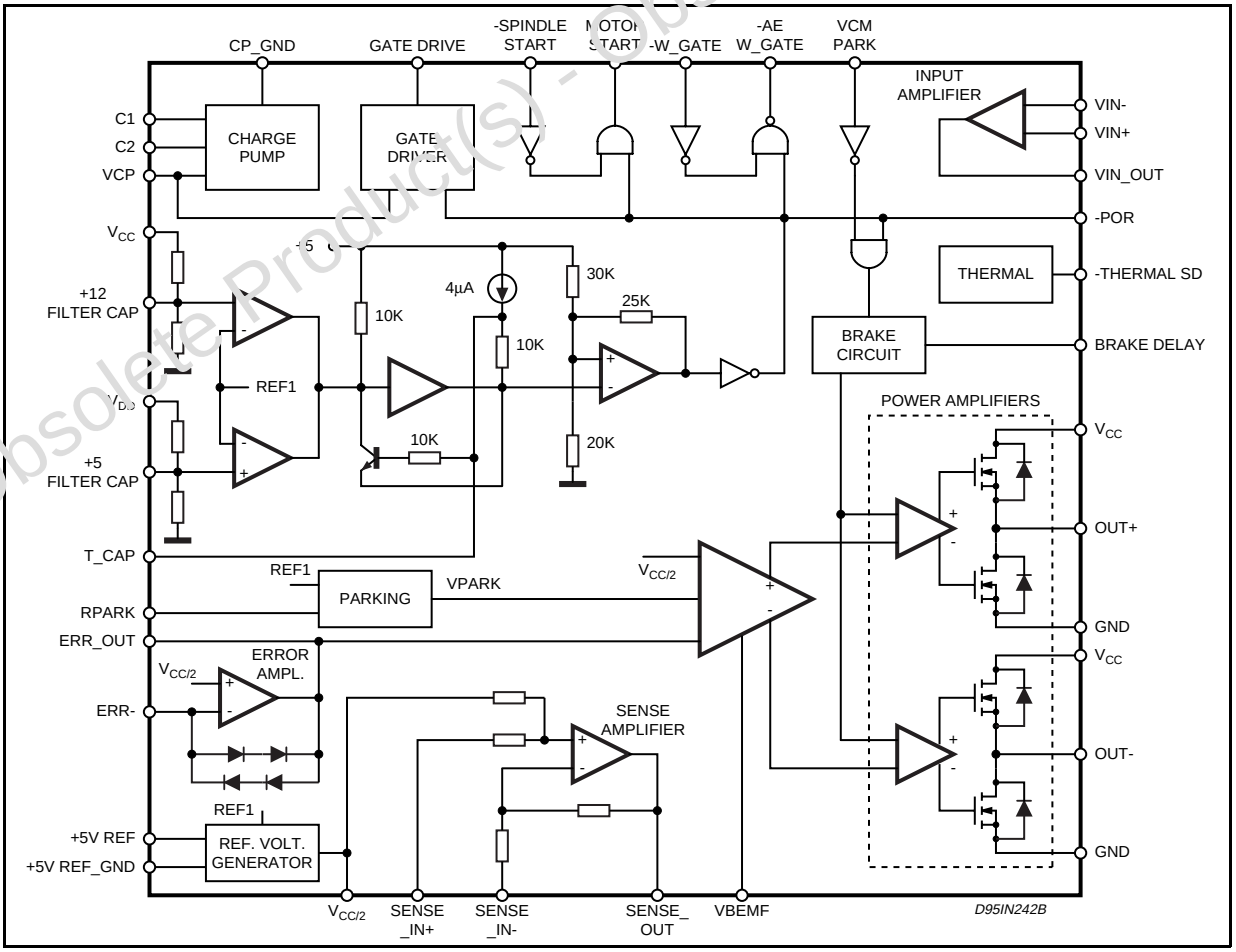
Automatic brake and parking of the head actuator is performed by logic or when a failure condition is detected by power supply monitors. An external resistor programs the parking voltage that enables the head retract. In addition, a 5V stable output is provided for the external usage, and a gate driver circuit enables an external power supply isolation N-MOSFET.

This device is built in BCD II technology allowing dense digital circuitry to be combined with high power bipolar power devices and is assembled in PQFP44.

PIN CONNECTION (Top view)



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_{pow.\ max.}$	Maximum supply voltage	15	V
$V_{digital\ max.}$	Maximum supply voltage	7	V
$V_{in\ max.}$	Maximum input voltage	$V_{digital}$ ±0.3	V
$V_{in\ min.}$	Minimum input voltage	GND - 0.3	V
I_{peak}	Peak sink/source output current	3	A
I_{dc}	DC sink/source output current	1.7	A
P_{tot}	Maximum total power dissipation	≅1.7	W
T_{op}	Operative temperature range	0 to 80	°C

THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{th\ j\text{-}case}$	Thermal resistance junction to case	≅20	°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction to ambient mounted on standard PCB (*)	≅60	°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction to ambient mounted on PCB (**)	≅35	°C/W

(*) Standard board construction: single layer (1S 0P); size 100mm long by 100mm wide.
(**) The board construction includes: a 6 layer board (2S 4P, with power planes ≅80%); size 100mm long by 99mm wide; package location near middle point of lenght and one third of width.

PIN FUNCTIONS

Pin	Name	Description
1	N.C.	Not Connected.
2	Filter_cap	Filter capacitor for 10V internal regulator. The capacitor is optional.
3	Brake Delay	Voice Coil Motor brake delay capacitor.
4	-Thermal SD	Pre Thermal Shut Down indication Output.
5	Sense_in+	Non inverting Input of Sense Amplifier.
6	Sense_in-	Inverting Input of Sense Amplifier.
7	Gnd	Ground.
8	Err_out	Error Amplifier Output.
9	Err-	Inverting Input of Error Amplifier.
10	Sense_out	Output of Sense Amplifier.
11	N.C.	Not Connected.
12	Vin_out	Output of Input Amplifier.
13	Vin-	Inverting Input of Input Amplifier.
14	Vin+	Non inverting Input of Input Amplifier.
15	+Vcc/2	Half Supply Voltage reference.
16	+Motor start	Motor start Output to Spindle Controller.
17	-AE_W_Gate	Write Gate Output to AE.
18	+Vdd	+5V Supply.
19	+Vcc	+12V Supply.
20	-POR	Power On Reset. Low will signal the failure of the logic supply or 12V supply
21	+5V Ref	+5V Reference Output from the Voltage Reference Regulator.
22	T_cap	Power On Reset Timing Capacitor. The capacitor sets the POR delay.
23	N.C.	Not Connected.
24	+5V Ref Gnd	Ground for Voltage Reference Generator.
25	+5Setpt	+5V Monitor Set Point and filtering

PIN FUNCTIONS (continued)

Pin	Name	Description
26	+12Setpt	+12V Monitor Set Point and filtering
27	Vbemf	Input BEMF from spindle motor for parking circuit.
28	Rpark	Resistor for setting the park voltage.
29	-W_Gate	Write Gate Input.
30	+VCM park	External input for parking. High will activate the park procedure.
31	-Spindle_start	Spindle Start input.
32	+Enable	Input. logic low will disable only the IC.
33	N.C.	Not Connected.
34	Cpgnd	Charge Pump Ground.
35	Gnd	Ground.
36	Out+	Power Amplifier Output.
37	Vcc	+12V Power Supply.
38	C1	Charge Pump Oscillator Output.
39	C2	Input for external Charge Pump Capacitor.
40	Vcp	Output for Charge Pump Storage Capacitor.
41	Vcc	+12V Power Supply.
42	Out-	Power Amplifier Output.
43	Gnd	Ground.
44	Gate Drive	Gate Drive for External Isolation N-MOSFETS.

ELECTRICAL CHARACTERISTICS (T_j = 25°C, Vdd = 5V, Vcc = 12V; unless otherwise specified.)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Vcc	Analog/Power supply voltage range		10.8	12	13.2	V
Vdd	Digital supply voltage range		4.5	5	5.5	V
Idd	Digital supply quiescent current	Output ENABLED		5		mA
Idd	Digital supply quiescent current	Output DISABLED		5		mA
Icc	Power supply quiescent current	Output ENABLED		20		mA
Icc	Power supply quiescent current	Output DISABLED		10		mA
THERMAL SHUT DOWN DATA						
T_{h_SD}	Shut down Temperature		135	160		°C
$T_{h\_SD\_H}$	Shut down hysteresys			25		°C
T_{h_Warn}	Pre Shut down alarm		115	140		°C
	Pre Shut down alarm hysteresys			15		°C
EXTERNAL N-MOSFET GATE DRIVER						
Vll	Low level voltage				500	mV
Vhl	High level voltage		Vcc+4			V
Isink	Current sinking capability		4			mA
Isource	Current source capability			0.5		mA
POWER ON RESET AND GATE SPECIFICATION						
$V_{dd\_und\_th}$	Digital undervoltage threshold		3.8	4.1	4.45	V
$V_{cc\_und\_th}$	Power undervoltage threshold		8.5	9.25	10.0	V
POR_{to}	POR timeout	Cpor = 1µF	375	500	625	ms
$POR_{\_delay}$	Time delay for POR Active				1	µs
$V_{dd\_POR\_T\_R}$	Power supply POR thereshold Resistance		10			KΩ

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
$V_{CC\_POR\_T\_R}$	Logic supply POR thereshold Resistance		10			KΩ
I_{POR_O}	POR output current drive		4			mA
LOGIC INTERFACE VOLTAGE LEVEL (All digital inputs are CMOS compatible)						
Voh	CMOS high level output voltage	Iout = 1.0mA	4.10			V
Vol	CMOS low level output voltage	Iout = 1.0mA			0.40	V
Vih	TTL high level input voltage		2			V
Vil	TTL low level input voltage				0.80	V
5V REFERENCE GENERATOR						
Vref	Voltage reference at Power On		4.75	5.00	5.25	V
Drift	Drift from Power On		-2		+2	%
loref	Current output		10			mA
INPUT AMPLIFIER						
Vi	Input voltage range		Vref (-)		Vref (+)	V
Vcm	Input common mode voltage range		0		5.00	V
Vds	Input differential voltage swing		-5		+5	V
Vos	Input offset voltage		-5		+5	mV
Ib	Input Bias current		-500		+500	nA
Gv	Open Loop voltage Gain		80			dB
SR	Output slew rate		0.6			V/µs
GBW	Gain bandwidth product		1			MHz
PSRR	Power supply rejection ratio		80			dB
Vo	Output voltage swing		9			V
ERROR AMPLIFIER						
Vi	Input voltage range		$V_{CC}/2$ -0.5		$V_{CC}/2$ +0.5	V
Vos	Input offset voltage		-5		+5	mV
Ib	Input Bias current		-500		+500	nA
Gv	Open Loop voltage Gain		80			dB
SR	Output slew rate		0.6			V/µs
GBW	Gain bandwidth product		1			MHz
PSRR	Power supply rejection ratio		80			dB
Vo	Output voltage swing		$V_{CC}/2$ -2Vbe		$V_{CC}/2$ +2Vbe	V
SENSE AMPLIFIER						
Vi	Input voltage range		Gnd		Vcc	V
Vos	Input offset voltage		-6		+6	mV
Ii	Input sink and source current		-1.5		+1.5	mA
PSRR	Power supply rejection ratio		50			dB
Gv	Vloltage gain		9.9	10	10.1	V/V
Rin	Differential input resistance		3			KΩ
GBW	Gain bandwidth product		1			MHz
Vli	Linear differential input voltage range	Gv = 10(V/V)	-0.35		+0.55	V
CMRR	Common mode rejection ratio		56			dB

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
POWER AMPLIFIER						
Rdson	DMOS on resistance	at 25°C			0.3	Ω
Gdv	Differential voltage gain			32		V/V
Iol	Output current leakage				500	µA
SR	Output slew rate		0.4			V/µs
Tsr	Saturation recovery time				5	µs
GBW	Gain bandwidth product		100			KHz
RETRACT						
Vr	Max. retract voltage	Vcc shorted to GND			300	mV
Vr	Max. retract voltage	Vcc Normal			1	V
CHARGE PUMP						
Cs	Storage capacitor				1	µF
Vs	Storage voltage		Vcc +4			V
Cp	Pump capacitor				0.2	µF

RETRACT TRUTH TABLE

	Input	Input	Output	Output
	-Retract	+Enable	Bridge Enable	+Retract
Brake and Retract	0	X	0	1
Run	1	1	1	0
Disable	1	0	0	0

BLOCK DESCRIPTION

POWER AMPLIFIERS

The two power amplifiers are connected in bridge configuration working in AB class.

SENSE AMPLIFIER

This stage senses the voltage drop across the Rsense.

The input stage is supplied by the charge pump voltage to have an high dynamic, while the other sections of the amplifier are supplied by the voltage of 10.5V internally regulated to have an high power supply rejection (this voltage, supplies also the error amplifier, the input amplifier and the operational amplifier which generates the Vcc/2 voltage).

The open loop gain is around 80dB and the bandwith is more than 1MHz.
The voltage gain is fixed internally at 10 V/V.

ERROR AMPLIFIER

This is the stage which compares the input voltage and the sense voltage, generating the control voltage for the power section.

The open loop gain and bandwith of this amplifier are similar to the sense amplifier.

The negative input and the output of the error amplifier are accessible externally in order to have the current loop compensation user configurable.

The dynamic of the output is limited at +/- 2Vbe to have a faster response of the output voltage.

INPUT AMPLIFIER

The inputs and the output pins are externally accessible to have the possibility to configure the transconductance gain of the current control loop selecting the voltage gain of this amplifier.

The open loop gain and bandwith of this amplifier are similar to the sense amplifier.

REFERENCE VOLTAGE GENERATOR

This block generates the two reference voltage **Vcc/2** and +5**VREF**.

The Vcc/2 voltage is used as reference by the current control loop.
The +5VREF is a very stable voltage generator that can be used as reference voltage of an external **DAC**.

POWER SUPPLY MONITOR

This circuit monitors the logic supply (5V) and the power supply (12V) and activates the power on reset output (POR) and the VCM PARK circuit.
After both logic and power supply reach their nominal value a timing capacitor (T_CAP) has to be charge before the POR output change from low to high level.

$$\text{POR delay} = \frac{C \cdot V}{I}$$

where:

- **C** is the capacitor value connected at pin T_CAP
- **V** is delta voltage that capacitor have to be charged (2.3V)
- **I** is the costant current charging the capacitor (4µA typ.)

At the two input pins, +12 FILTER CAP and + 5 FILTER CAP, can be connected two capacitors for filtering the noise on the power supply, avoiding in this case undesired commutations of the POR signal because of some fast negative spikes on the line.

BRAKE AND PARKING CIRCUITS

The voice coil driver is switched into the parking condition through the VCM PARK input or when the POR signal is low. In such condition immediately the output stage turns on the two lower DMOS of the power bridge to activate the BRAKE of the voice coil motor.
After a delay generated by the capacitor at the BRAKE DELAY pin, only one of the two lower DMOS stays on while the opposite half bridge is tristated.

$$\text{BRAKE delay} = \frac{C \cdot V}{I}$$

where:

- **C** is the capacitor value connected at pin BRAKE DELAY
- **V** is delta voltage that capacitor have to be charged (3V)
- **I** is the costant current charging the capacitor (5µA typ.)

The parking voltage is then supplied by the PARKING circuit connected to the output that has been tristated.
The value of such a voltage is set by connecting an external resistor between the RPARK pin and ground.

$$V_r = \frac{Vbandgap \cdot 10^4}{Rpark}$$

where:

Vr is the retract voltage for parking the heads

Vbandgap is the internal bandgap reference voltage of 1.4V

Rpark is value of the resistor connected at RPARK pin

The parking circuit takes the power supply from the spindle driver through the VBEMF pin, so that in case of power fail the retract of the heads is possible using the rectified BEMF voltage coming from the spindle motor.

CHARGE PUMP

The charge pump circuit is used as a means of almost doubling the power supply voltage (12V) in order to drive the upper DMOS of the power bridge.
The energy stored in the in the capacitor connected at VCP pin is also used to drive the gate of the external N-MOSFET.

GATE DRIVER

This circuit provide the voltage driving the gate of the external isolation N-MOSFET, and it is controlled by the POR signal.

THERMAL

The thermal protection circuit has two threshold, the first if the pre shut down alarm that activates the THERMAL SD signal and the second is the shut down temperature that tristates the output stage when the junction temperature increases over this level.

APPLICATION INFORMATION

Example of calculation of the error amplifier compansation for the stability of the current control loop. As can be seen from the draw of the current control loop circuit of the next page, the voltage across the load is:

#1

$V_L = A_{CPW} \cdot A_{CERR} \cdot (A_{CINP} \cdot V_{IN} - A_{CENSE} \cdot V_{sense})$

$V_{sense} = Rs \cdot I_L$

$V_L = (Z_L + Rs) \cdot I_L$

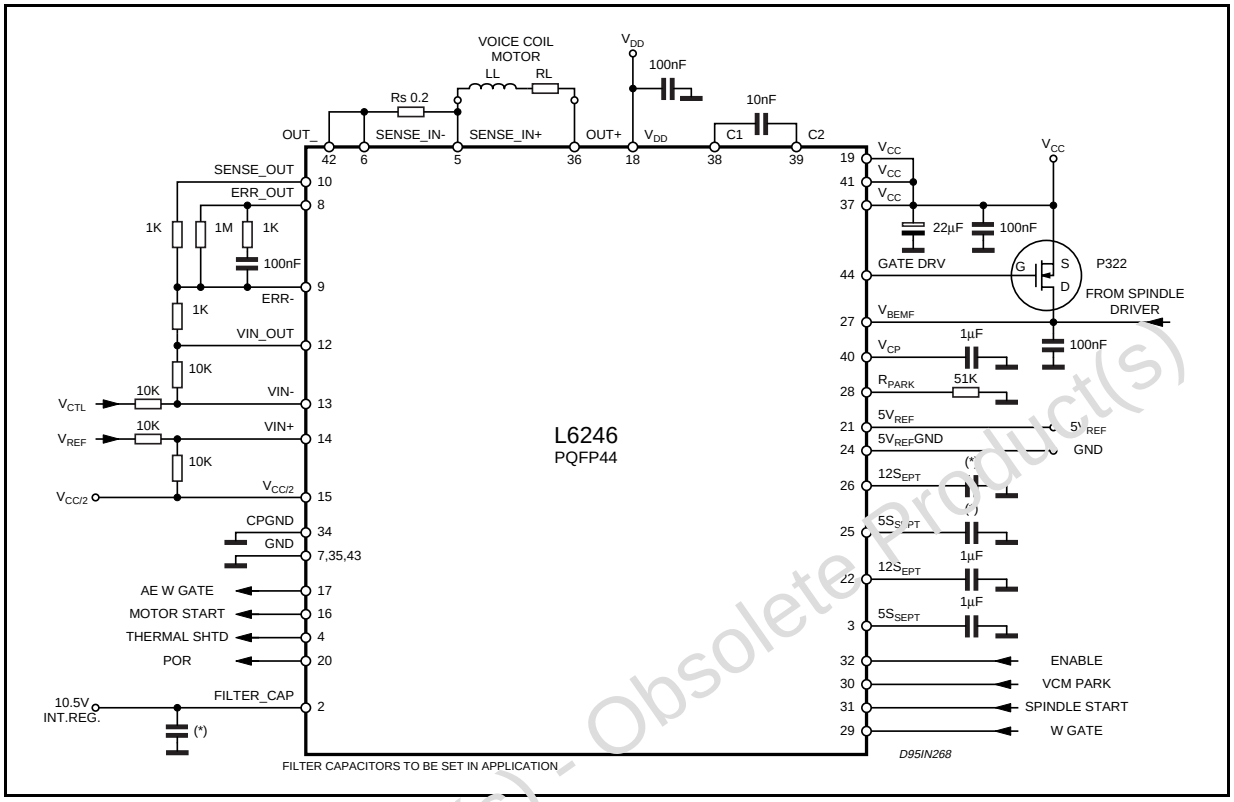
where A_C... is the closed loop gain of Power, Error, Sense and Input Amplifier.

Changing in the #1 the transfer function between the load current and the V_{IN} is:

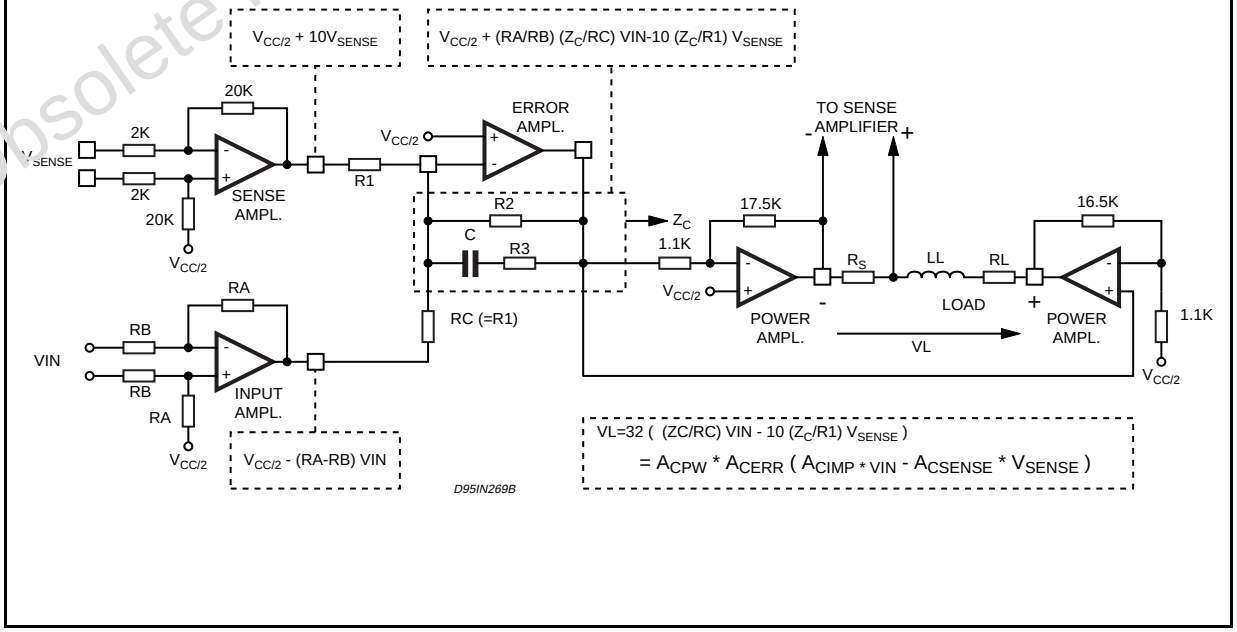
#2

$$\frac{I_L}{V_{IN}} = \frac{A_{CPW} \cdot A_{CERR} \cdot A_{CINP}}{Z_L + R_S + A_{CPW} \cdot A_{CERR} \cdot A_{CSENSE} \cdot R_S}$$

Typical Application Circuit



Current Control Loop Circuit



If Now We Define:

#3

$$Aloop = A_{CPW} \cdot A_{CERR} \cdot A_{CSENSE} \cdot \frac{R_S}{R_S + Z_L}$$

we obtain:

#4

$$\frac{I_L}{V_{IN}} = \frac{Aloop \cdot \frac{A_{CINP}}{A_{CSENSE}} \cdot \frac{1}{R_S}}{1 + Aloop}$$

Atlowfrequencyis:

$$Aloop = 32 \cdot \frac{R2}{R1} \cdot 10 \cdot \frac{R_S}{(R_S + Z_L)}$$

if R2 = 1M, R1 = 1K, R_S = 0.2, R_L = 7
then Aloop = 8889 = 80dB.

Being Aloop very high we can simplify the **#4** in this way:

$$\frac{I_L}{V_{IN}} = \frac{A_{CINP}}{A_{CSENSE}} \cdot \frac{1}{R_S} = \frac{1}{10 \cdot 0.2} = \frac{1}{2}$$

For the stability we have to study the stability of Aloop, that as we can see from the **#3** is a multiplication, so in dB is a sum:

$$Aloop\ |_{dB} = A_{CPW}\ |_{dB} + A_{CERR}\ |_{dB} + A_{CSENSE}\ |_{dB} + \frac{R_S}{R_S + Z_L}\Big|_{dB}$$

So we can take in consideration the BODE diagrams of the each operational amplifier, with particular attention to the Error amplifier.

1) The Power amplifier is actually composed by two operational amplifiers in the way to have a gain of +16 and -16 (in voltage) respectevely, for a total of 32 = 30dB.
The point at -3dB is around 130KHz.

2) The Sense amplifier has a gain of 20dB with the point at -3dB around 210KHz.

3) The load introduce an attenuation of:

$20\log \frac{R_S}{R_S + R_L}$ = -31dB with R_S = 0.2 and R_L = 7

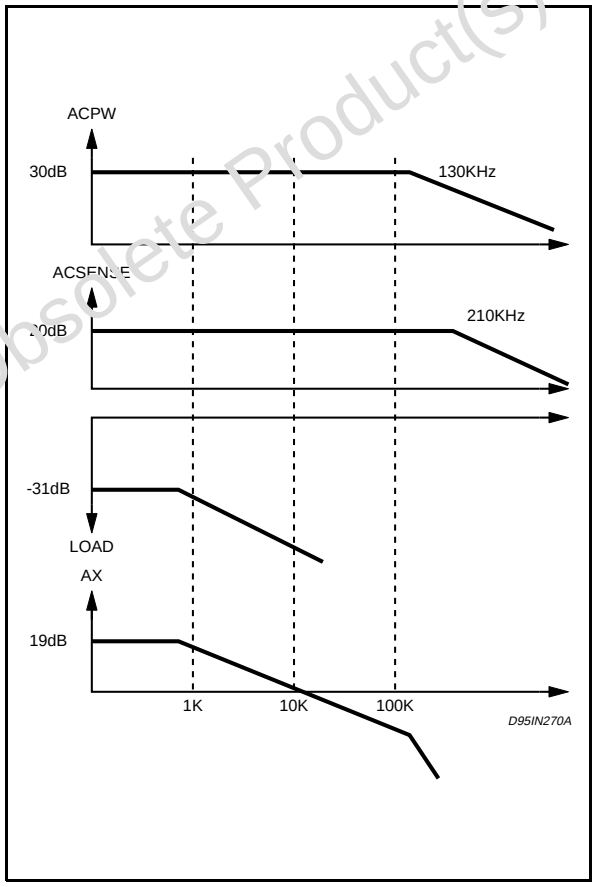
and its pole is at frequency $\frac{1}{2\pi L / (R_S + R_L)}$

so around 1KHz if **L = 1.2mH**.

So considering:

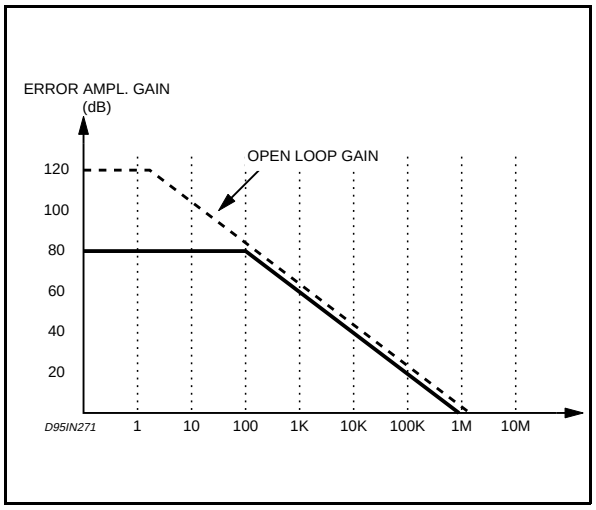
$$Ax\ |_{dB} = Aloop\ |_{dB} A_{CERR}\ |_{dB} A_{CPW}\ |_{dB} + A_{CSENSE}\ |_{dB} + \frac{R_S}{R_S + R_L}\Big|_{dB}$$

we have these Bode diagrams:



As can be easily see the bandwith is narrow and the gain is low. It is possible to increase both choosing an appropriate compensation of the Error amplifier.

The total bandwith should be, of course, at least a decade lower of the 130KHz to avoid instability problem. The bandwith guaranteed by the Error amplifier has a Gmax of 80dB and a gain of 0dB at 1MHz approximately, the real is some dB more with a larger bandwith.



Using the compensation network of the draw of pag.8, we have a error amplifier transfer function of:

$$\frac{V_O}{V_I} = -\frac{ZC}{R1} = -\frac{R2}{R1} \cdot \frac{1 + scR3}{1 + sc\,(R3 + R2)}$$

so:

$$Gmax\ (DC) = \frac{R2}{R1} = 1000 = 60dB$$

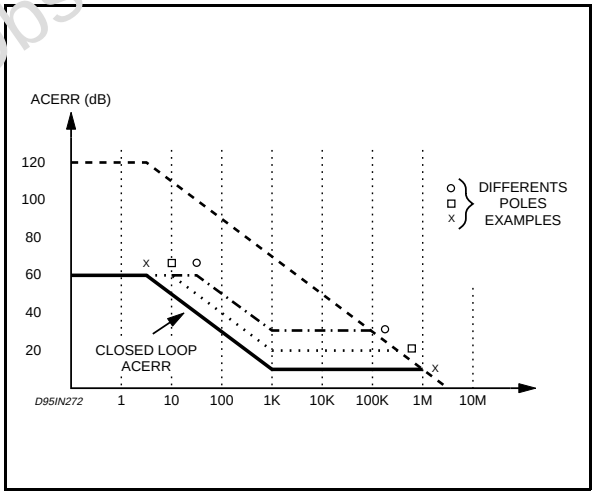
with R1 = 1MΩ and R2 = 1KΩ

$$zero = \frac{1}{2\,\pi\,R3C}$$

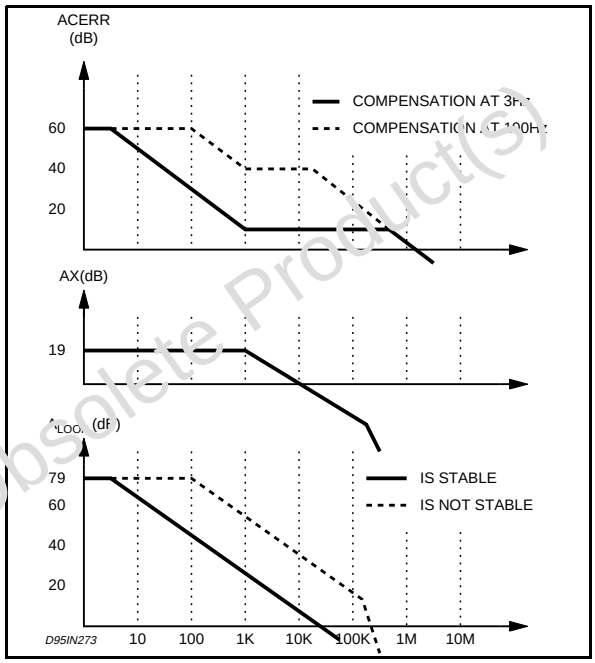
$$pole = \frac{1}{2\,\pi\,(R3 + R2)\,C}$$

Note: Fpole is lower than Fzero

The best choice is to cancel the pole of the load (at around 1KHz) with the zero of the compensation.



As can be seen the choice of the pole influence overall in fixing the gain at high frequency.
The gain at high frequency must be choosen in order to not create instability problem, because more higher is this gain and lower is the second pole that we have at high frequency.
If this pole is taken close to the other that we have already seen at 130KHz and 210KHz, instability problems can arise.
Adding together $AX\ |_{dB}$ and $A_{CERR}\ |_{dB}$ we obtaine the Aloop:



So the choice of the compensation network must be done in order to fix at the beginning the Gmax of the error amplifier depending on the ratio $\frac{R2}{R1}$.

To calculate the R3 and C values satisfying the following system:

$$\frac{1}{2\,\pi\,R3C} = \frac{\frac{1}{2\,\pi\,L}}{R_L + R_{sense}}$$

Error amplifier zero equal to load pole

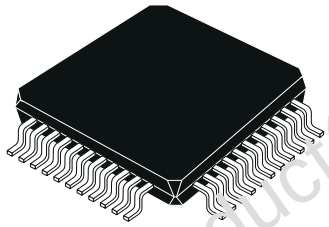
$$\frac{1}{2\,\pi\,(R3 + R2)C} = \frac{\text{Admissible Bandwith}}{\text{Gloop}} =$$

$$= \frac{\frac{130KHz}{10}}{8912} = 1.5Hz$$

This example is for crossing the 0dB one decade before the first pole of the Power Amplifier (130KHz), starting with a Gloop max of 79dB.

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.45			0.096
A1	0.25			0.010		
A2	1.95	2.00	2.10	0.077	0.079	0.083
B	0.30		0.45	0.012		0.018
c	0.13		0.23	0.005		0.009
D	12.95	13.20	13.45	0.51	0.52	0.53
D1	9.90	10.00	10.10	0.390	0.394	0.398
D3		8.00			0.315	
e		0.80			0.031	
E	12.95	13.20	13.45	0.510	0.520	0.530
E1	9.90	10.00	10.10	0.390	0.394	0.398
E3		8.00			0.315	
L	0.65	0.80	0.95	0.026	0.031	0.037
L1		1.60			0.063	
K	0°(min.), 7°(max.)					

OUTLINE AND MECHANICAL DATA



PQFP44 (10 x 10)