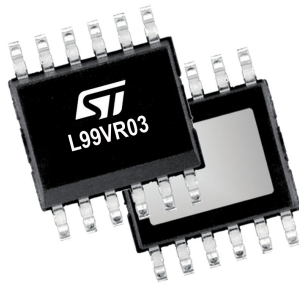


Automotive low dropout linear voltage regulator having 300 mA of current capability




PWSSO12
4.9x3.9x1.5 mm

Features

| | | |
|---------------------|----------|----------------------------|
| Max. supply voltage | V_S | 40 V |
| Output current | I_O | 300 mA |
| Quiescent current | I_{qn} | 800 nA ⁽¹⁾ |
| | | 3.5 μ A ⁽²⁾ |

1. Maximum value with regulator disabled.
2. Maximum value with regulator enabled.

- AEC-Q100 qualified 
- Wide input voltage operating range up to 40 V
- Low quiescent current consumption
- Output voltage options: 3.3 V or 5 V
- Output voltage precision $\pm 2\%$
- Enable input for enabling/disabling the voltage regulator
- Thermal shutdown and short-circuit current limitation
- Undervoltage-lockout UVLO
- Wide operating temperature range $T_J = -40\text{ }^\circ\text{C}$ to $175\text{ }^\circ\text{C}$
- Sustaining slow ramp-up applications
- Supply voltage rejection: $> 60\text{ dB}$ at 1 kHz
- Performant line and load regulation

Application

- Automotive MCU power supplies
- Body control modules
- Telematics control units
- Automotive head units
- Headlights

Description

L99VR03 is a low dropout linear voltage regulator designed for automotive applications available in PWSSO12 package. The LDO delivers up to 300 mA of load current and consumes as low as 800 nA of quiescent current when the regulator is disabled and only 3.5 μ A quiescent current at no load. The device is quite suitable for standby microprocessor control-unit systems, especially in automotive applications. The input voltage operating range is up to 40 V. The L99VR03 features enable. The L99VR03 is available in different output voltage options (3.3 V or 5 V). High output voltage accuracy ($\pm 2\%$) is kept over wide temperature range, line and load variation. The regulator output current is internally limited so that the device is protected against short-circuit, as it features over temperature protection.

Prerelease product(s)

Product status link

[L99VR03](#)

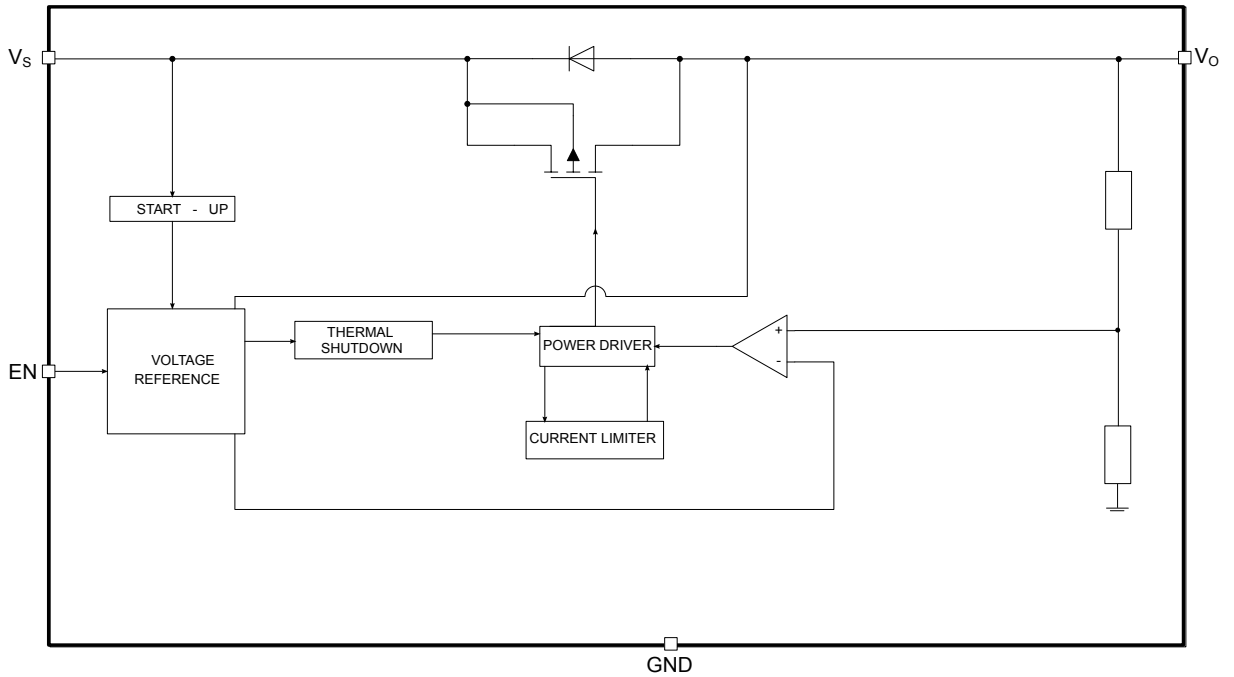
Product summary

| Order code | Package | Packing |
|-----------------------------|---------|---------------|
| 3.3 V output voltage | | |
| L99VR033PTR | PWSSO12 | Tape and reel |
| 5.5 V output voltage | | |
| L99VR035PTR | PWSSO12 | Tape and reel |

1 Block diagram and pin description

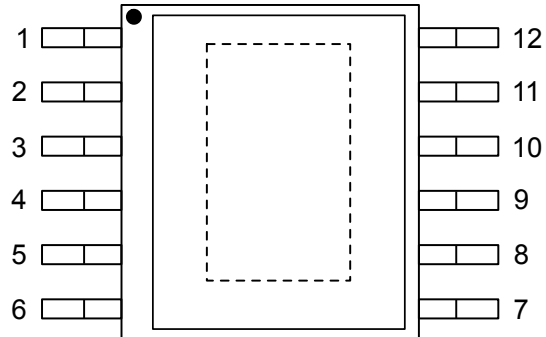
1.1 Block diagram

Figure 1. Functional block diagram



Prerelease product(s)

1.2 Pin description

Figure 2. Pin connection (top view)

Table 1. Pin function

| # | Name | Function |
|-----|----------------|--|
| 1 | V _S | LDO supply voltage |
| 2 | DNC | Do not connect, leave the pin floating |
| 3 | V _O | LDO output voltage |
| 4 | GND | Ground reference |
| 5 | DNC | Do not connect, leave the pin floating |
| 6 | DNC | Do not connect, leave the pin floating |
| 7 | DNC | Do not connect, leave the pin floating |
| 8 | DNC | Do not connect, leave the pin floating |
| 9 | DNC | Do not connect, leave the pin floating |
| 10 | DNC | Do not connect, leave the pin floating |
| 11 | DNC | Do not connect, leave the pin floating |
| 12 | EN | Enable input set V _{EN} : High = Turn on the device Low = Turn off the device EN pin cannot be leaved floating |
| TAB | TAB | Connected to the ground |

2 Electrical specifications

2.1 Absolute maximum ratings

Stressing the device above the rating listed in the Table 2 may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute maximum ratings

| Symbol | Parameter | Value | Unit |
|----------|---|--------------------|------|
| V_S | DC supply voltage | -0.3 to 28 | V |
| V_S | Single pulse/ $t_{max} < 400$ ms “transient load dump” | 40 | V |
| V_O | DC output voltage | -0.3 to 7 | V |
| I_O | DC output current | Internally limited | - |
| V_{EN} | Enable input | -0.3 to 28 | V |
| VESD HBM | V_S pin vs GND, ESD HBM voltage level | ± 4 | kV |
| | ESD HBM voltage level (HBM-MIL STD 883C) | ± 2 | kV |
| VESD CDM | ESD CDM voltage level (CDM AEC-Q100-011) | ± 500 | V |
| | ESD CDM voltage level on corner pins (CDM AEC-Q100-011) | ± 750 | V |

2.2 Thermal data

2.2.1 Thermal resistance

Table 3. Operation junction temperature

| Symbol | Parameter | Value | Unit | Item |
|---------------|--|------------------------|------|-------|
| $R_{thj-amb}$ | Junction to ambient thermal resistance | 28.4 ⁽¹⁾⁽²⁾ | °C/W | A.002 |

1. $R_{thj-amb}$ based on a 4-layer JEDEC PCB (2S2P) test board with thermal vias (see the Figure 20).

2. Measurements were performed according to JEDEC 51.2 in still air.

2.2.2 Thermal protection

Table 4. Temperature threshold

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit | Item |
|------------------|--------------------------------|----------------|------|------|------|------|-------|
| $T_{prot}^{(1)}$ | Thermal protection temperature | | - | 190 | - | °C | A.003 |
| T_{prot_hyst} | Thermal protection hysteresis | | - | 5 | - | °C | A.004 |
| T_J | Operating junction temperature | T_J | -40 | - | 175 | °C | A.005 |
| T_{stg} | Storage temperature | T_{stg} | - | - | 150 | °C | A.006 |

1. Thermal protection is guaranteed by design and characterization.

2.3 Electrical characteristics

Values specified in this section are for $V_S = 4.5\text{ V to }28\text{ V}$, $T_J = -40\text{ °C to }+150\text{ °C}$, unless otherwise stated.

Table 5. General characteristics

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit | Pin | Item |
|------------------|---|---|-------|------|-------|---------------|-----------------|-------|
| V_{O_3V3} | Output voltage 3.3 V | $V_S = 4.5\text{ to }28\text{ V}$ $I_O = 0\text{ mA to }300\text{ mA}$ | 3.234 | 3.3 | 3.366 | V | V_O | A.007 |
| V_{O_5V} | Output voltage 5 V | $V_S = 6\text{ to }28\text{ V}$ $I_O = 0\text{ mA to }300\text{ mA}$ | 4.9 | 5 | 5.1 | V | V_O | A.007 |
| I_O | DC output current | $V_O = 3.3\text{ V, }V_O = 5\text{ V}$ | - | - | 300 | mA | V_O | A.008 |
| I_{short} | Short circuit current value | $V_O = 3.3\text{ V, }V_O = 5\text{ V}$ | 450 | - | 900 | mA | V_O | A.009 |
| $\Delta V_O/V_O$ | Static line regulation | V_S is from 4.5 V for $V_O = 3.3\text{ V}$ or 6 V for $V_O = 5\text{ V to }40\text{ V}$ $I_O = 150\text{ mA}$ | - | - | 10 | mV | $V_S,$ V_O | A.010 |
| $\Delta V_O/V_O$ | Static load regulation | $I_O = 1\text{ mA to }300\text{ mA, }V_S = 14\text{ V}$ $V_O = 3.3\text{ V, }V_O = 5\text{ V}$ | - | - | 10 | mV | V_O | A.011 |
| V_{dp} | Drop voltage | $I_O = 300\text{ mA}$ $V_O = 5\text{ V, }V_O = 3.3\text{ V}$ | - | 0.55 | 1 | V | $V_S,$ V_O | A.012 |
| PSRR | Power supply rejection ratio ⁽¹⁾ | $V_S = 13.5\text{ V, }I_O = 300\text{ mA,}$ frequency = 1 kHz, $V_O = 3.3\text{ V}$ $V_O = 5\text{ V, }C_O = 2.2\text{ }\mu\text{F}$ | - | 76 | - | dB | $V_S,$ V_O | A.013 |
| I_{qn} | Current consumption with regulator disabled $I_{qn} = I_S - I_O$ | $V_S = 4.5\text{ to }28\text{ V}$ for $V_O = 3.3\text{ V}$ $V_S = 6\text{ to }28\text{ V}$ for $V_O = 5\text{ V}$ EN = low | - | - | 800 | nA | $V_S,$ V_O | A.014 |
| I_{qn_LL} | Current consumption with regulator disabled $I_{qn_LL} = I_S - I_O$ | $V_S = 4.5\text{ to }28\text{ V}$ for $V_O = 3.3\text{ V}$ $V_S = 6\text{ to }28\text{ V}$ for $V_O = 5\text{ V}$ $I_O = 0\text{ mA, EN} = \text{high}$ | - | - | 3.5 | μA | $V_S,$ V_O | A.023 |
| I_{qn_O} | Current consumption with regulator enabled $I_{qn_O} = I_S - I_O$ | $V_S = 4.5\text{ to }28\text{ V}$ for $V_O = 3.3\text{ V}$ $V_S = 6\text{ to }28\text{ V}$ for $V_O = 5\text{ V}$ $I_O = 1\text{ mA, EN} = \text{high}$ | - | 23 | 30 | μA | $V_S,$ V_O | A.015 |
| I_{qn_50} | Current consumption with regulator enabled $I_{qn_50} = I_S - I_O$ | $V_S = 4.5\text{ to }28\text{ V}$ for $V_O = 3.3\text{ V}$ $V_S = 6\text{ to }28\text{ V}$ for $V_O = 5\text{ V}$ $I_O = 50\text{ mA, EN} = \text{high}$ | - | 40 | 50 | μA | $V_S,$ V_O | A.016 |
| I_{qn_150} | Current consumption with regulator enabled $I_{qn_150} = I_S - I_O$ | $V_S = 4.5\text{ to }28\text{ V}$ for $V_O = 3.3\text{ V}$ $V_S = 6\text{ to }28\text{ V}$ for $V_O = 5\text{ V}$ $I_O = 150\text{ mA, EN} = \text{high}$ | - | 140 | 160 | μA | $V_S,$ V_O | A.017 |
| I_{qn_300} | Current consumption with regulator enabled $I_{qn_300} = I_S - I_O$ | $V_S = 4.5\text{ to }28\text{ V}$ for $V_O = 3.3\text{ V}$ $V_S = 6\text{ to }28\text{ V}$ for $V_O = 5\text{ V}$ $I_O = 300\text{ mA, EN} = \text{high}$ | - | 175 | 200 | μA | $V_S,$ V_O | A.018 |

1. Guaranteed by design - not tested.

Table 6. Enable characteristics

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit | Pin | Item |
|---------------------|-----------------------|----------------|------|------|------|------|-----|-------|
| V _{En_low} | EN input low voltage | | - | - | 0.7 | V | EN | A.019 |
| V _{En_hig} | EN input high voltage | | 2 | - | - | V | EN | A.020 |

Table 7. UVLO characteristics

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit | Pin | Item |
|------------------------|---|---------------------|------|------|------|------|----------------|-------|
| V _{s UVLO} | Ramp V _S down until the output turns OFF | EN = V _S | - | - | 2.5 | V | V _S | A.021 |
| V _{UVLO_hyst} | | EN = V _S | 60 | - | 500 | mV | V _S | A.022 |

Note: *All parameters are guaranteed in the junction temperature range -40 °C to 150 °C (unless otherwise specified); the L99VR03 device is still operative and functional at higher temperatures (up to 175 °C). Parameters limit at higher junction temperature than 150 °C may change respect to what is specified as per the standard temperature range. Device functionality at high junction temperature is guaranteed by characterization.*

All parameters are guaranteed by design for V_O not reported in test condition.

Minimum input voltage values are achievable adopting an input ceramic capacitor: C5750X7R2A475M230KA - ceramic capacitor multistrata SMD, 4.7 μF, 100 V, ±20%, X7R, C series.

Prerelease product(s)

2.4 Electrical characteristics curves

Figure 3. Output voltage vs T_J

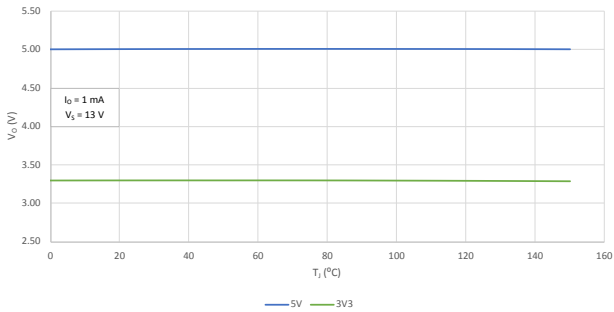


Figure 4. Output voltage vs V_S

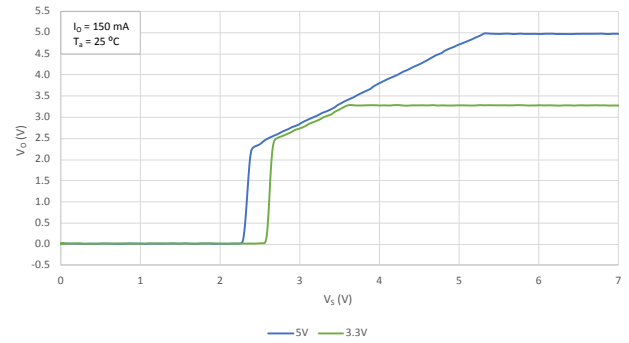


Figure 5. Drop voltage vs output current

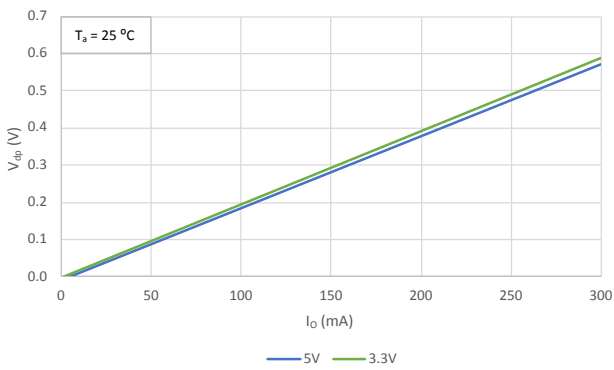


Figure 6. Current consumption vs output current

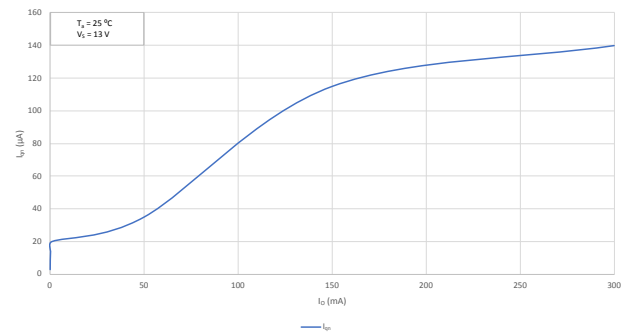


Figure 7. Current consumption vs input voltage ($I_O < 1$ mA)

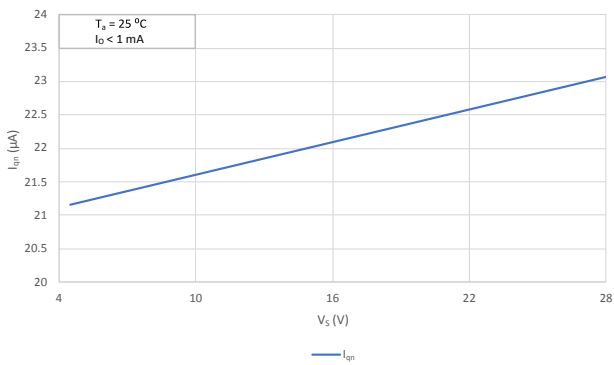
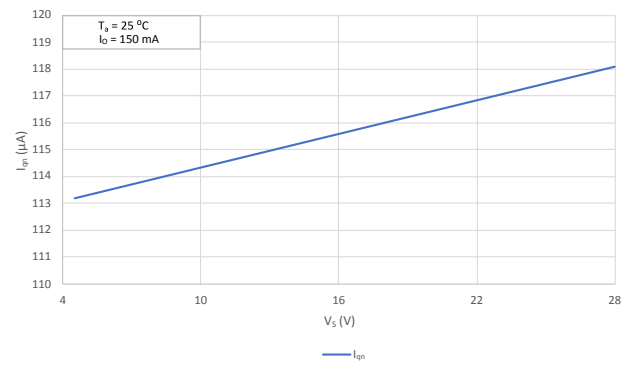


Figure 8. Current consumption vs input voltage ($I_O = 250$ mA)



Prerelease product(s)

Figure 9. Current consumption vs input voltage ($I_O = 300\text{ mA}$)

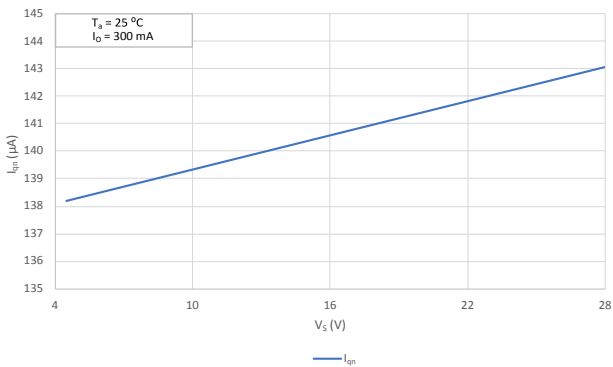


Figure 10. PSRR

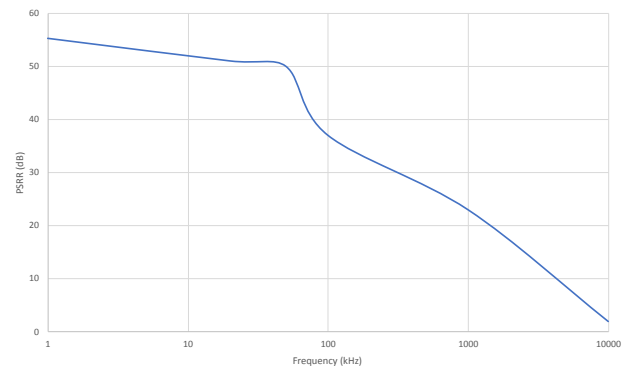


Figure 11. Output voltage vs enable voltage ($V_O = 3.3\text{ V}$)

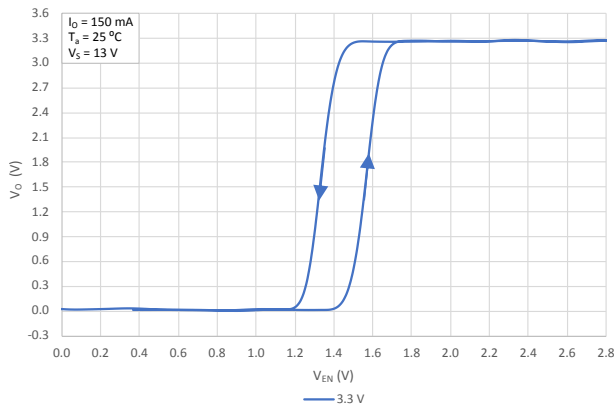


Figure 12. Output voltage vs enable voltage ($V_O = 5\text{ V}$)

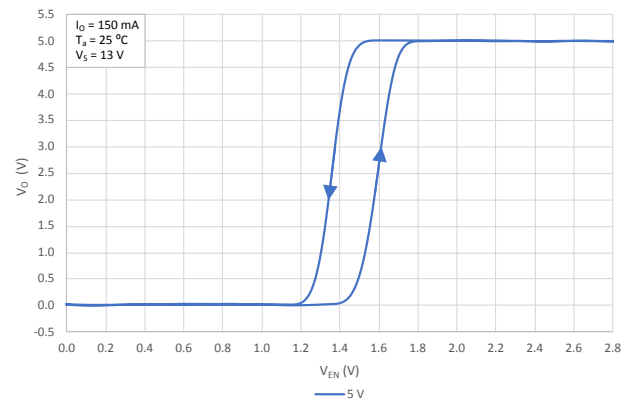


Figure 13. V_{EN_high} vs T_J

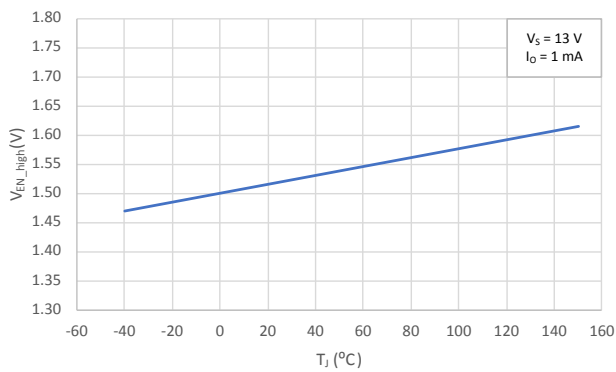
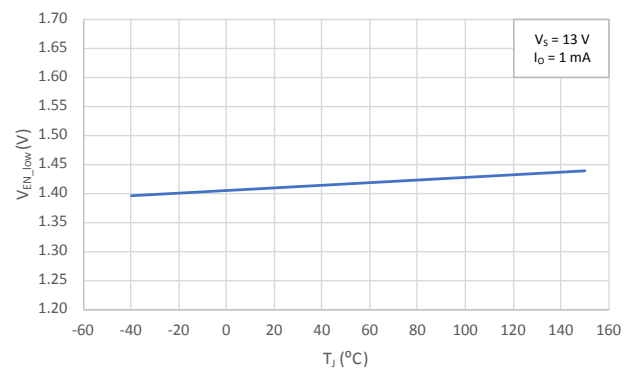


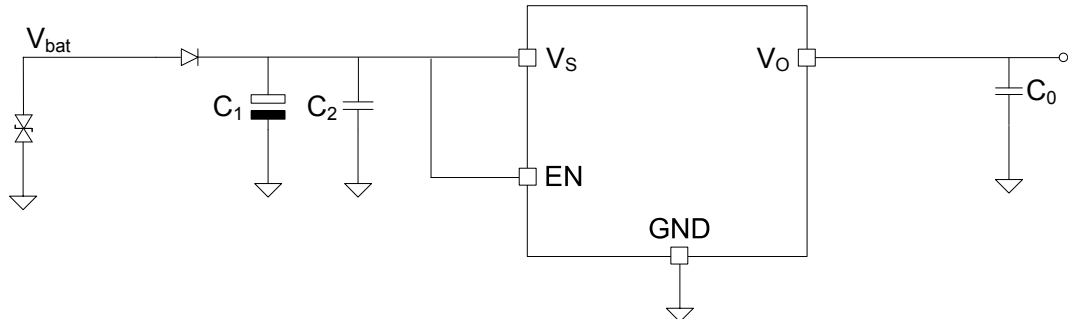
Figure 14. V_{EN_low} vs T_J



Prerelease product(s)

3 Application information

Figure 15. Application schematic



Input ceramic capacitor $C_2 \geq 1 \mu\text{F}$ is necessary for the regulator to operate properly.

The other input capacitor C_1 can be used as a backup supply for the application. The C_0 capacitor, connected to the output pin, is for bypassing to GND the high-frequency noise and it guarantees stability even during sudden line and load variations.

Tiny output capacitors reduce board space and BOM cost: stable operation with $2.2 \mu\text{F}$ capacitor min, $4.7 \mu\text{F}$ recommended to improve load transient response. $\text{ESR} \leq 10 \text{ m}\Omega$.

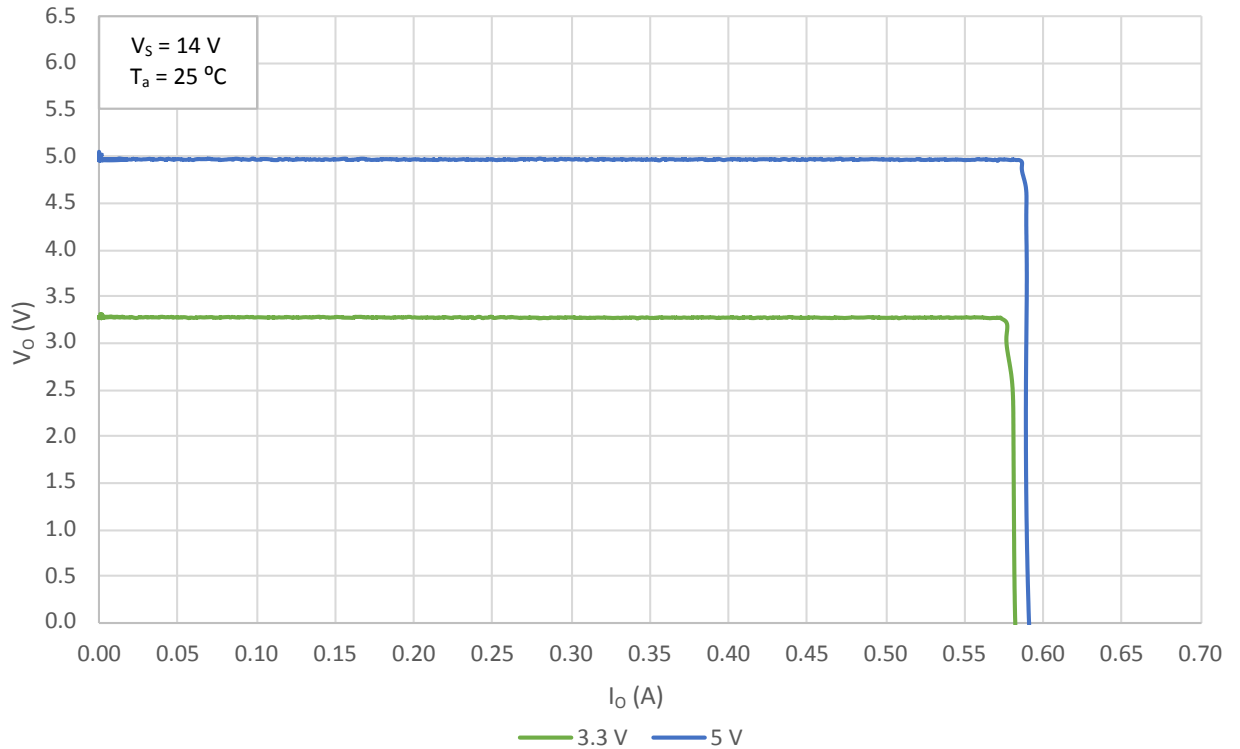
3.1 Voltage regulator

The voltage regulator uses a p-channel MOS transistor as a regulating element. With this structure, a very low dropout voltage at current up to $I_O = 300 \text{ mA}$ is obtained. The high-precision of the output voltage ($\pm 2\%$) is obtained with a pretrimmed reference voltage. The voltage regulator automatically adapts its own quiescent current to the output current level. In light load conditions, the quiescent current goes down to $I_{Q_LL} = 3.5 \mu\text{A}$. L99VR03 operates with reduced input voltage (post regulation) minimizing the internal power dissipation and maximizing the output current. During initial power-up, after a thermal shutdown and a short to ground event, the regulator has a soft start incorporated to control initial current through the pass element and the output capacitor.

3.2 Output current limitation

Output current limitation is present to protect the regulator and the application from overload condition, such as short to ground.

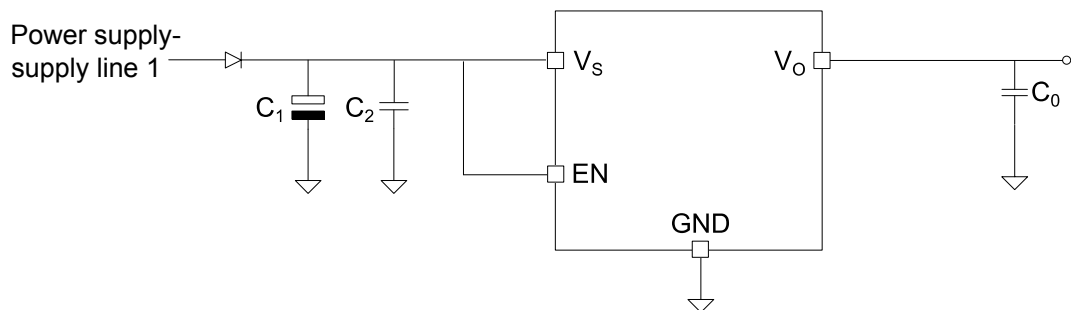
Figure 16. Behavior of output current versus regulated voltage V_O



3.3 Enable

The L99VR03 is enabled/disabled by the enable input. With the EN pin above V_{En_high} and the input voltage above V_{S_UVLO} , the device becomes active with a stable regulated output voltage. With the EN pin below V_{En_low} the device is disabled, reducing the quiescent current as low as 800 nA. The embedded hysteresis (V_{En_hyst}) avoids an undefined state of the device in case of slow ramp up signals applied to the EN input. It may happen that the enable pin must be driven by components supplied at a voltage different from the regulator supply voltage. In this case the EN input pin must be set high only once $V_S > 1.5\text{ V}$. A solution to drive the enable pin is depicted in the Figure 17.

Figure 17. Typical example of enable control

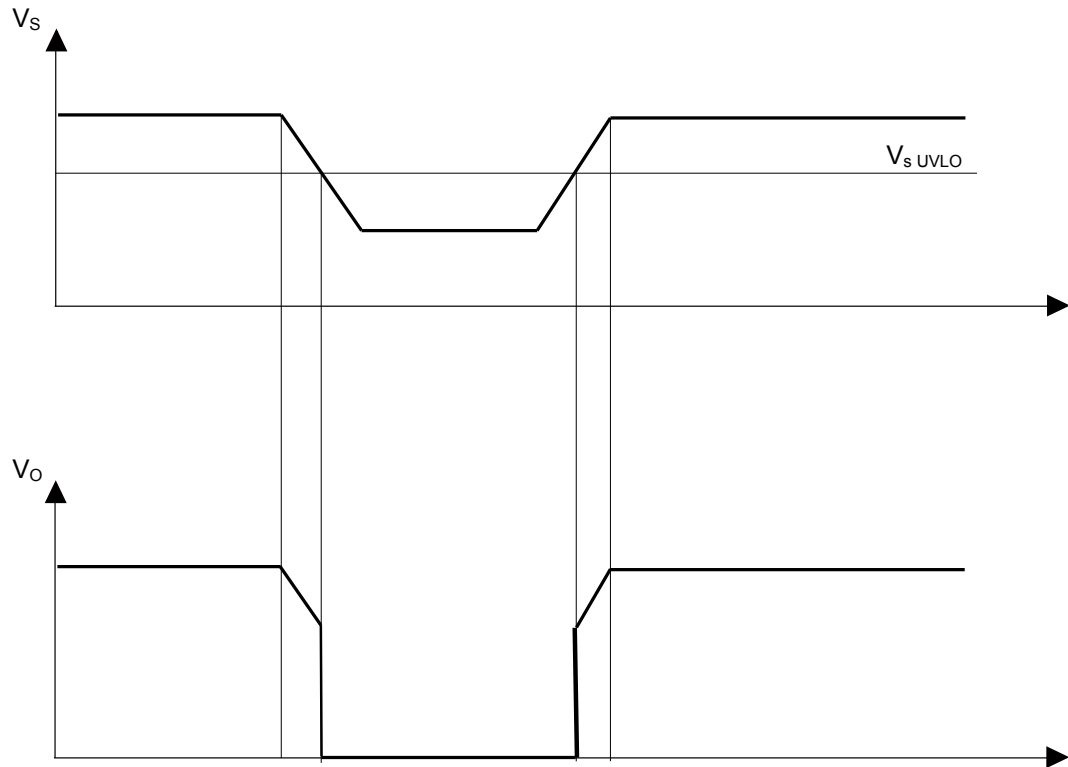


In any case, since the enable input voltage is linked to the maximum DC supply voltage (V_S) applied to the L99VR03 (-0.3 V to 28 V), special care must be adopted in driving the EN pin to avoid exceeding the absolute maximum rating.

3.4 Undervoltage lockout UVLO

The undervoltage lockout (UVLO) circuit allows to turn off the regulator element if the input voltage drops below the internal threshold, $V_{s\text{ UVLO}}$, avoiding undesired unknown output state during low input voltage. When the input voltage is above the $V_{s\text{ UVLO}}$ threshold, the regulating element is again turned on. If the input voltage has a negative transient which drops below the UVLO threshold and recovers, the regulator turns off and powers up with a normal power-up sequence once the input voltage is above the required levels.

Figure 18. Undervoltage lock out on output voltage

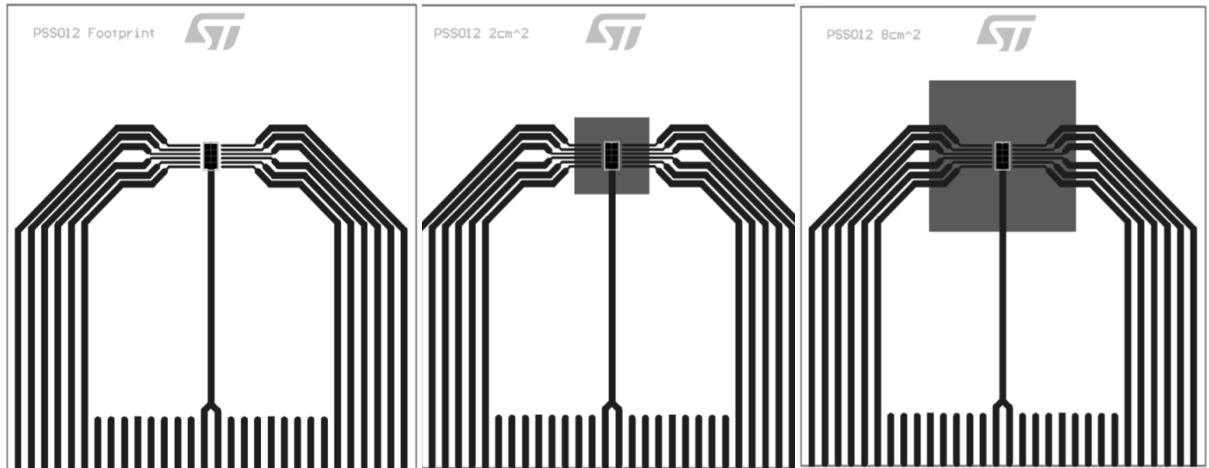


Prerelease product(s)

4 Package and PCB thermal data

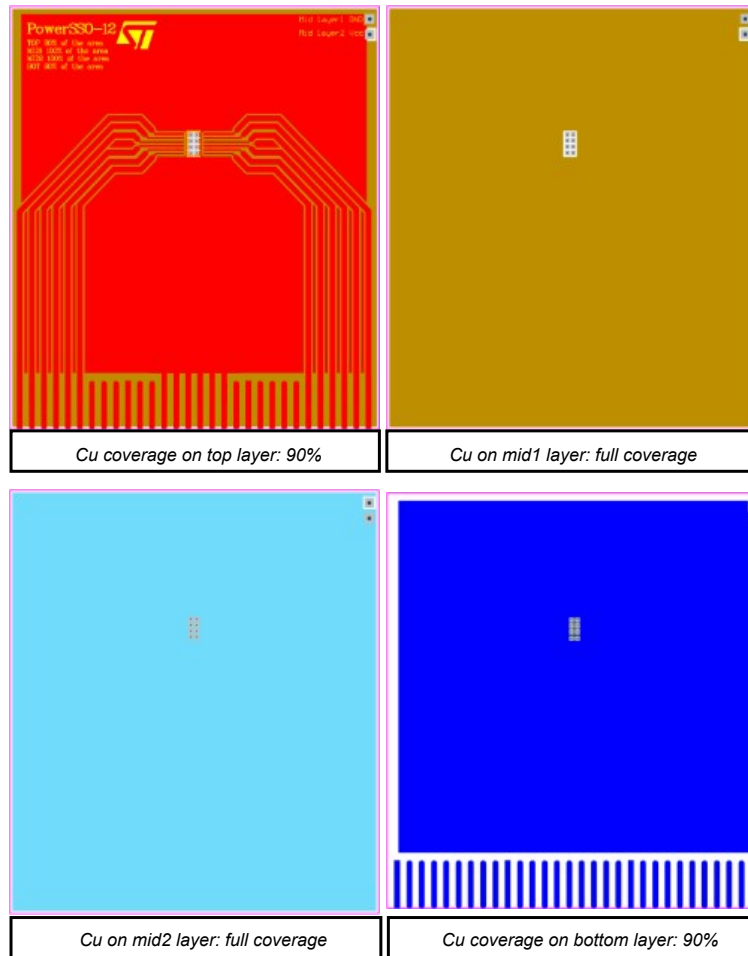
4.1 Thermal data

Figure 19. PCB 2 layers



- Board finish thickness 1.6 mm \pm 10%
- Board four layers
- Board dimension 77 x 86 mm
- Board Material FR4
- Cu thickness 0.070 mm (outer layers)
- Cu thickness 0.035 mm (inner layers)
- Thermal vias separation 1.2 mm
- Thermal via diameter 0.3 mm \pm 0.08 mm
- Cu thickness on vias 0.025 mm
- Footprint dimension 2.2 x 3.9 mm

Figure 20. PCB 4 layers



- Board finish thickness 1.6 mm $\pm 10\%$
- Board four layers
- Board dimension 77 x 86 mm
- Board Material FR4
- Cu thickness 0.070 mm (outer layers)
- Cu thickness 0.035 mm (inner layers)
- Thermal vias separation 1.2 mm
- Thermal via diameter 0.3 mm ± 0.08 mm
- Cu thickness on vias 0.025 mm
- Footprint dimension 2.2 x 3.9 mm

Prerelease product(s)

Figure 21. $R_{thj-amb}$ vs PCB copper area in still air condition

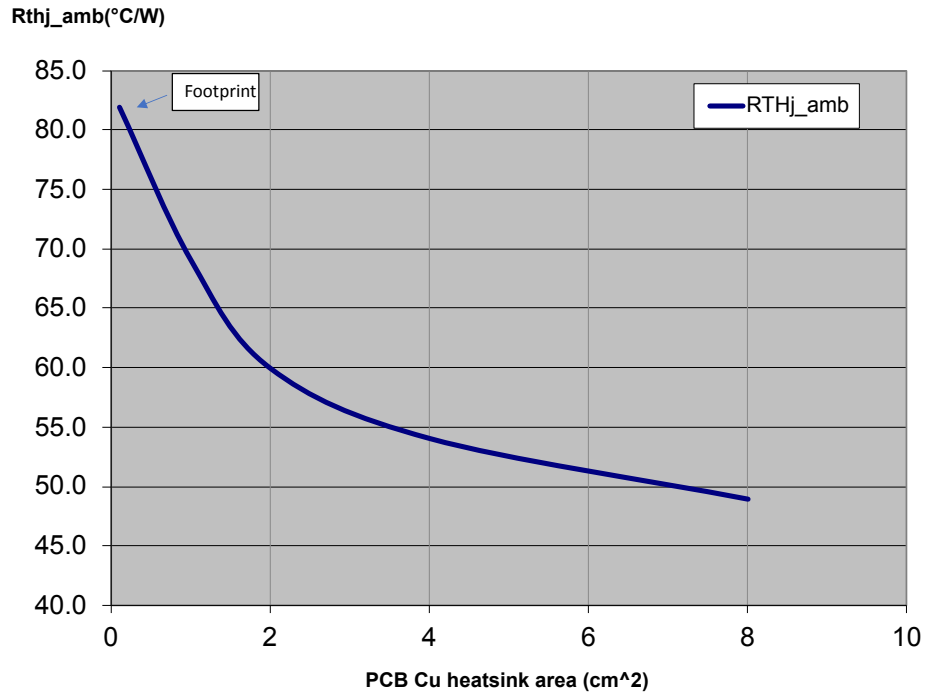
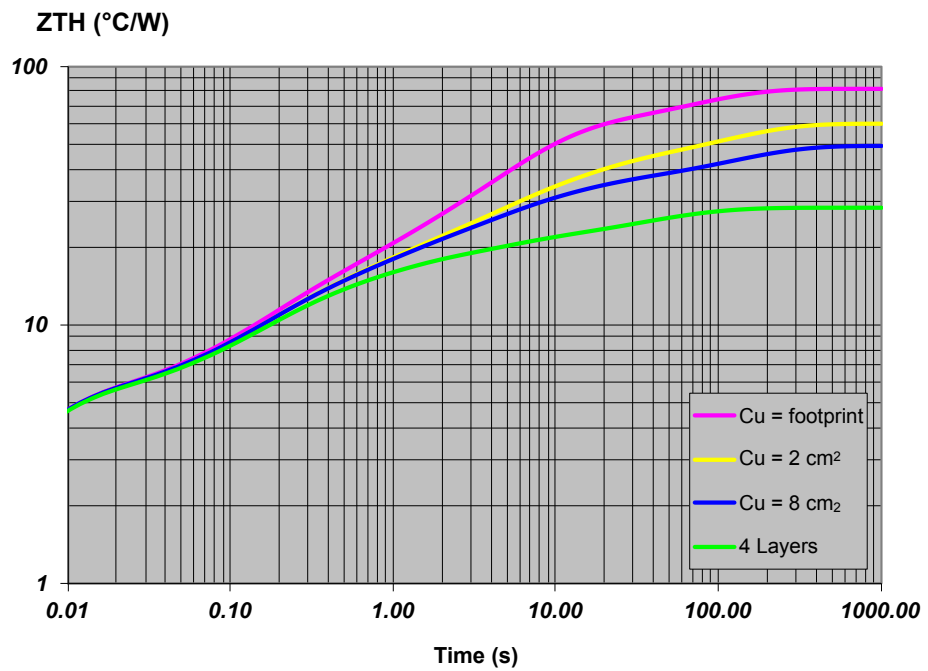


Figure 22. Thermal impedance curves junction to ambient



Pulse calculation formula:

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta) \tag{1}$$

Where: $\delta = tp/T$

Prerelease product(s)

Figure 23. Thermal fitting model of a V_{reg}

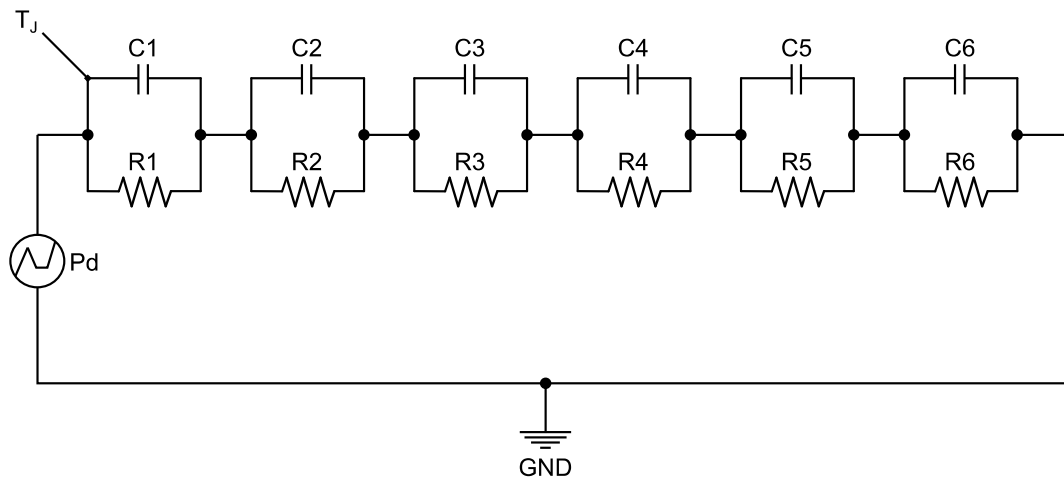


Table 8. Thermal parameter

| Thermal parameters | 2 layer PCB | | | 4L |
|---|-------------|------|------|-----|
| | FP | 2 CM | 8 CM | |
| R1 ($^{\circ}\text{C}/\text{W}$) | 4.9 | - | - | - |
| R2 ($^{\circ}\text{C}/\text{W}$) | 5 | - | - | - |
| R3 ($^{\circ}\text{C}/\text{W}$) | 6 | - | - | - |
| R4 ($^{\circ}\text{C}/\text{W}$) | 18 | 9 | 8 | 4.5 |
| R5 ($^{\circ}\text{C}/\text{W}$) | 22 | 15 | 10 | 4 |
| R6 ($^{\circ}\text{C}/\text{W}$) | 26 | 20 | 15 | 4 |
| C1 ($\text{W}\cdot\text{s}/^{\circ}\text{C}$) | 0.001 | - | - | - |
| C2 ($\text{W}\cdot\text{s}/^{\circ}\text{C}$) | 0.03 | - | - | - |
| C3 ($\text{W}\cdot\text{s}/^{\circ}\text{C}$) | 0.1 | - | - | - |
| C4 ($\text{W}\cdot\text{s}/^{\circ}\text{C}$) | 0.4 | 0.4 | 0.4 | 0.8 |
| C5 ($\text{W}\cdot\text{s}/^{\circ}\text{C}$) | 0.27 | 0.8 | 1 | 7 |
| C6 ($\text{W}\cdot\text{s}/^{\circ}\text{C}$) | 3 | 6 | 9 | 15 |

Prerelease product(s)

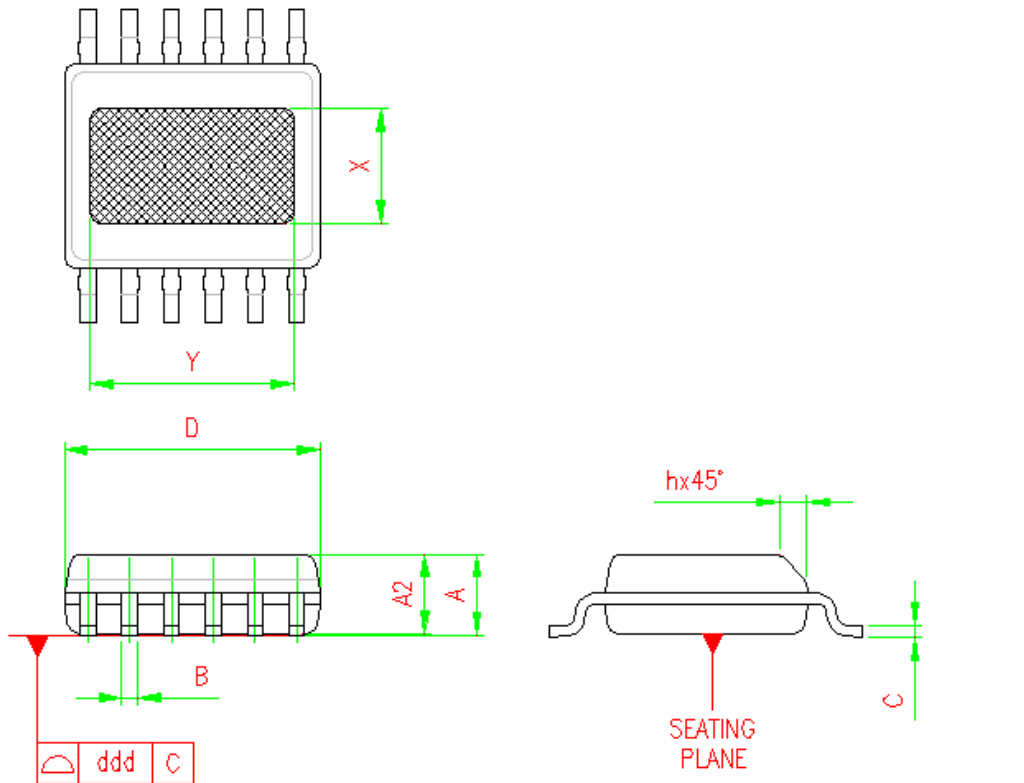
5 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

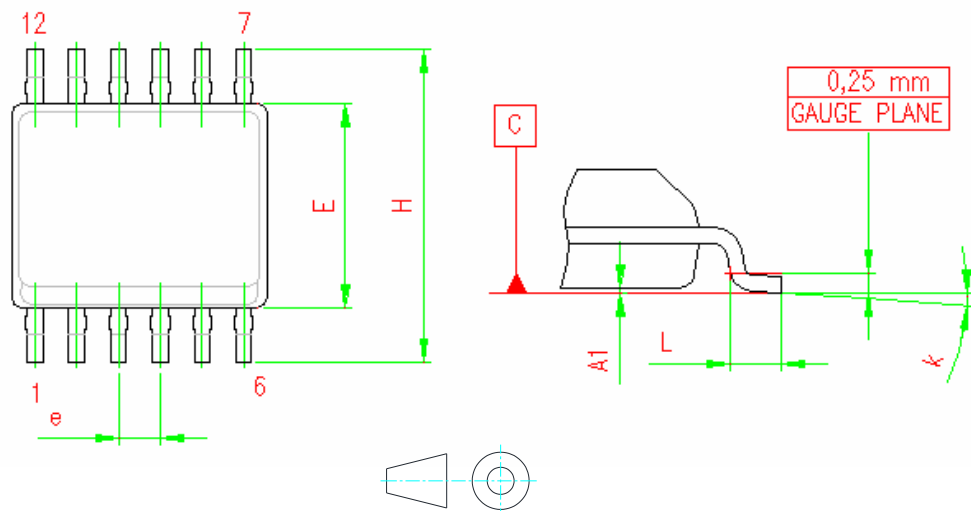
5.1 PWSSO12 (4.9x3.9x1.5 mm exposed pad down) package information

Figure 24. PWSSO12 (4.9x3.9x1.5 mm exposed pad down) package outline

BOTTOM VIEW



TOP VIEW



Prerelease product(s)

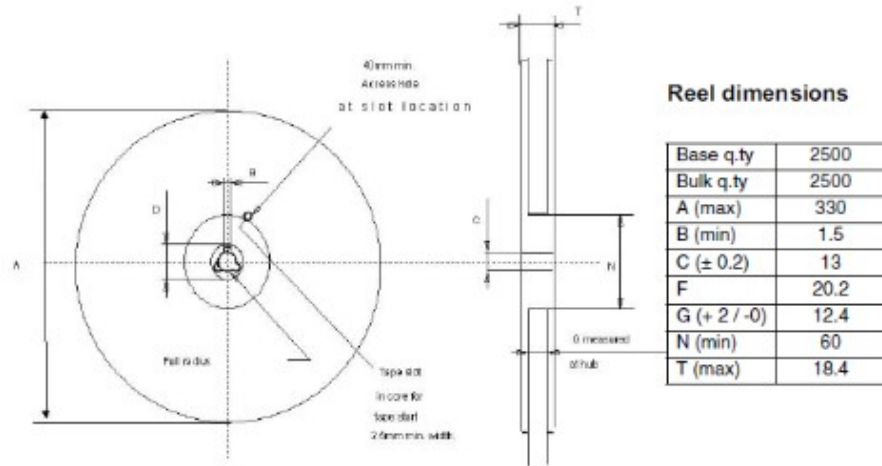
Table 9. PWSSO12 (4.9x3.9x1.5 mm exposed pad down) package mechanical data

| Symbol | Dimensions in mm | | |
|--------|------------------|------|------|
| | Min. | Typ. | Max. |
| A | 1.25 | - | 1.70 |
| A1 | 0.00 | - | 0.10 |
| A2 | 1.10 | - | 1.60 |
| B | 0.2 | - | 0.41 |
| C | 0.190 | - | 0.25 |
| D | 4.80 | - | 5.00 |
| E | 3.80 | - | 4.00 |
| e | - | 0.80 | - |
| H | 5.80 | - | 6.20 |
| h | 0.25 | - | 0.50 |
| L | 0.40 | - | 1.27 |
| k | 0d | - | 8d |
| X | 2.20 | - | 2.80 |
| Y | 2.90 | - | 3.50 |
| ddd | - | - | 0.10 |

Prerelease product(s)

5.2 PWSSO12 packaging information

Figure 25. PWSSO12 tape and reel shipment

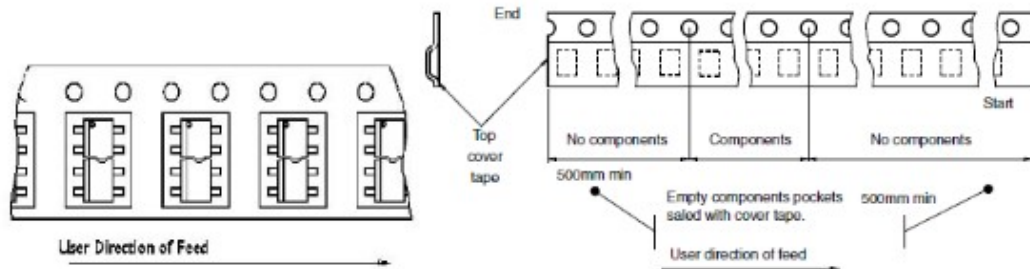
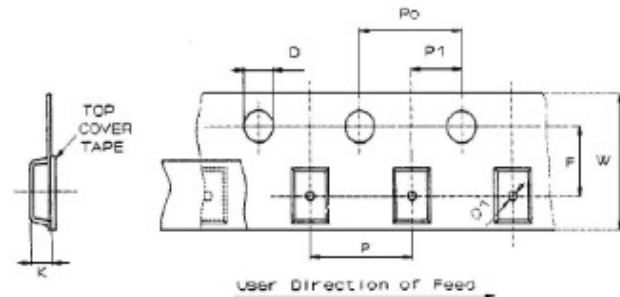


Tape dimensions

According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb. 1988

| | | |
|-------------------|------------|-----|
| Tape width | W | 12 |
| Tape hole spacing | P0 (± 0.1) | 4 |
| Component spacing | P | 8 |
| Hole diameter | D (± 0.05) | 1.5 |
| Hole diameter | D1 (min) | 1.5 |
| Hole position | F (± 0.1) | 5.5 |
| Compartment depth | K (max) | 4.5 |
| Hole spacing | P1 (± 0.1) | 2 |

All dimensions are in mm.



Revision history

Table 10. Document revision history

| Date | Version | Changes |
|-------------|---------|------------------|
| 04-Dec-2024 | 1 | Initial release. |

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