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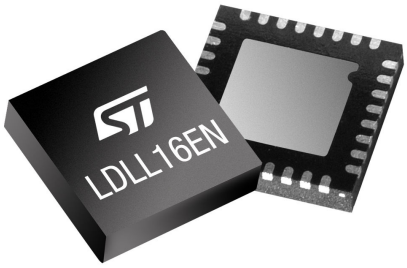
LDLL16EN

Datasheet

16-channel LED driver with automotive CAN FD light interface



QFN32L 5x5

Product status link
LDLL16EN

Product summary	
Order code	LDLL16ENTR
Package	QFN32L 5x5
Packing	Tape and reel

Features

- AEC-Q100 qualified
- General
  - CAN FD light compatible serial interface, protocol handler - CAN FD light is standardized in ISO 11898-1:2024 annex A
  - RX/TX interface - for communication with external shared transceiver
  - High precision oscillator integrated - no external quartz required
  - QFN32L 5x5 with wettable flanks and exposed pad
  - Timeout watchdog with fail-safe operation
  - Low standby current
  - Standalone and bus mode operation
  - 1 direct drive input - for two function groups supporting ASIL requirements
  - Multifunction capability - up to two different lighting functions in one IC
  - Widest configurability by embedded non-volatile and volatile memories
  - Battery supply voltage range from 5 V to 40 V
- Linear regulators
  - Operating temperature range from -40 °C to 150 °C
  - 16 constant current output channels - low-side configuration
  - Output current from 6.3 mA to 100 mA - parallelable outputs
  - Output voltage up to 20 V
  - Current setting per channel by 8-bit DAC
  - Analogue dimming, 8-bit PWM channel individual exponential brightness control and 8-bit global PWM dimming
  - Programmable PWM frequency
  - Optimized turn on/off time, gradual outputs delay and dithered clock - for better EMC performances
- Protection and diagnostic
  - Integrated 8-bit ADC - for full and flexible diagnostic
  - 1 dedicated line for fault bus
  - Temperature warning (one threshold)
  - Overtemperature shutdown
  - Short circuit and open-load detection and protection
  - Automatic LED current derating - through external NTC measurement and device junction temperature (T_J)

Application

- Automotive rear lighting
- Automotive ambient lighting
- Automotive exterior and interior light expansions (logo, grill, symbols, courtesy light…)

Description

The LDLL16EN is a monolithic 16-channel LED driver designed for automotive exterior and interior LED lighting applications. It guarantees up to 20 V output driving capability, allowing users to connect several LEDs in series, and features 16 regulated current sinkers able to provide from 6.3 mA to 100 mA programmable current to drive LEDs.

The LDLL16EN integrates a robust purely automotive CAN FD light compatible serial communication interface which allows a high rate data transmission (up to 1 Mbit/s) and uses CAN FD structure for long frames.

The device integrates a protocol handler, so no additional external components are needed to facilitate communication with the commander ECU, and a RX/TX interface for communication with external transceiver sharable among several devices (up to 6).

The LDLL16EN can operate in bus mode using CAN FD light compatible interface or in stand-alone/fail-safe mode using internal few time programmable (FTP) memory registers.

1 Introduction

The LDLL16EN is a monolithic 16-channel LED Driver designed for automotive exterior and interior LED lighting applications. It guarantees up to 20 V output driving capability, allowing users to connect several LEDs in series, and features 16 regulated current sinkers able to provide from 6.3 mA to 100 mA programmable current to drive LEDs.

The LEDs brightness can be adjusted separately through an 8-bit PWM exponential dimming control.

The LDLL16EN integrates a robust purely automotive CAN FD light compatible serial communication interface, which allows a high rate data transmission (up to 1 Mbit/s) and uses the CAN FD structure for long frames. The device integrates a protocol handler, so no additional external devices are needed to facilitate communication with the commander ECU, and a RX/TX interface for communication with an external transceiver sharable among several devices (up to 6). The LDLL16EN can operate in bus mode using the CAN FD light compatible interface or in stand-alone/fail-safe mode using internal few time programmable (FTP) memory registers.

Thanks to its programmability through the CAN FD light compatible communication interface, the device supports generic platform approaches, which require a software configurability of several parameters.

This differential robust interface offers a detailed diagnostic of the device itself, as well as of the controlled LED strings, and makes the device suitable for high data rate transmission, up to 1 Mbit/s.

As the device potentially controls safety critical functions, such as brake, built-in features are integrated in order to support a high level of functional safety at application level: a programmable timeout watchdog, a monitoring of the watchdog counter, a fail-safe state (limp-home function) and one direct input.

The device supports control of up to two individual lighting functions, each channel can be mapped flexible to the direct input or not, and features also one V_{PREG} pin, to supply the current sinkers through an external preregulator.

Thanks to integrated high precision oscillators, the device autonomously generates all relevant timing functions such as PWM frequency, duty cycle, trigger points for ADC conversion, phase shift, etc. No external timers are required.

In the LDLL16EN, thanks to the integration of an 8-bit ADC, a complete diagnostic is also available: open-load, output channel short to external preregulator, output channel LED (single or multiple) short detection, LED current derating in case of device temperature increasing.

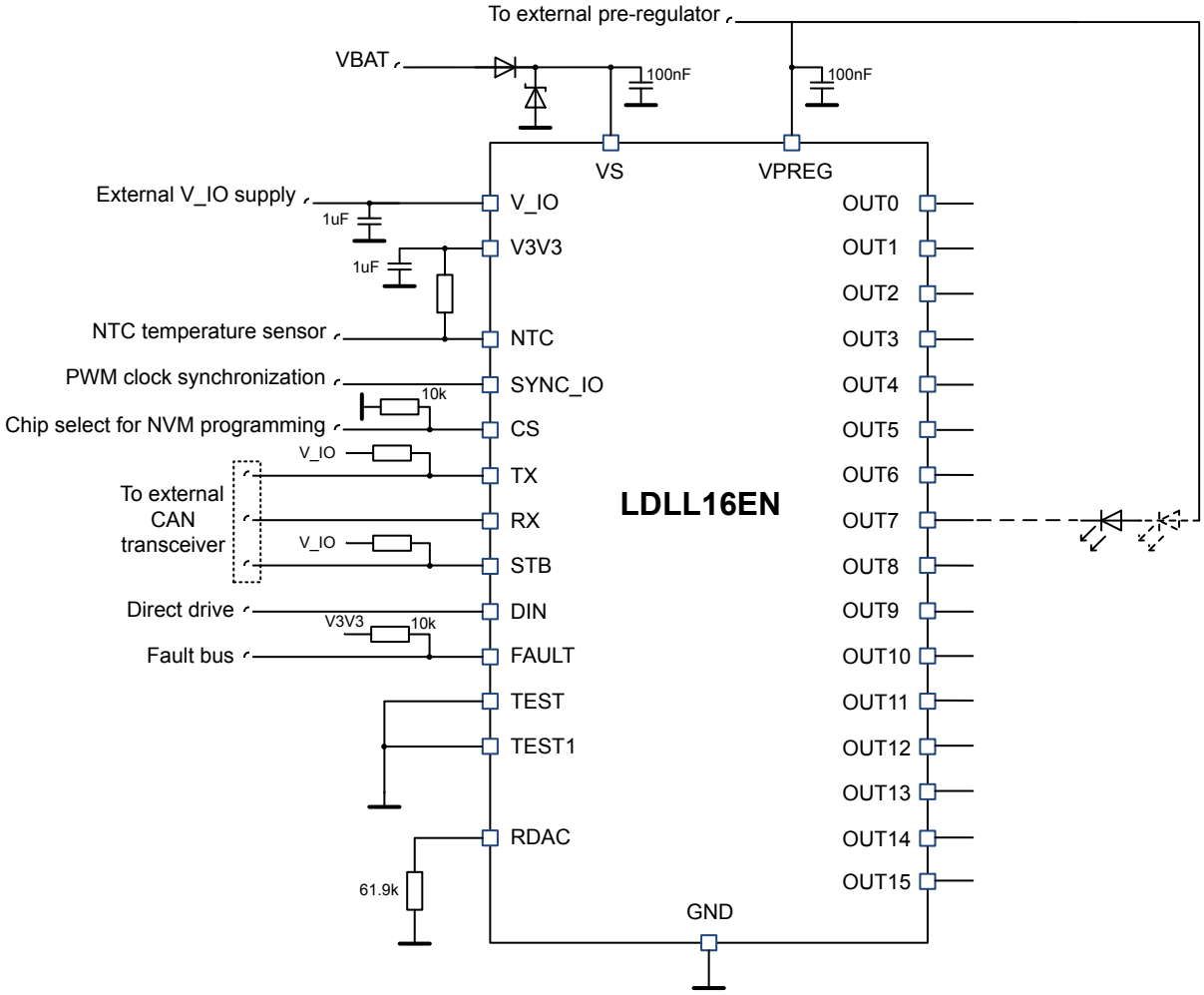
Diagnostic thresholds are freely configurable for each function group. Moreover, the user can configure the desired device reaction to detected faults, ensuring maximum flexibility for the application and sophisticated auto-recovery strategies.

The device features also the output gradual delay, which avoids the contemporary turning on of all the channels used for a specific light function, reducing the inrush current. To further improve EMI performances, the device implements an internal clock dithering to have a spread spectrum noise reduction.

Thermal management is equipped with thermal warning (TW) and outputs thermal shutdown (TSD). The device performs an automatic thermal derating based on external NTC measurement as well on device junction temperature (T_J).

The supply voltage range is between V_{S_MIN} and 40 V avoiding any additional load dump protection on the power supply stage.

Figure 1. LDLL16EN - simplified application schematic



1.1 Device information

Figure 2. **Functional block diagram**

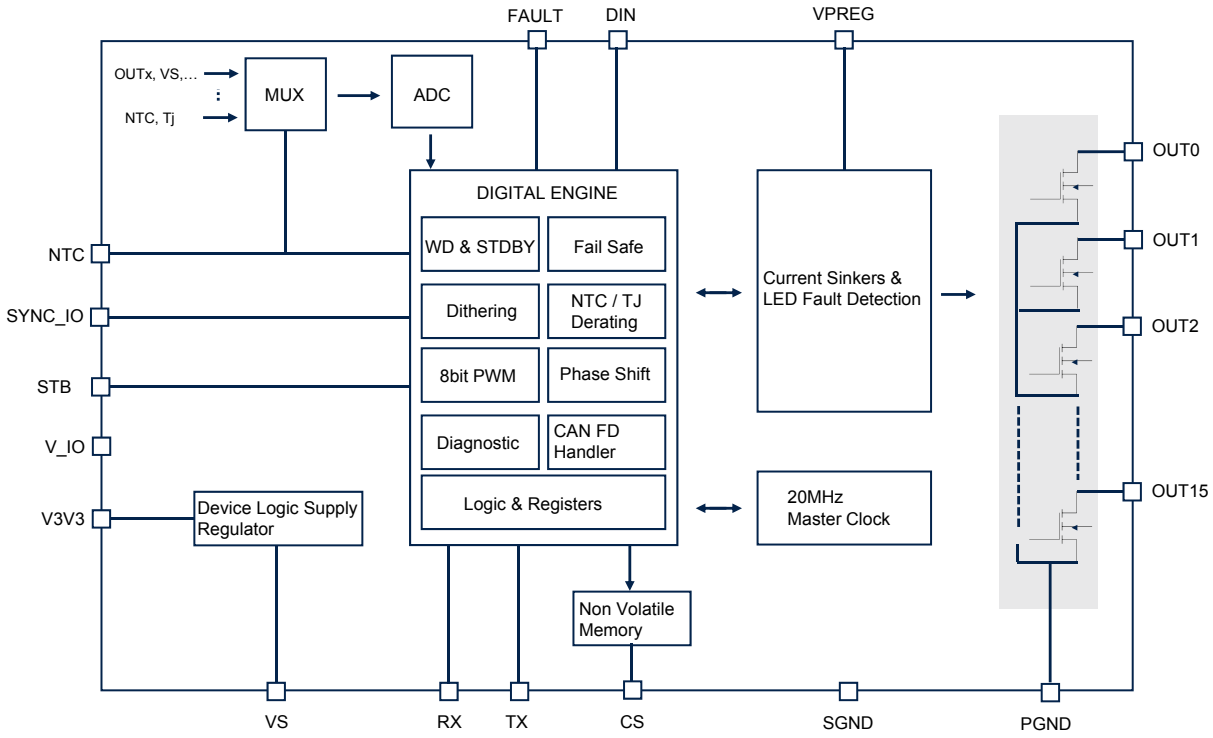


Figure 3. **Application diagram - example**

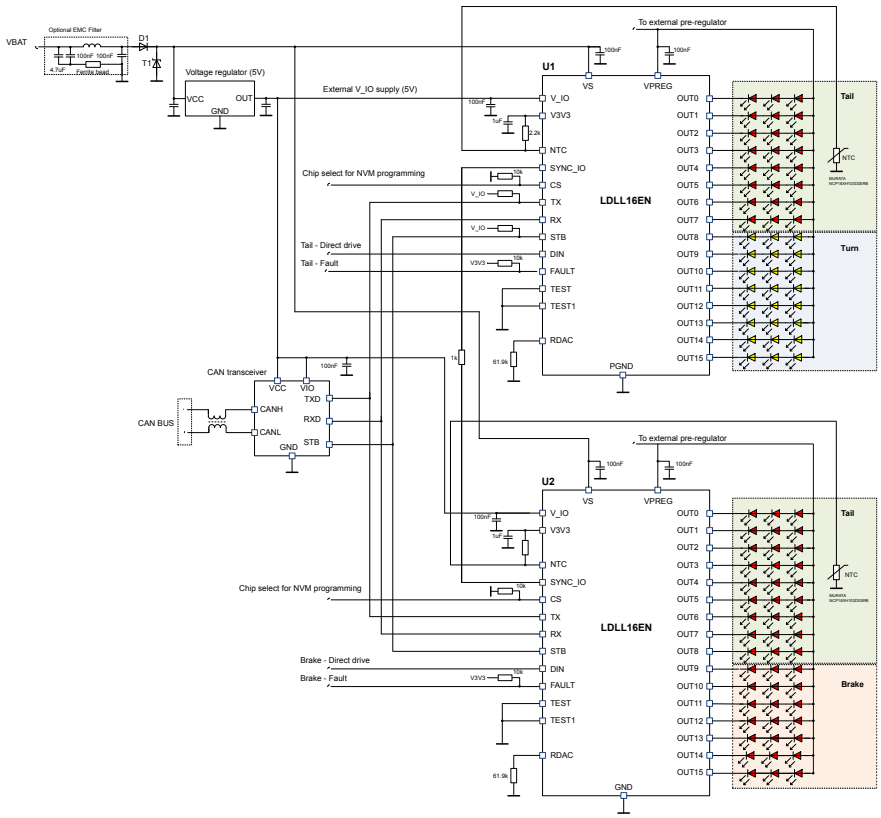


Figure 4. **QFN32L 5x5 connection diagram**

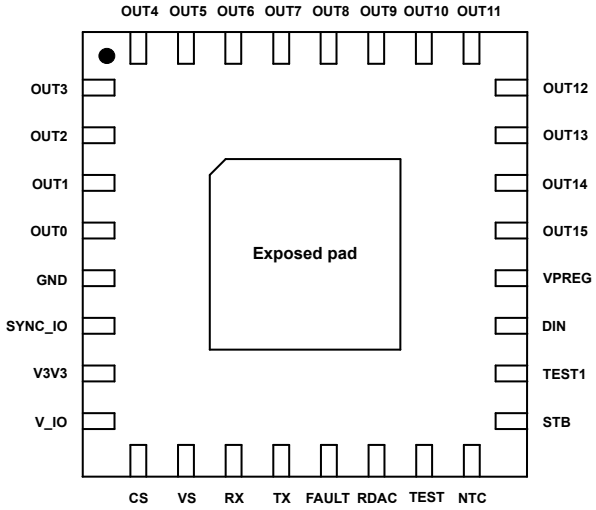


Table 1. **Pin list description**

Pin #	Name	Type I/O	Description
1-4, 21-24, 25-32	OUTx x = 0-15	O	Output pin, up to 16 channels – low-side configuration.
5	GND	I/O	Ground connection.
6	SYNC_IO	I/O	Synchronization input/output pin – for PWM synchronization among several devices. Left floating when not used. It is suggested to connect a shared 1kΩ resistor in series as protection when 2 or more devices are synchronized (therefore in the event that, by mistake, two or more devices are both configured as master).
7	V3V3	I/O	3.3 V regulator output voltage (logic and I/O). Connect a low ESR capacitor (1 µF) close to this pin.
8	V_IO	I/O	I/O pin receiving external CAN transceiver supply regulator's output voltage (to manage TX and STB pins).
9	CS	I	Chip select input – for entering test and programming mode.
10	VS	I	Input supply pin ofthe IC. Connect VS to the car battery voltage. Must be reverse protected (external diode). Input supply for the 3.3 V internal linear voltage regulator.
11	RX	I	Receive CAN FD light compatible data. Input.
12	TX	O	Transmit CAN FD light compatible data output. It is suggested to use 2 kΩ pull-up resistor.
13	FAULT	I/O	I/O pin for diagnostic (1 fault pin used for diagnostic)
14	RDAC	I	External resistor for DACs current reference It is suggested to use E96 series, 61.9 kΩ (1% tolerance standard thin film resistance, ±0.7%, 100 ppm/K, temperature spread in the range [-40÷100]°C).
15, 18	TESTx		Internal use only. To be connected to GND.
16	NTC	I	NTC pin for LEDs thermal control. Connect an external NTC resistor.
17	STB	O	CAN (external) transceiver standby mode control output. It is suggested to use 10 kΩ.
19	DIN	I	Direct input pin.
20	VPREG	I	1 pin for connection to external pre-regulator (to beconnected to the anode of LED strings).
NA	EP	NA	Exposed (thermal) pad-connected to PCB ground, for thermal dissipation.

2 Device supply concept

The LDLL16EN IC is supplied through VS pin, connected to the car battery through an external diode for reverse polarity protection.

The supply voltage is in the range of [V_{S_MIN} ÷ 40] V, avoiding any additional load dump protection on power supply stage. On top of that, no device reset will occur in the supply voltage range of [3 ÷ V_{S_MIN}] V, to keep digital content during cold cranking pulse.

In that range, [3 ÷ V_{S_MIN}] V, and till POR threshold ($V_{3V3\_POR\_L}$) is not reached, full device protection is granted and digital part (register content and state machine) is kept alive.

An under-voltage threshold (V_{S_UV}) is implemented to avoid wrong output current due to low battery and, till device leaves the voltage range between under-voltage V_{S_UV} and under-voltage reset $V_{S\_UV\_RST}$, some parameters may deviate versus specified value.

3 Linear current sinkers

3.1 General description

The LDLL16EN features 16 low-side linear current generators to regulate from 6.3 mA to 100 mA current on the output LED strings.

The output channels can be put in parallel to address all those light functions needing higher current than the programmable one.

In this device, the current can be individually programmed per channel by using an integrated 8-bit DAC. The output channels paralleling is allowed, provided that all these channels are controlled simultaneously.

Supplied directly from car battery, the LDLL16EN IC guarantees up to 20 V output driving capability, allowing users to connect several LEDs in series.

Each LED string can be supplied by battery or through one external pre-regulator connected between battery and LED string anodes.

The pre-regulated (V_{PREG}) and battery (V_S) voltages are internally monitored by an 8-bit ADC, the results are stored in a dedicated result register. The ADC is used also to monitor the device temperature (T_J) as well as all the output channels. These channels are refreshed once per PWM period in on-state. The minimum PWM on-time (vs PWM frequency), to ensure a correct channel ADC reading, is $t_{PWM\_ON\_OFF}$ time (see the Table 63). In any case, ADC will not perform any reading operation before a configurable blanking time ($t_{DIAG\_BLANK\_GROUP\_X}$, see the Table 65) is elapsed. This blanking time is applied on the first channel turn on as well as on each PWM rising edge.

The ADC monitoring of all these parameters allows a complete diagnostic: open-load, output channel short to external pre-regulator, output channel LED (single or multiple) short detection, LED current derating in case of device temperature increasing.

The LDLL16EN features an 8-bit logarithmic PWM for dimming control to adjust separately the brightness for each channel. A linear 8-bit global dimming dedicated for each function group mapped with Direct Input pin can be superimposed with the channel individual dimming.

A slow turn-on and turn-off time (t_{SR_ON} and t_{SR_OFF}) of the channel improves the system low noise generation performances. Moreover, this device features the output gradual delay (t_{GD}) which avoids contemporary turning on of all the channels used for a specific light function, reducing the inrush current.

To further improve EMI performances, the device implements an internal clock dithering to have a spread spectrum noise reduction.

The LDLL16EN integrates a thermal sensor block used to sense the device junction temperature (T_J) as well as to detect thermal warning (TW) and thermal shutdown (TSD) thresholds, granting device protection in case of temperature increasing.

The sensed junction temperature (T_J) is monitored by an 8-bit ADC with the aim of starting an automatic, downwards derating of the LED string current as soon as the TW threshold is reached. The derating ends when the value (I_PROG-Imin)/2+Imin of LED current is reached, which corresponds to T_J = 165 °C.

The 8-bit ADC is also used to monitor the voltage on the NTC pin, where an external resistor can be connected. If the monitored voltage, whose value depends on the temperature detected by the NTC resistor itself, reaches the V_{NTC_TH} threshold (programmable by 3 bits, see the Table 64), a downwards derating of the LED string current automatically starts, till a fraction of the nominal LED current is reached , this LED current end value is calculated as (I_PROG-Imin)/2+Imin. This corresponds to a NTC temperature 20 °C higher than V_{NTC_TH}.

The monitoring of both T_J and NTC voltage is contemporary active.

The device can be controlled by microcontroller via CAN FD light compatible interface. Stand-alone operation (no microcontroller used) is also possible thanks to direct drive functionality and full configurability by FTP. This latter can be programmed (up to N_{FTP} cycles) in application via CAN FD light compatible interface. Moreover, there is the possibility to lock any FTP area to avoid unintentional writing.

3.2 Channel current setting

The LDLL16EN features 16 low-side linear current generators to regulate from 6.3 mA to 100 mA current on the output LED strings. The current can be individually programmed per channel through 8-bit DAC per channel (setting CUR_SET_CHx bits, see the Section 6: FTP and RAM memory mapping).

The output channels can be put in parallel to address all those light functions needing higher current than the programmable one.

Moreover, the value programmed in the 8-bit DAC per channels group is stored in the RAM and can be reconfigured dynamically in bus/normal mode.

3.3 Channel driver drop-out voltage

To guarantee the regulation of the programmed channel current, a minimum output voltage (V_{OUTx_DROP}) across each current generator must be ensured.

The Table 2 shows the minimum channel V_{OUTx_DROP} at the boundary of the regulation region (output current is 3% less than the target value, output power MOS already in the triode region).

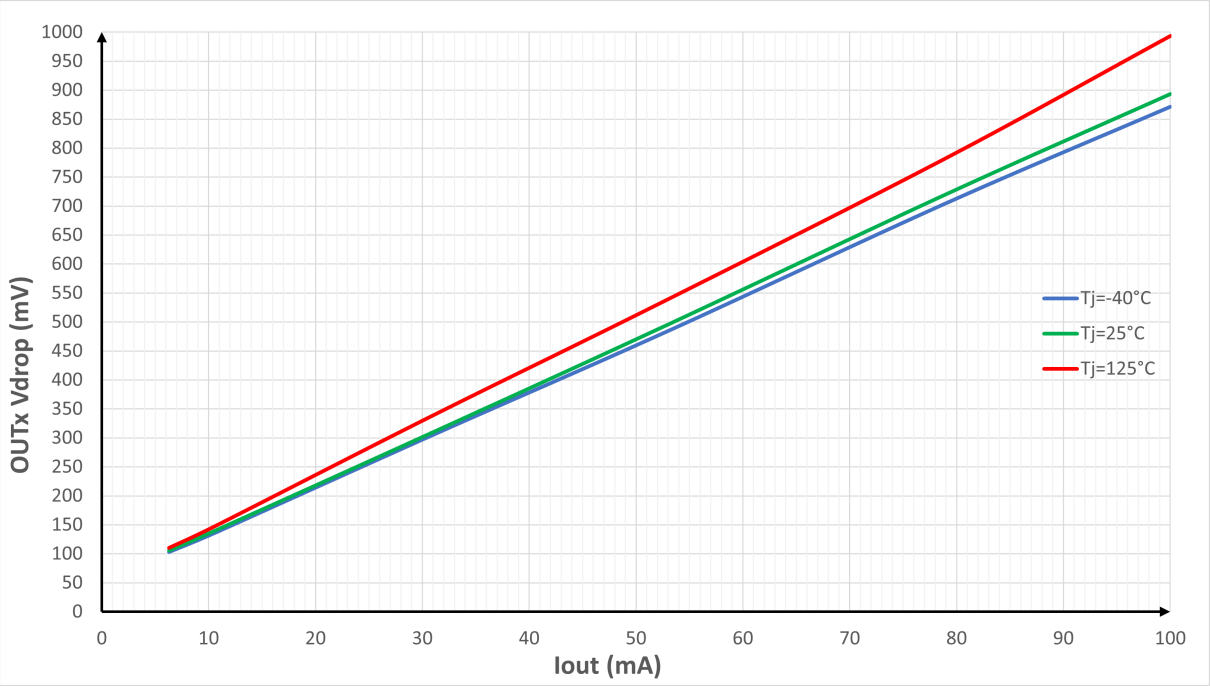
If on one hand a lower than minimum recommended V_{OUTx_DROP} leads to a regulated current lower than the expected one, a too high V_{OUTx_DROP} implies too high power dissipation.

To guarantee the current regulation while optimizing the power dissipation on each channel, in the case of maximum current set on one channel and T_J at 125 °C (worst case condition), the minimum output voltage drop (from device OUTx to device GND) is 1 V. In Figure 5. Output channels voltage drop in function of the output current and temperature is shown the generic channel drop-out voltage as function of the channel output current for the 3 main temperature values.

Table 2. Minimum channel drop-out voltage at maximum current vs T_J

T_J [°C]	V_{OUTx_DROP} [V]
125	1
25	0.9
-40	0.875

Figure 5. Output channels voltage drop in function of the output current and temperature



3.4 Channel output gradual delay

The LDLL16EN features the output gradual delay, which consists in a gradual turning on of the current generators. In case of driving several outputs simultaneously, the output gradual delay is applied in order to lower the current transients and improve device emissions. This feature can be activated – for all the channels - through one dedicated bit (OUT_DELAY, see the Section 6: FTP and RAM memory mapping).

In case one or more channels are not enabled, a gradual delay is increased according to the number of channels turned OFF.

The gradual delay concept is valid in PWM mode as well: in this case, the PWM waveform is shifted and the gradual delay is applied also when channel is turned OFF.

The output gradual delay feature is valid both for normal/bus mode and fail-safe/stand-alone mode. In this latter case, direct input (DIN) controls output channels as per FTP setting (DIN_MAP_CHx, 1 bit, see the Section 6: FTP and RAM memory mapping).

The delay between each output, in DC and PWM mode, is showed in Figure 6 and the Figure 7.

Figure 6. Gradual delay concept - GD active and DC = 100%

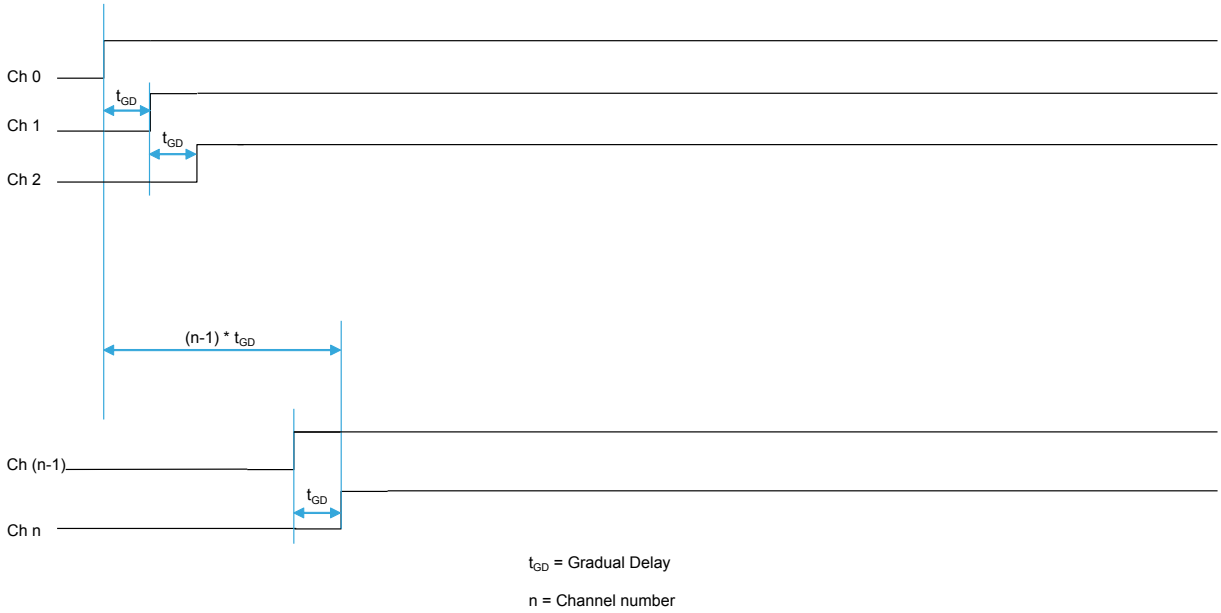
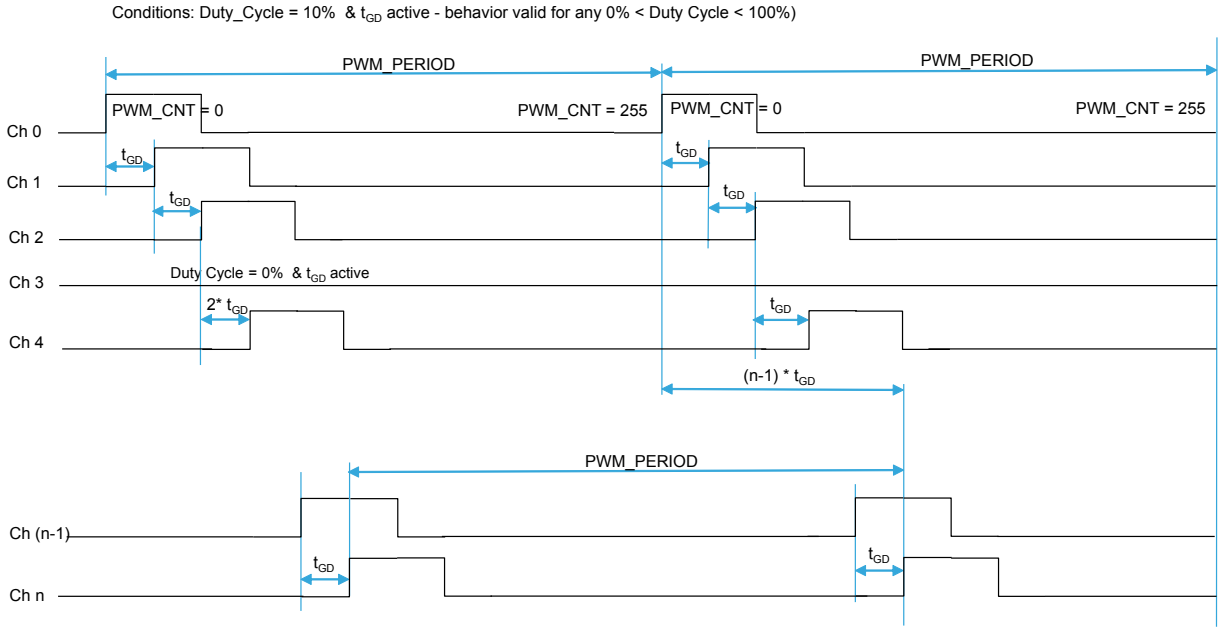


Figure 7. Gradual delay concept - GD active and DC = 10%



4 Functional description

4.1 Operating modes

The LDLL16EN features different operating modes. The related device states are reported in Figure 8 and well detailed in the following sub-chapters.

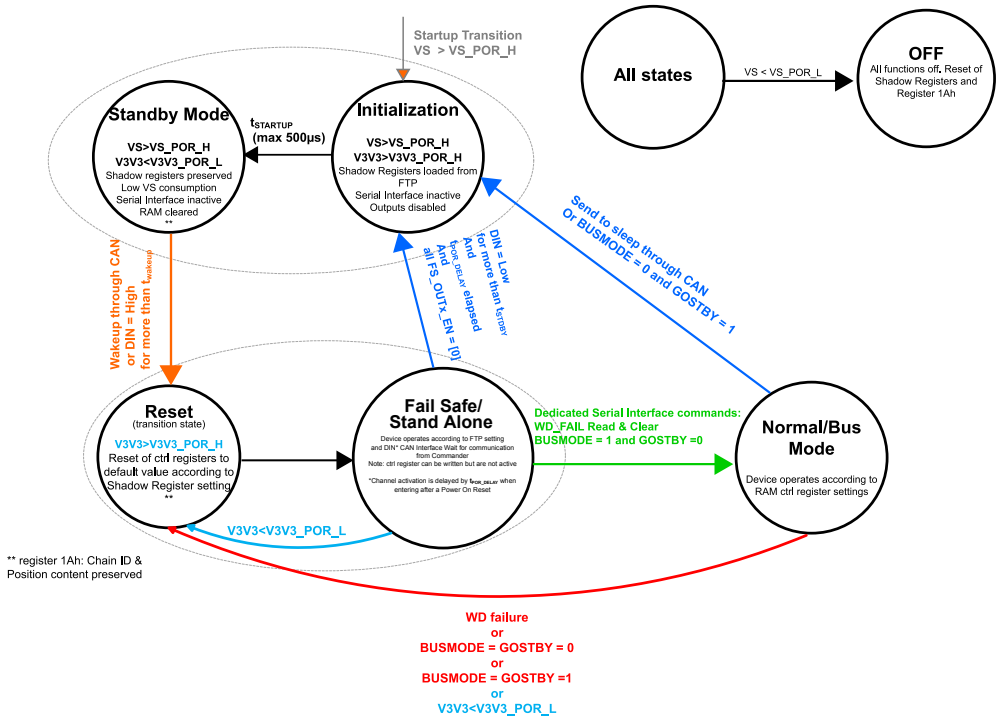
There are 2 bits for safe transition between different modes: BUSMODE and GOSTBY bits (see the Section 6: FTP and RAM memory mapping) configuration is used to set, leave and check device normal/bus operating mode.

A dedicated pattern through the CAN FD light compatible interface is used to wake up and to send to sleep the device. On top of that, the device can be opportunely woken up or sent to sleep also through the DIN pin and (BUSMODE, GOSTBY) bits respectively.

As the device potentially controls safety critical functions such as brake and turn indicators, built-in features are integrated to support a high level of functional safety on the application level. The LDLL16EN features a programmable timeout watchdog by WD_CONF (2 bits, see the Section 6: FTP and RAM memory mapping), a monitoring of the watchdog counter by WD_STATUS (2 bits, see the Section 6: FTP and RAM memory mapping), a fail-safe, and a direct input mode.

To keep the device in normal/bus mode, a watchdog trigger bit (WD_TRIG<0>, see the Section 6: FTP and RAM memory mapping) is cyclically toggled within the programmable watchdog timeout period. In case of watchdog failure, the WD_FAIL bit (see the Section 6: FTP and RAM memory mapping) is set and the device leaves normal/bus mode operation to enter fail-safe mode.

Figure 8. Device state diagram



Note: Partial networking feature is not supported by the device. Mixed state on the bus has to be avoided. In case devices are sent to initialization/standby mode NOT through a broadcast "send to sleep" command, the first UNICAST response frame of the device after wakeup has to be ignored.

4.1.1 Standby mode

The prerequisite for this mode is:

- Device in initialization phase

The device enters standby mode under the following condition:

- By default, once the device is powered (V_S present) and leaves the initialization phase ($V_S > V_{S\_POR\_H}$)

The standby mode characteristics are:

- Shadow register(1) preserved
- RAM cleared
- $V_S > V_{S\_POR\_H}$
- $V_{3V3} < V_{3V3\_POR\_L}$
- V_S low consumption
- CAN FD light compatible interface inactive - RX pin in recessive state for more than t_{RX_IDLE}

1. *Shadow registers are RAM copy of FTP registers, added to speed up the transition between standby to fail-safe modes and fail-safe to normal modes.*

The device leaves this mode if:

- Wake up (WUP) pattern is sent through CAN FD light compatible interface

Or

- DIN High for a time $t > t_{WAKEUP}$

4.1.2 Initialization

The device enters initialization phase under the following conditions:

- Sleep pattern sent through CAN FD light compatible interface

Or

- One frame setting bit (BUSMODE,GOSTBY) = (0,1)

Or

- DIN low for a time $t > t_{STDBY}$ AND power on reset delay time (t_{POR_DELAY}) elapsed AND all channels NOT set permanently ON in fail-safe (all FS_OUTx_EN bits = [0])

The initialization mode characteristics are:

- $V_S > V_{S\_POR\_H}$
- $V_{3V3} > V_{3V3\_POR\_H}$
- Shadow register(1) loaded from FTP
- Outputs disabled
- CAN FD light compatible interface inactive

1. *Shadow registers are RAM copy of FTP registers, added to speed-up transition between standby to fail-safe modes and fail-safe to normal modes.*

The device leaves automatically initialization mode entering standby mode after $t_{STARTUP}$.

4.1.3 Reset mode

The device enters reset mode (transition state) under the following conditions:

- By default, once the device leaves standby mode;
- If device state is fail-safe/stand-alone mode, when $V_{3V3} < V_{3V3\_POR\_L}$
- If device state is normal/bus mode, when one of the following events occurs:
  - Watchdog failure
  - One frame setting bits (BUSMODE,GOSTBY) = (0,0)
  - One frame setting bits (BUSMODE,GOSTBY) = (1,1)
  - $V_{3V3} < V_{3V3\_POR\_L}$

The reset mode characteristics are:

- $V_{3V3} > V_{3V3\_POR\_H}$
- Reset of control register to default values according to the shadow register setting
- CAN FD light compatible interface inactive

The device leaves automatically reset mode and enters fail-safe/stand-alone mode after 400 ns (typical).

4.1.4 Fail-safe/Stand-alone mode

The device enters fail-safe/stand-alone mode automatically 400 ns (typical) after reset mode.

Fail-safe/stand-alone mode characteristics are:

- Device operates according to FTP setting and direct input
- CAN FD light compatible interface wait for communication from the commander

Note: Control registers can be written but are not active.

When the device leaves this mode, it can enter standby or normal/bus mode. If the device receives the two following frames:

- The first frame reads and clears the WD_FAIL bit (bit <15>, Device status register #3)
- The second frame (not necessarily directly consecutive to the first frame) sets BUSMODE = 1 and GOSTBY = 0 (bit <0-1>, Device configuration register #4)

The device enters in bus mode.

Note: If WD_FAIL read and clear operation is not performed (and in case of WD_FAIL = 1) device state remains in fail-safe but control register is reset to default value.

Upon the condition:

- DIN low for a time $t > t_{STDBY}$ AND power on reset delay time (t_{POR_DELAY}) elapsed AND all channels NOT set permanently ON in fail-safe (all FS_OUTx_EN bits = [0])

The device enters standby mode.

Upon the condition:

- $V_{3V3} < V_{3V3\_POR\_L}$

The device enters in reset transition mode:

- RAM content is reloaded with shadow register content
- Device remains in fail-safe state with GSB.RSTB = 1, to inform the user any potential write operations already performed in fail-safe has to be repeated

4.1.5 Normal/Bus mode

The device enters the normal/bus mode if the device receives the following frames:

- The first frame reads and clears the WD_FAIL bit (bit <15>, Device status register #3)
- The second frame sets BUSMODE = 1 and GOSTBY = 0 (bit <0-1>, Device configuration register #4)

Note: If WD_FAIL read and clear operation is not performed (and in case of WD_FAIL = 1) device state remains in fail-safe but control register is reset to default value.

In this mode the device operates according to its RAM register settings. Direct input access can be enabled/disabled by a dedicated bit (DIN_EN). In order to maintain the device in normal/bus mode the watchdog toggle bit has to be refreshed within the watchdog timeout time-frame.

The device leaves normal/bus mode, entering initialization state (to refresh shadow register with FTP configuration), upon the following conditions:

- Send to sleep pattern is sent through CAN FD light compatible interface or
- BUSMODE = 0 and GOSTBY = 1

The device leaves normal/bus mode, entering reset transition state, upon the following conditions:

- Watchdog failure
- One frame setting bits (BUSMODE,GOSTBY) = (0,0)
- One frame setting bits (BUSMODE,GOSTBY) = (1,1)

- $V_{3V3} < V_{3V3\_POR\_L}$
  - RAM content reloaded with shadow register content
  - Device will reach fail-safe state with GSB.RSTB = 1, to inform the application about the reason of this transition

4.2 Programmable functions

4.2.1 Direct drive and functional configuration

Output channels assignement

The LDLL16EN features 1 direct input pin (DIN).

Each output can be assigned to DIN or to none by 1 dedicated FTP bit (DIN_MAP_CHx, see the Section 6: FTP and RAM memory mapping) per output channel, as showed in Table 3.

Table 3. Output channel mapping to DIN

DIN_MAP_CHx <0>	Output Channel Status
0	OUTx NOT mapped (Group 0)
1	OUTx mapped on DIN (Group 1)

In fail-safe/stand-alone mode, the outputs are always controlled by DIN - according to the assignment defined in Table 3, except the case when the channel is programmed permanently ON by dedicated FTP bits (FS_OUTx_EN <0>, see the Section 6: FTP and RAM memory mapping). When this bit is set, the related output channel “x” is permanently active in fail-safe/stand-alone mode regardless of the DIN, see Table 4.

Table 4. Output channel in fail-safe/stand-alone mode

FS_OUTx_EN <0>	Output channel status
0	OUTx according to DIN_MAP_CHx <0>
1	OUTx permanently ON

In case the channel is configured ON in fail-safe/stand-alone mode, a configurable delay of the output activation after power on reset (t_{POR_DELAY}) prevents any undesired flashing while configuring the devices and entering normal/bus mode. In other words, after power on reset, all outputs are kept off till power on reset delay time elapses to prevent any flashing during the time needed to enter in bus mode operation.

In normal/bus mode, the direct inputs access to outputs can be enabled/disabled for each channel. If enabled (DIN_EN), bus control is applied when DIN = 0. If DIN is set (DC or PWM) the bus control is automatically disabled (after elapsing of t_{FILTER}) and overtaken by DIN (the direct inputs have priority versus bus control). Bus control is re-established upon $t_{BUS\_CONTROL}$ elapse after last falling edge on DIN.

For DIN, a read-back information is available. It is forecasted one status bit (DIN_STATUS <0>, see the Section 6: FTP and RAM memory mapping) to support functional safety.

The LDLL16EN features also 1 V_{PREG} pin to supply the anode of the LED strings through an external pre-regulator.

4.2.2 PWM operation

In the LDLL16EN, the brightness of LED strings can be modified by PWM. The PWM dimming could be performed in different ways:

- Through serial bus
- Through direct input
- Through power line

When PWM operation is managed through the serial bus, there are 3 bits (PWM_FREQ, see the Section 6: FTP and RAM memory mapping) to configure the PWM frequency of the channels.

The PWM frequency range is reported in the table below.

Table 5. PWM frequency range

PWM_FREQ [2÷0]			PWM_FREQ [Hz]
bit 2	bit 1	bit 0	
0	0	0	200
0	0	1	300
0	1	0	400
0	1	1	500
1	0	0	700
1	0	1	1000
1	1	0	1200
1	1	1	1400

For all the non-mapped output channels (see Table 3), the PWM frequency and duty cycle is the same as DIN mapped channels (as reported in the dimming with direct input in fail-safe/stand-alone mode section).

Dimming with serial bus

In the LDLL16EN, each channel can be individually dimmed on 8-bit exponential duty cycle to adequate LED brightness change to human eye light perception, giving in this way the impression of brightness linear variation. The exponential law used to calculate the dimming steps is the following:

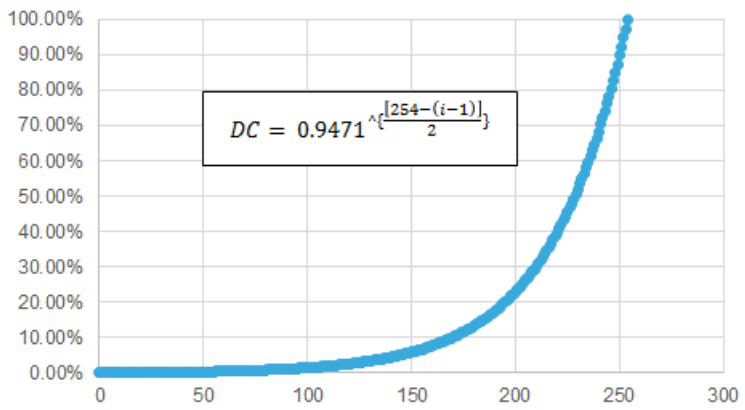
$$ton_i = PWM_{period} \cdot \alpha^{\Lambda\left\{\frac{[N-(i-1)]}{2}\right\}} \quad (1)$$

Where ton_i is the LED ON-time during step number "i", $1 \le i \le 255$, $\alpha \approx 0.9471$, $N = 254$.

For the step number "i" = 0, DC is set to "0".

The function of duty cycle vs 8-bit PWM_DUTY_CHx setting is shown in the following graph. The minimum duty cycle is clamped to 0.1% in any case.

Figure 9. Duty cycle vs PWM_DUTY_CHx

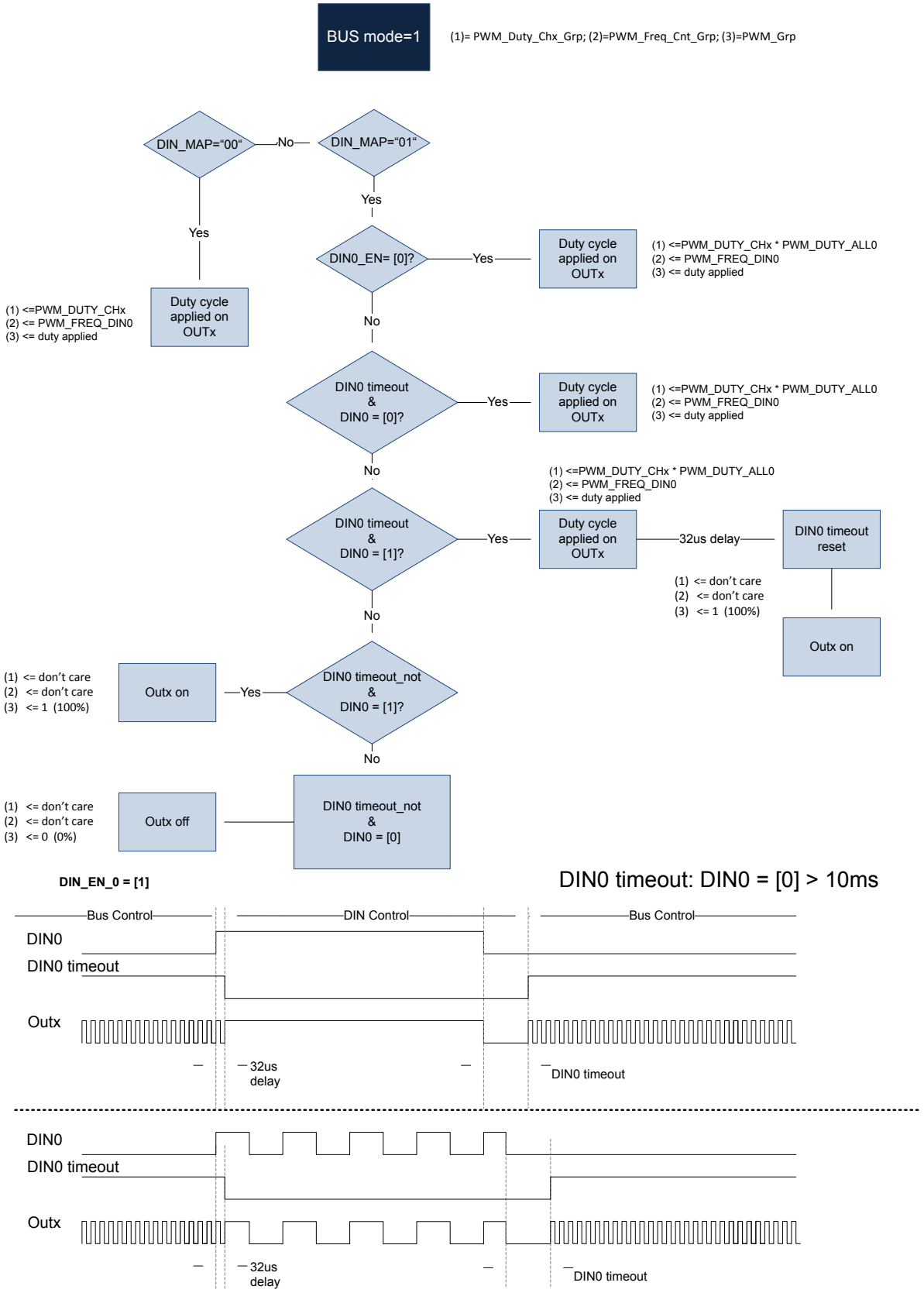


The duty cycle is configurable through serial bus (PWM_DUTY_CHx, 8-bit per channel, see the Section 6: FTP and RAM memory mapping) and the programmed value is stored in the RAM.

The individual duty cycle per channel can be superimposed by a linear 8-bit global dimming PWM_DUTY_ALL (applicable for outputs mapped to DIN). The resulting duty cycle is the product of PWM_DUTY_CHx*PWM_DUTY_ALL. Global dimming is not available for function group not mapped to DIN. If global dimming is not desired, the PWM_DUTY_ALL register has to be programmed with FFh.

Direct input access to outputs can be enabled or disabled for each channel separately in bus/normal mode. If direct input is enabled (by DIN_EN configuration bit, see the Section 6: FTP and RAM memory mapping), bus control is applied when DIN = 0. In case of DIN <> 0, the bus control is automatically disabled (after t_{FILTER} filtering time) and overtaken by DIN: the DIN input control has priority versus bus control. After a timeout higher than $t_{BUS\_CONTROL}$ after the last falling edge on DIN, the bus control is reactivated. The characteristics of the function group are illustrated in the following flow chart.

Figure 10. PWM concept for DIN function group



The PWM frequency and phase relation of several devices can be synchronized versus each other through the SYNC_IO pin. There is one dedicated bit (SYNC_IO_PC, see the Section 6: FTP and RAM memory mapping) to configure the device in Provider [1] or Consumer [0] mode.

In provider mode, the clock frequency with scaler and phase signal is transferred to the SYNC_IO line. In consumer mode, clock frequency and phase signal on the SYNC_IO line is used to synchronize its own clock. Consequently the phase relation among several devices can be configured, through FTP only, by PHASE_DEV bits (3 bits, see the Section 6: FTP and RAM memory mapping).

Table 6. PWM phase shift (in consumer mode)

PHASE_DEV [2÷0]			PWM_PHASE_SHIFT [µs]
bit 2	bit 1	bit 0	
0	0	0	0
0	0	1	15
0	1	0	30
0	1	1	45
1	0	0	60
1	0	1	75
1	1	0	90
1	1	1	105

The internal PWM clock oscillator can be reset by PWM_SYNC bit (see the Section 6: FTP and RAM memory mapping) in order to start the PWM period at a known phase relation.

Dimming with direct input in fail-safe/stand-alone mode

The LDLL16EN features the channel output PWM dimming through direct input control.

The direct Inputs control the output channels as per FTP setting (see Table 3).

There is 1 configuration bit (PWM_FS_ALL_EN, see the Section 6: FTP and RAM memory mapping) for enabling internal PWM dimming in stand-alone/fail-safe mode. The PWM signal is deactivated by the related DIN: if DIN = 0, the outputs are off; otherwise the outputs follow the internal PWM signal.

The channel PWM control concept in fail-safe/stand-alone mode is illustrated in the following flow charts.

Figure 11. PWM control concept fail-safe/stand-alone mode main layer

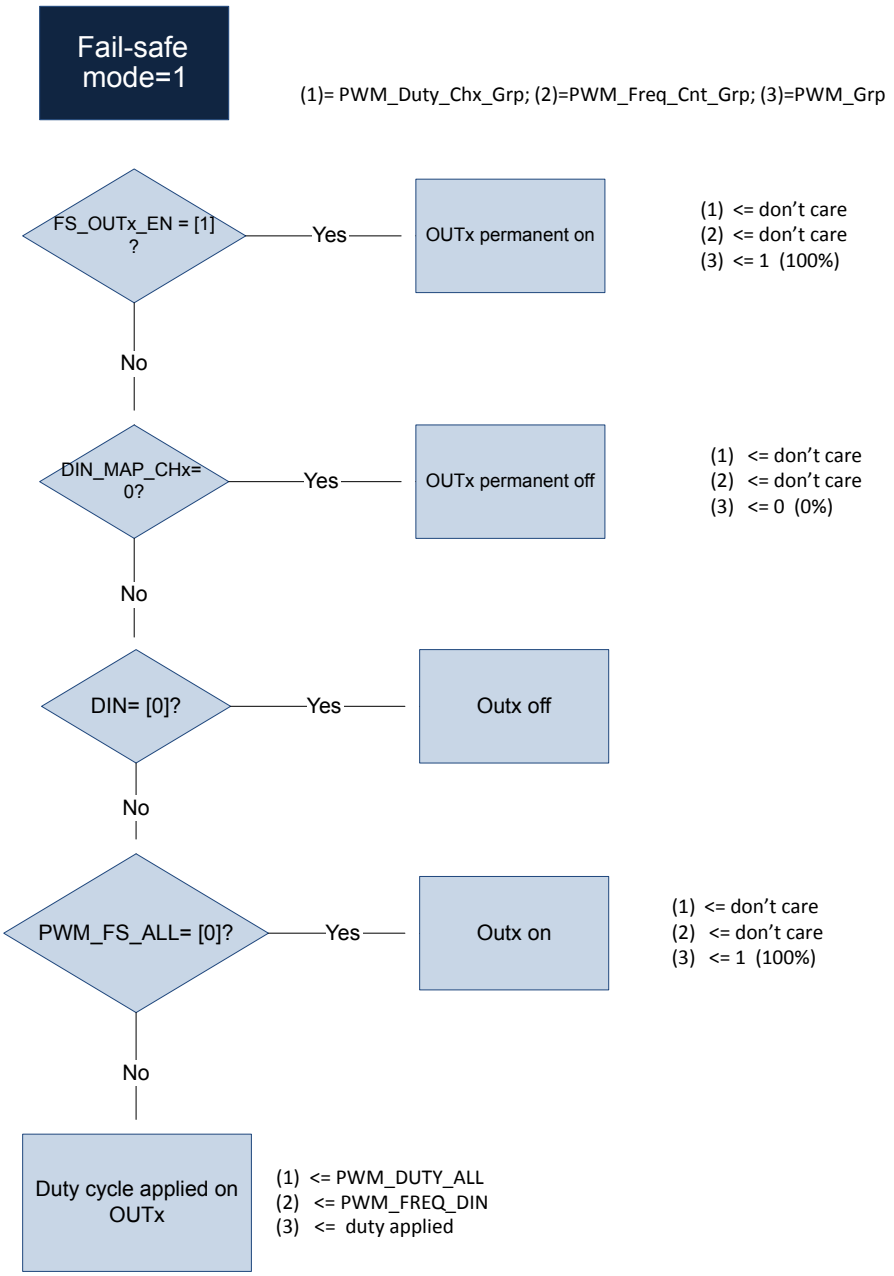
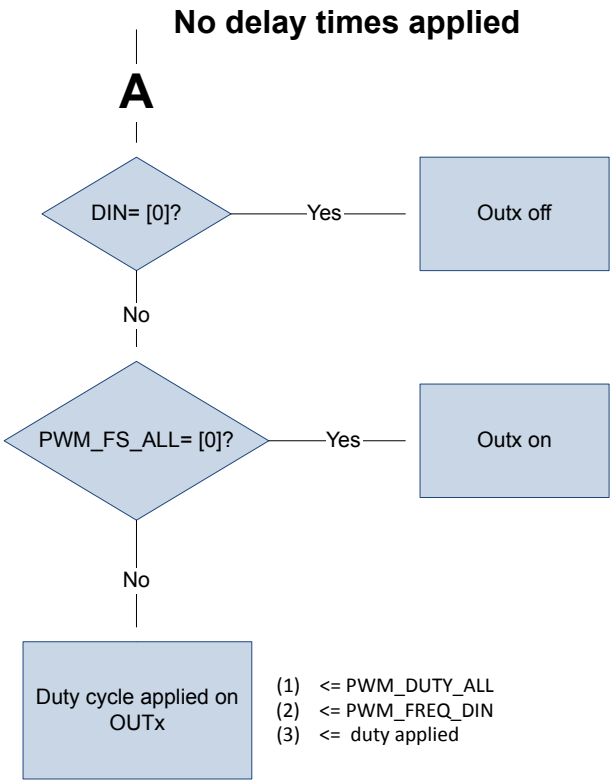


Figure 12. **Output and PWM control concept DIN (Group 1)**



Dimming with power line

In the LDLL16EN, PWM dimming through power line is possible by rectifying the V_S supply and connecting the power line to the direct input through resistor divider. A buffer capacitor on V_S supply pin has to be able to supply the device during PWM off state to keep it in operating mode without any reset.

When dimming through power line is performed, PWM frequency is expected in the range of [100÷200 Hz] with 5% minimum duty cycle. The startup time for light function availability is $t_{STARTUP\_PWM\_VS}$.

The $t_{STARTUP\_PWM\_VS}$ parameter is the time needed for device startup, from device power up (presence of V_S) to the channel activation.

4.3 Protections and diagnostic

4.3.1 Diagnostic availability and validation - strategy

The LDLL16EN performs a configurable blanking time for the diagnosis, which is applied on the first channel turn on as well as on each PWM rising edge.

There are 2 configuration bits per each group of channels (DIAG_BLANK_GROUP_X, see the Section 6: FTP and RAM memory mapping) to set the desired blanking time before validating any fault related to the channel, either NOT mapped or mapped to DIN.

The possible configuration values are reported in the table below.

Table 7. **Diagnostic blanking time configuration**

DIAG_BLANK_GROUP_X [1÷0]	$t_{DIAG\_BLANK\_GROUP\_X}$ [µs]
00	5
01	10
10	15
11	20

After $t_{DIAG\_BLANK\_GROUP\_X}$ elapses, a failure counter starts, and any channel fault is validated after N_Fails number of detected failures (also non-consecutive). The N_Fails readings are kept in memory up to N_Fails_reset (number of consecutive NOT failures detection), then the counter will be reset.

Diagnostic validation strategy is applied to any possible load fault: LED shortage, output channel short to V_{PREG}, open-load. If the on-time of any channel is shorter than the configured blanking time, the device automatically disables fault detection.

4.3.2 Fault reaction mode and fault bus capability

In the LDLL16EN, there is 1 fault pin with "Fault Bus" capability: 1 open drain fault pin (FAULT) is associated with 1 direct input (DIN), output channels are mapped according to DIN_MAP_CHx.

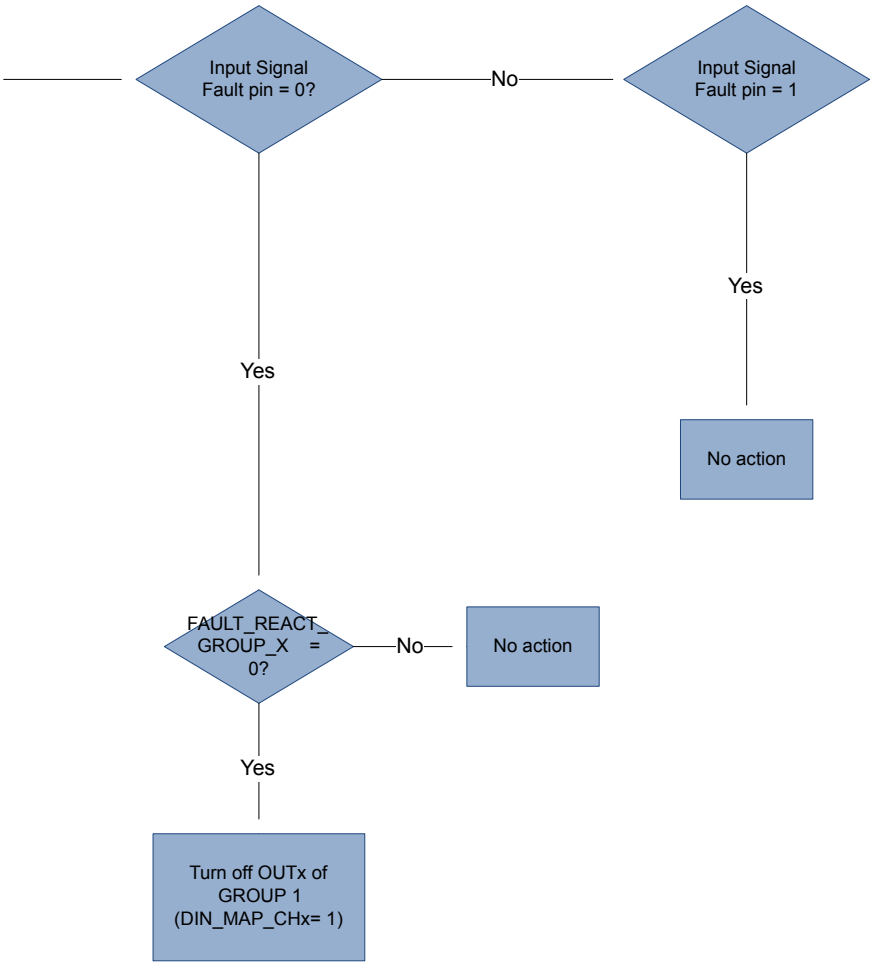
The fault pin is bidirectional, active low. The fault pins of several devices can be connected all together to have a common fault bus associated to a particular light function. This allows an automatic deactivation of complete light function in case of fault on single LED string only, according to the selected fault reaction mode.

There is, in fact, 1 bit per each group (FAULT_REACT_GROUP_X, see the Section 6: FTP and RAM memory mapping) for fault reaction mode configuration:

Table 8. Fault reaction mode configuration

FAULT_REACT_GROUP_X <0>	Fault reaction mode
0	Fault on one string => all strings of same group deactivated
1	Fault on one string => no action on other strings of same group

Figure 13. Device reaction on fault inputs - flow chart



4.3.3 Thermal warning

The LDLL16EN integrates a temperature warning with one threshold.

If the junction temperature (T_J) of the device, read by 8-bit internal ADC, rises above the threshold (T_{TW}), the thermal warning status bit (TW, see the Section 6: FTP and RAM memory mapping) is set. Thermal warning is also reported in the global status byte register, in particular global warning (GW) bit is set.

As soon as the T_J drops below the thermal warning reset threshold (T_{TW} - T_{TW_HYST}), the corresponding thermal warning status bit is automatically cleared.

Even if a temperature warning is detected, device as well as output channels are kept functional.

To avoid further temperature increase, it is possible to start a thermal derating, if set, when thermal warning threshold is reached.

4.3.4 Thermal shutdown

If the junction temperature of the LDLL16EN rises above the shutdown temperature threshold (T_{TSD}), a thermal shutdown event is detected: all the output channels are switched off and the thermal shutdown status bit (TSD, see the Section 6: FTP and RAM memory mapping) is set. The fault pin (FAULT) is pulled low.

Thermal shutdown event is also reported in the global status byte register, in particular functional error 1 (FE1) bit is set.

As soon as the T_J drops below the thermal shutdown reset threshold (T_{TSD} - T_{TSD_HYTS}), the output channels are automatically re-activated. The corresponding thermal shutdown status bit (T_{TSD}) is automatically cleared as soon as T_J drops below the thermal shutdown reset threshold (T_{TSD} - T_{TSD_HYST}), contemporarily to channel re-activation.

In case of thermal shutdown, device logic and state machine remain active.

4.3.5 LED current derating

In case of temperature increasing, the device performs an automatic LED current derating based on the measurement of external NTC voltage as well as on the internal device temperature (T_J).

An integrated thermal sensor is used to sense the device junction temperature (T_J) as well as to detect thermal warning (TW) and thermal shutdown (TSD) thresholds, granting device protection in case of temperature increasing. The sensed junction temperature (TJ) is monitored by 8-bit ADC with the aim of starting an automatic, downwards derating of the LED string current as soon as the TW threshold is reached. The derating ends when the value (I_PROG-Imin)/2+Imin of LED current is reached, which corresponds to T_J = 165 °C.

The 8-bit ADC is also used to monitor the voltage on the NTC pin, where an external resistor can be connected. If the monitored voltage, whose value depends on the temperature detected by the NTC resistor itself - reaches the V_{NTC_TH} threshold (programmable by 3 bits, see the Table 64), a downwards derating of the LED string current automatically starts, till a fraction of the nominal LED current is reached , this LED current end value is calculated as (I_PROG-Imin)/2+Imin. This corresponds to a NTC temperature 20 °C higher than V_{NTC_TH}.

The monitoring of both T_J and NTC voltage is contemporarily active. The actual derating is determined by the parameter which would require the most severe derating.

4.3.6 V_S undervoltage lockout

If the V_S supply falls below VS undervoltage threshold (V_{S_UV}), the device is deactivated - regardless of the operating mode, and the fault pin (FAULT) is pulled low. This feature is implemented, in order to avoid any operation outside the allowed V_S operating range.

If supply undervoltage event is detected, the related flag (V_{S_UV}, see the Section 6: FTP and RAM memory mapping) is set and reported also in the global status byte register, where device error (DE) bit is set.

As soon as the V_S supply crosses the undervoltage reset threshold ($V_{S\_UV\_RST}$) the device is automatically re-activated.

4.3.7 Channel output – LED short circuit detection

The LDLL16EN features the LED (single or multiple) short circuit fault detection, both in bus mode and fail-safe/ stand-alone mode, based on voltage monitoring across the channel output voltage: the detection is done by comparing the absolute output voltage (VOUTx) versus a configurable threshold.

The device features 2 configurable short circuit thresholds ($V_{SHT\_TH\_GROUP\_X}$, see the Table 9).

This configurability allows the short detection of one or more LEDs shortage within the string connected to a given channel mapped according to DIN_MAP_CHx <0>.

The LED short circuit detection is masked when the LED supply voltage (V_{PREG}) is below a power good threshold ($V_{PG\_TH\_VPREG}$), which is configurable in the range of [$V_{PG\_TH\_VPREG\_min}$ ÷ $V_{PG\_TH\_VPREG\_max}$] with a step equal to $V_{PG\_TH\_VPREG\_step}$.

There is one status bit (PG_NOT_VPREG, see the Section 6: FTP and RAM memory mapping) to indicate the selected voltage threshold is reached. If this bit is equal to "1", the desired voltage threshold is not reached and the diagnostic disabled; otherwise, the threshold is reached and the diagnostic enabled.

After power good threshold is reached, the short circuit detection starts and the channel is recognized in fault as soon as its output voltage, read by ADC - is higher than the specified threshold ($V_{SHT\_TH\_GROUP\_X}$).

Table 9. LED short circuit threshold - group

DIN_MAP_CHx <0>	Short circuit threshold group
0	Short circuit threshold for Group 0 ($V_{SHT\_TH\_GROUP\_0}$)
1	Short circuit threshold for Group 1 ($V_{SHT\_TH\_GROUP\_1}$)

The short circuit detection can be enabled /disabled through the SHT_DET_EN bit (see the Section 6: FTP and RAM memory mapping): if this bit is equal to "0", the short circuit detection is disabled (that is, if the channel is directly supplied from V_S instead of a pre-regulated voltage, it is recommended to disable short circuit detection, to avoid erroneous fault detection during voltage drops on V_S line); otherwise, the short circuit detection is enabled. In this latter case, two different scenarios are possible: enable or disable the channel output deactivation in case of short circuit, by one dedicated bit per each group (SHT_OFF_GROUP_X, see the Section 6: FTP and RAM memory mapping). If SHT_OFF_GROUP_X bit is set to 0, the faulty channel output is kept active in case of short circuit, otherwise the faulty channel is latched off. The channel is recognized in short circuit as soon as its output voltage, read by ADC, is less than the specified short circuit threshold ($V_{SHT\_TH\_GROUP\_X}$, see Table 9).

In bus mode, the faulty channel output is latched off and the dedicated fault bit (SHT_CHx, see the Section 6: FTP and RAM memory mapping) is set. The channel output can be restarted and the fault bit will be cleared by sending a read and clear command to address 28h. Selective bitwise read and clear is possible.

In case of fault in fail-safe/stand-alone mode:

- for the channels configured with FS_OUTx_EN = 0, the output is latched off and it is cleared upon falling edge of DIN with t_{DIN_FALL} settling time. This means that fault is not cleared during PWM dimming with PWM off-time shorter than t_{DIN_FALL} time.
- for the channels configured with FS_OUTx_EN = 1, after elapsing the $t_{AUTORESTART}$, the faulty channel is automatically re-activated and the SHT_CHx bit is cleared.

If outputs are permanently enabled by FS_OUTx_EN = 1, in case of LED short circuit, they will be latched and the latch can be cleared only through a power on reset condition.

For all those channels mapped on DIN (DIN_MAP_CHx = 1), the LDLL16EN features the indication of LED short circuit on FAULT pin.

If the bit SHT_EN (see the Section 6: FTP and RAM memory mapping) is equal to "0", the short circuit fault detection is NOT propagated on FAULT bus; whilst if SHT_EN = 1, the short circuit of the faulty channel is indicated on associated FAULT bus (pulled low).

The LED short event is also reported in the global status byte register, in particular functional error 2 (FE2) bit is set.

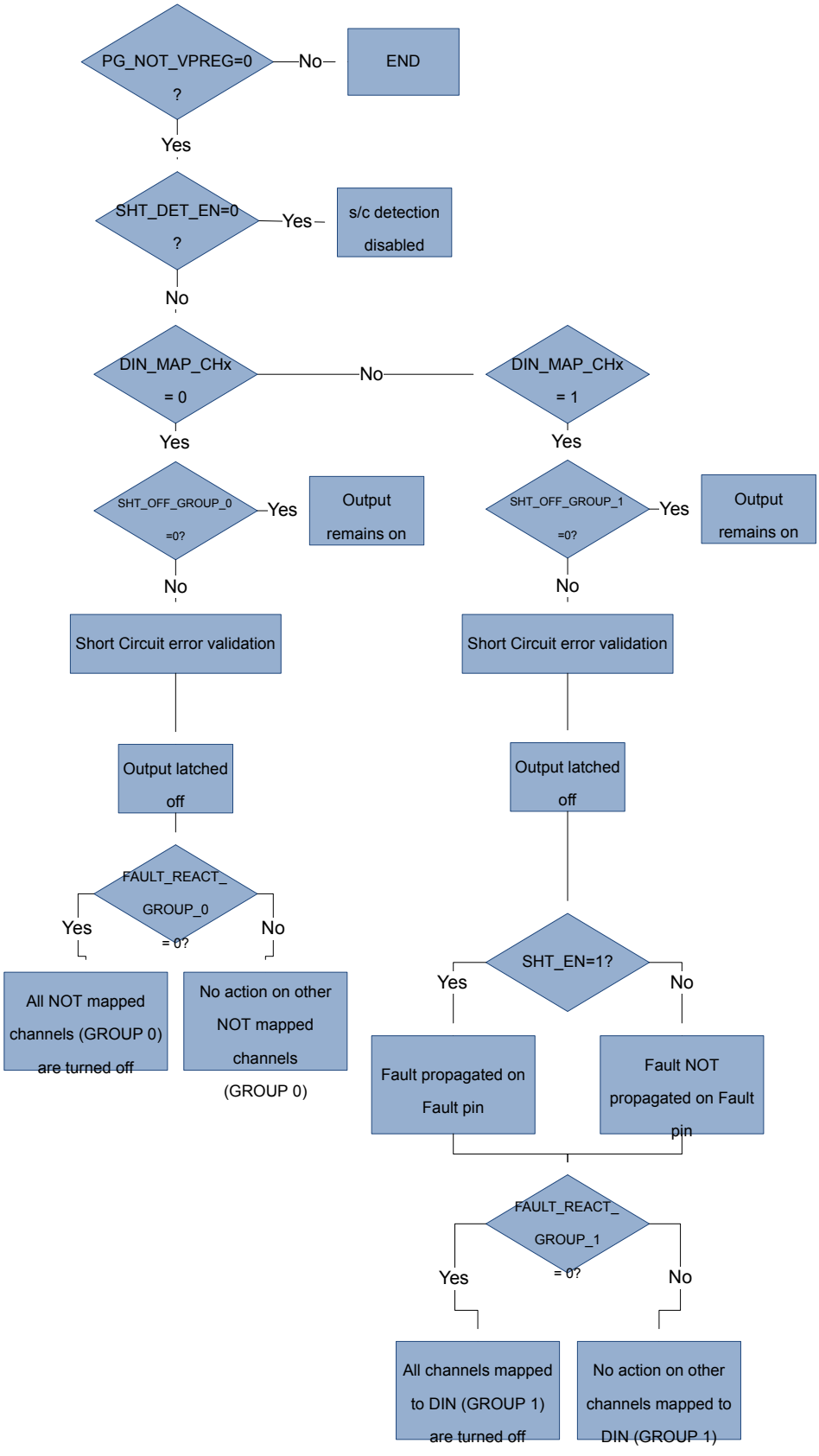
Then, for both mapped and non-mapped channels, according to the fault reaction mode configuration bit (see the Table 8), an automatic deactivation of the complete light function respectively of the faulty channel only is performed.

The flow chart reported in the Figure 14 shows how the device manages the faulty channel and the channels corresponding to DIN_MAP_CHx as well as the fault pin handling.

Figure 14. LED short circuit fault management

Validation:short circuit error counter reaches 15 detected events.

Counter is reset upon 3 consecutive no-fault samples.



4.3.8 Channel output – short circuit to V_{PREG}

The LDLL16EN features the output channel voltage shortage detection versus the external pre-regulator, both in bus mode and fail-safe/stand-alone mode, by comparing the voltage difference between V_{PREG} and V_{OUTx} (V_{LED}) versus a fixed threshold ($V_{OUT\_SHT\_PREG\_TH}$).

The short to V_{PREG} detection is masked when the LED supply voltage (V_{PREG}) is below a power good threshold ($V_{PG\_TH\_VPREG}$), which is configurable in the range of ($V_{PG\_TH\_VPREG\_min}$ ÷ $V_{PG\_TH\_VPREG\_max}$) with a step equal to $V_{PG\_TH\_VPREG\_step}$.

There is one status bit (PG_NOT_VPREG, see the Section 6: FTP and RAM memory mapping) to indicate the selected voltage threshold is reached. If this bit is equal to "1", the desired voltage threshold is not reached and the diagnostic disabled; otherwise, the threshold is reached and the diagnostic enabled.

After power good threshold is reached, the fault detection starts and the channel is recognized in fault as soon as V_{LED} is less than the specified threshold ($V_{OUT\_SHT\_PREG\_TH}$).

If a shortage between a channel output and the pre-regulated voltage is detected, the related channel bit (OUT_SHT_VPREG_CHx, see the Section 6: FTP and RAM memory mapping) is set.

When this flag is set, the faulty channel is disabled regardless of the setting of its own short off (SHT_OFF_GROUP_X) bit. The OUT_SHT_VPREG_CHx flag is a Read & Clear bit: channel "x" is latched off in case of fault, it will restart after bit clearing. If fault is still there, the channel will be latched off again.

In case of fail-safe/stand-alone mode, after elapsing the $t_{AUTORESTART}$, the faulty channel is automatically re-activated and the OUT_SHT_VPREG_CHx bit is cleared.

Channel output short to pre-regulator voltage event is also reported in the global status byte register, in particular functional error 2 (FE2) bit is set.

For all (and only) those channels mapped on DIN (DIN_MAP_CHx = 1), the LDLL16EN features the indication of short circuit to V_{P_REG} on FAULT pin.

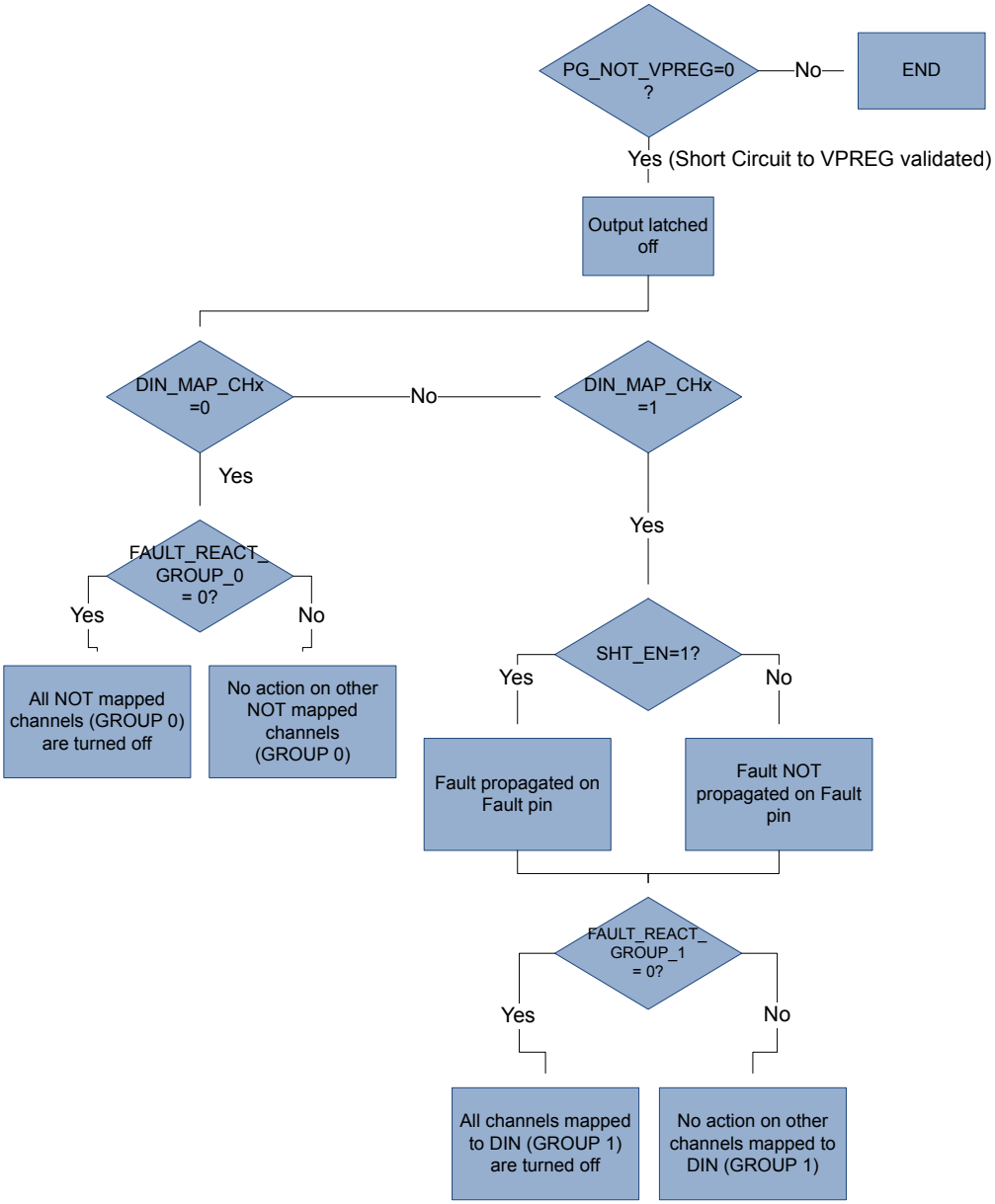
If the bit SHT_EN (see the Section 6: FTP and RAM memory mapping) is equal to "0", the short circuit fault detection is NOT propagated on FAULT bus; whilst if SHT_EN = 1, the short circuit of the faulty channel is indicated on associated FAULT bus (pulled low).

Then, for both mapped and non-mapped channels, according to the status of the fault reaction mode configuration bit (see Table 8), an automatic deactivation of the complete light function respectively of the faulty channel only is performed.

The flow chart reported in the Figure 15 shows how the device manages the faulty channel and the channels corresponding to DIN_MAP_CHx as well as the fault pin handling.

Figure 15. Short to V_{PREG} fault management

Validation:short circuit to VpreReg error counter reaches 15 detected events.
Counter is reset upon 3 consecutive no-fault samples.



4.3.9 Channel output – open-load detection

The LDLL16EN features the open-load (no current regulation) detection, implemented in both bus mode and fail-safe/stand-alone mode as well.

The open-load detection is masked when the LED supply voltage (V_{PREG}) is below a power good threshold ($V_{PG\_TH\_VPREG}$), which is configurable in the range of ($V_{PG\_TH\_VPREG\_min}$ ÷ $V_{PG\_TH\_VPREG\_max}$) with a step equal to $V_{PG\_TH\_VPREG\_step}$.

There is one status bit (PG_NOT_VPREG, see the Section 6: FTP and RAM memory mapping) to indicate the selected voltage threshold is reached. If this bit is equal to "1", the desired voltage threshold is not reached and the diagnostic is disabled; otherwise the threshold is reached and the diagnostic enabled.

After power good threshold is reached, the fault detection starts and the channel is recognized in open-load as soon as its output voltage, read by ADC, is less than the specified open-load threshold (V_{OL_TH}).

In bus mode, the faulty channel output is latched off and the dedicated fault bit (OL_CHx, see the Section 6: FTP and RAM memory mapping) is set. The channel output can be restarted and the fault bit will be cleared by sending a read and clear command to address 29. Selective bitwise read and clear is possible.

In case of fault in fail-safe/stand-alone mode:

- for the channels configured with FS_OUTx_EN = 0, the output is latched off and it is cleared upon falling edge of DIN with t_{DIN_FALL} settling time. This means that fault is not cleared during PWM dimming with PWM off-time shorter than t_{DIN_FALL} time;
- for the channels configured with FS_OUTx_EN = 1, after elapsing the $t_{AUTORESTART}$ time, the faulty channel is automatically re-activated and the OL_CHx bit is cleared.

For all (and only) those channels mapped on DIN (DIN_MAP_CHx = 1), the LDLL16EN features the indication of open-load on FAULT pin.

If the bit OL_EN (see the Section 6: FTP and RAM memory mapping) is equal to "0", the open-load fault detection is NOT propagated on FAULT bus; whilst if OL_EN = 1, the open-load of the faulty channel is indicated on associated FAULT bus (pulled low).

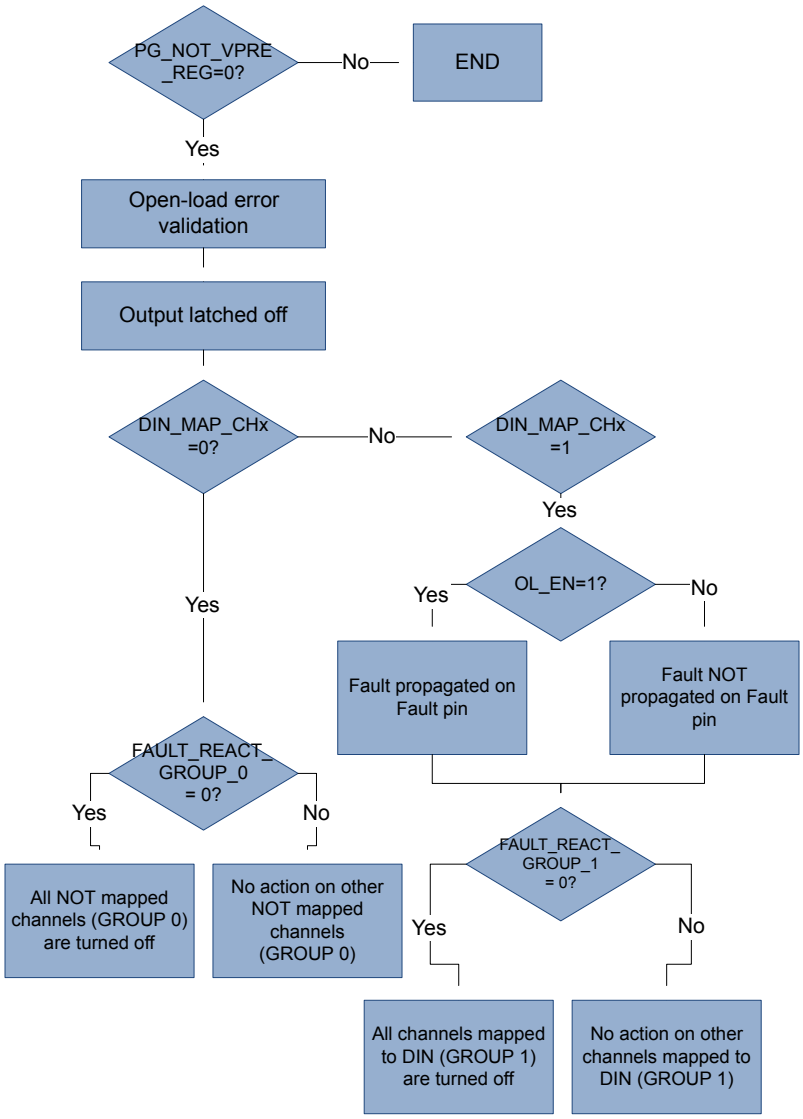
Channel open-load event is also reported in the global status byte register, in particular functional error 2 (FE2) bit is set.

Then, for both mapped and non-mapped channels, according to the status of the fault reaction mode configuration bit (see Table 8), an automatic deactivation of the complete light function respectively of the faulty channel only is performed.

The flow chart reported in the Figure 16 shows how the device manages the faulty channel and the channels corresponding to DIN_MAP_CHx as well as the fault pin handling.

Figure 16. Open-load fault management

Validation: open-load error counter reaches 8 detected events.
Counter is reset upon 3 consecutive no-fault samples.

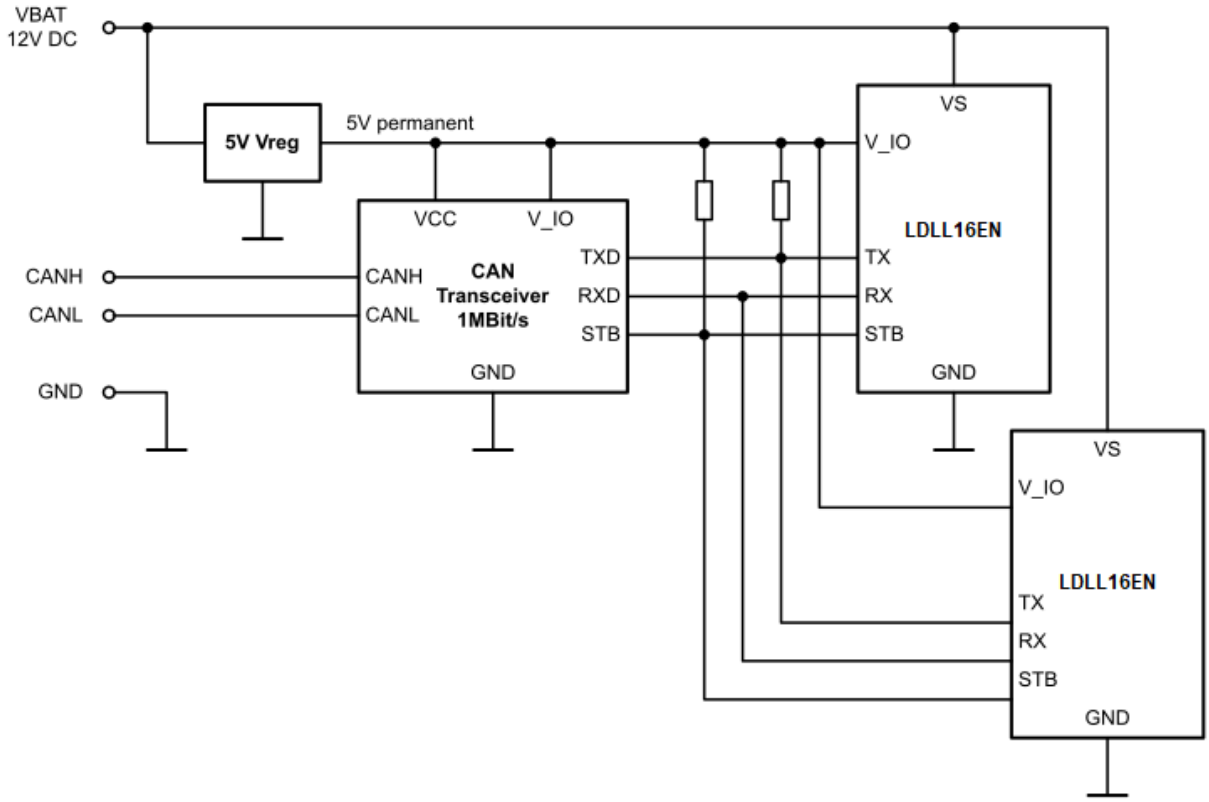


5 Communication interface

5.1 External CAN transceiver

The LDLL16EN provides an interface for connecting an external CAN transceiver. This interface has three logic pins (RX, TX, STB) and allows the parallel connection of several devices (up to 6) sharing one external CAN transceiver:

Figure 17. External CAN transceiver connection - example



The TX pin is an open drain output connected to transmit data to the transceiver. It has an active pull-up function, which improves the slope of the rising edges of the TX signal (except for the ACK-bit).

The RX pin is an input directly connected to receive data from the transceiver. It has a wake-up detection capability compatible with common transceivers providing an indication of a wake up pattern at the RXD pin.

The STB pin is a programmable open-drain pin which can be either actively pull high or low, depending on the logic level required by the transceiver. This pin is used to control the state of the transceiver. In active mode, it is actively pulled high (or low, depending on the FTP setting) to keep the transceiver in active state. In standby mode, it is in high impedance state, so the STB pin level is defined by external pull-up (pull-down) resistor, to keep the transceiver in standby mode. The STB pin is activated automatically upon wake-up pattern detection at the RX pin, to set the transceiver in active mode.

The external transceiver, as well as LDLL16EN's V_IO pins, are supplied from external 5 V voltage regulator. Since this 5 V supply is also required in standby mode, it is important to choose a voltage regulator with low quiescent current, as it contributes to the total standby current of the entire module.

Two main constraints should be considered for transceiver choice:

1. Wake up (WUP) propagation in Standby, to allow wakeup decoding by CAN Handler IP
2. WUP filtering based preferably on CAN standard ISO 11898-2 Tshort filtering time (max 1.8us) because Tlong filtering time (max 5us) could block completely CANFD Light WUP frame propagation, based on 5us dominant/recessive pulses.

5.2 CAN FD light compatible network protocol

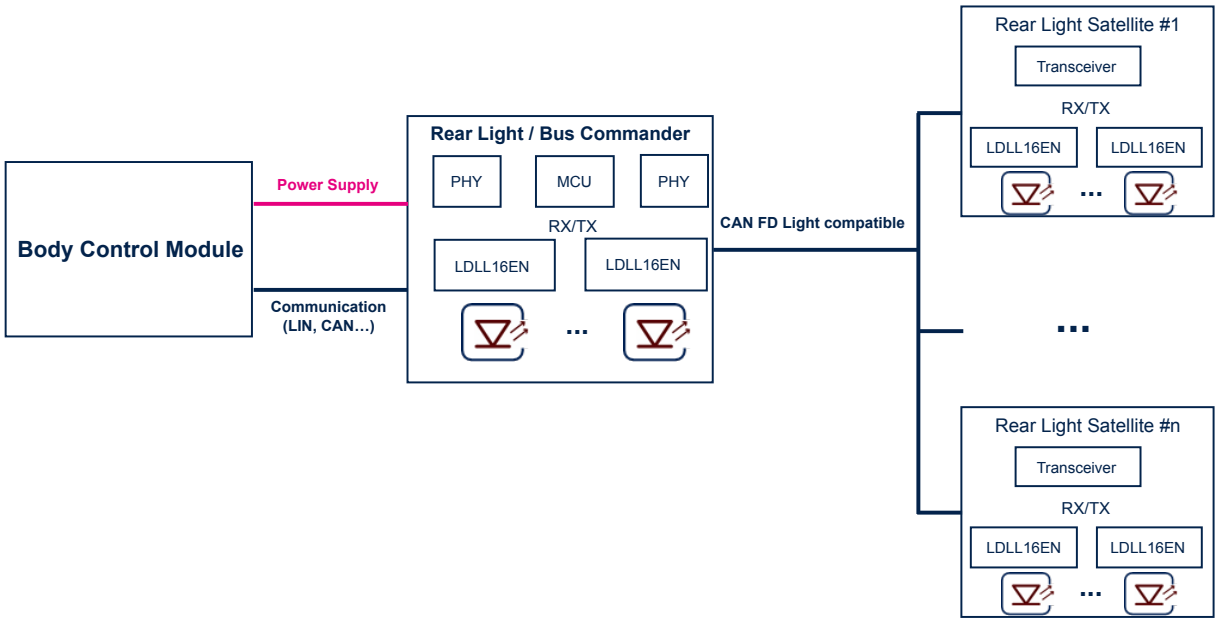
The LDLL16EN features a serial CAN FD light compatible interface, a robust commander-responder communication bus

It can uses CAN FD physical interface, therefore differential bus wiring, and a protocol implemented by a CAN FD protocol controller. It guarantees a defined edge density for synchronization and, for safety, CRC and error checking are provided.

The system overview is shown in the Figure 18. The communication commander is implemented in the rear LED ECU using the protocol controller in the µC and a CAN FD transceiver. An additional transceiver (for example LIN, high speed CAN or others) may be used by the ECU to communicate with other ECUs in the car. The communication responders are located in the LED satellites.

The communication commander is implemented in the rear LED ECU using the protocol controller in the µC and a CAN FD transceiver. An additional transceiver (for example LIN, high-speed CAN or other) may be used by the ECU to communicate with other ECUs in the car. The communication responders are located in the LED satellites.

Figure 18. System overview



5.3 Protocol overview

5.3.1 Basic overview

The CAN FD light compatible network is a bus system on which all participants share the same differential wires. Messages being sent by one participant are received by all others. Its protocol uses a commander-responder scheme. The commander is implemented in the host ECU while the responders are built in the LED drivers.

The responders only answer upon request by the commander, therefore no collision resolving mechanisms are needed.

Two basic message types are used: broadcast messages and unicast messages.

A broadcast message is sent to the responders and expects no answer from them. The responders on the bus pick the data relevant for them from the message.

A unicast message is addressed to a specific responder that answers by sending the requested data.

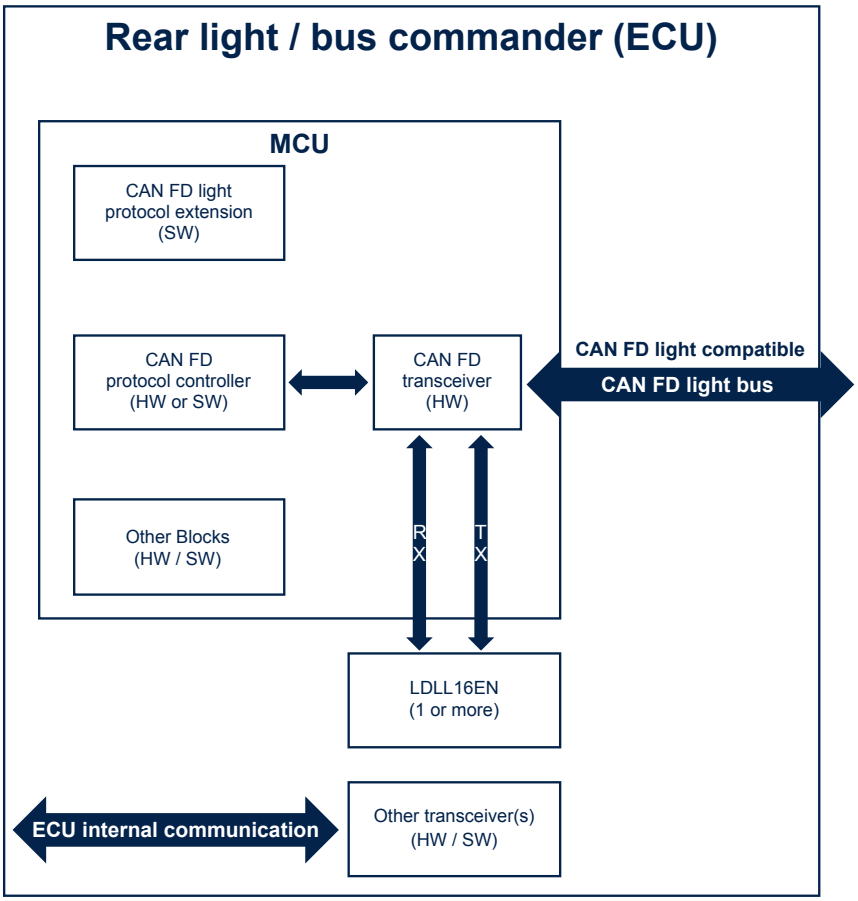
A specific unicast message can be sent in predefined intervals to serve a watchdog triggering. The unicast message can expect an answer from the addressed responder within a given time frame. Both mechanisms can be used to implement an efficient supervision scheme, which allows the detection of a disconnected or failed network participant.

5.3.2 Commander

The Figure 19 shows the block diagram of the commander as referred in the Figure 18. The protocol commander uses a standard CAN FD protocol controller that may be already implemented in the automotive microcontroller in hardware or software. An additional CAN FD protocol extension software controls this protocol controller to make it act as CAN FD light compatible commander and implements the commander side of the CAN FD light compatible protocol.

To access the physical interface of the CAN FD network a standard CAN FD transceiver is used.

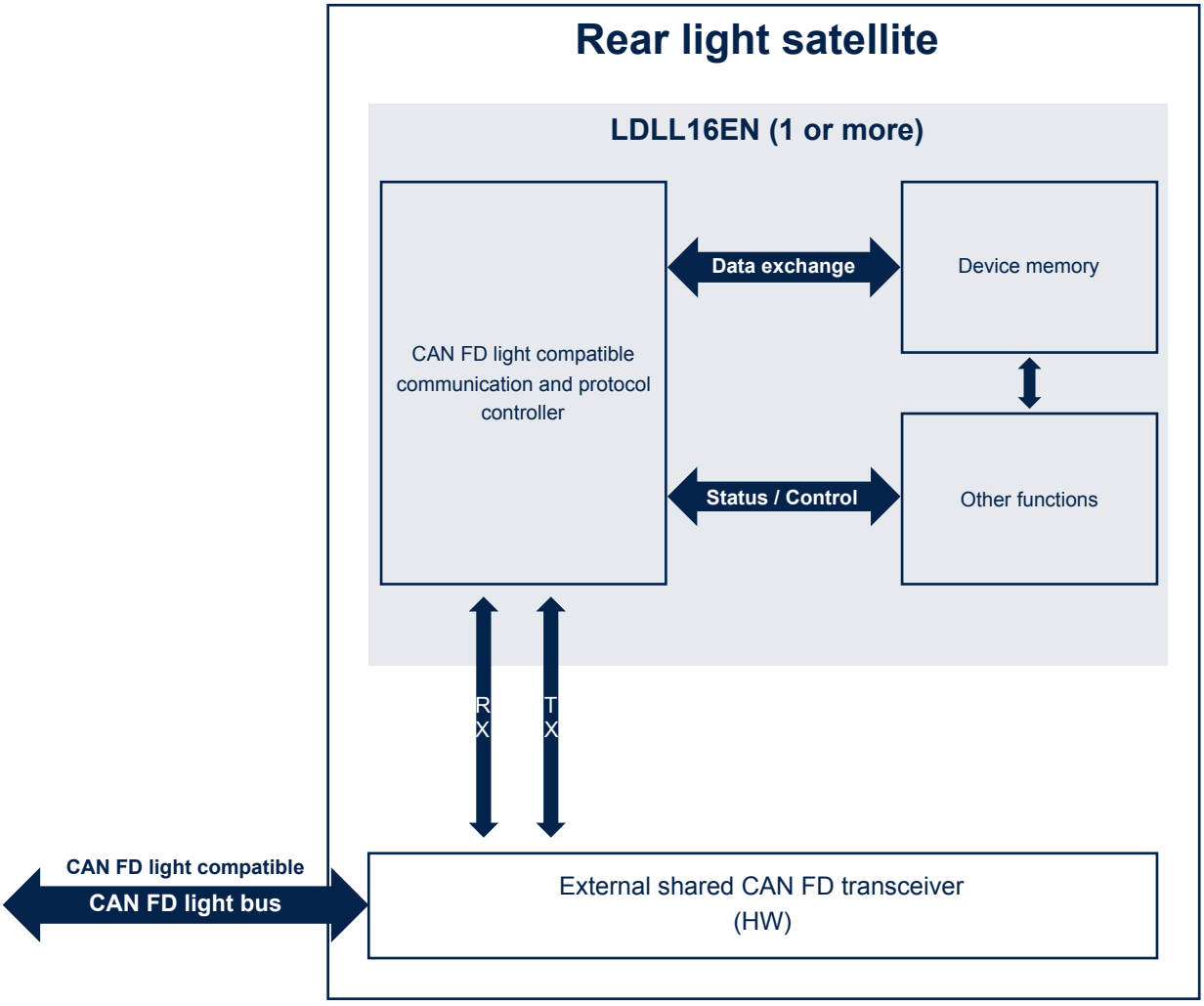
Figure 19. Commander block diagram



5.3.3 Responder

The CAN FD light compatible responder is located in the satellites (see the Figure 18) and inside the LDLL16EN LED controller device (see the Figure 20).

Figure 20. Responder ECU controller device

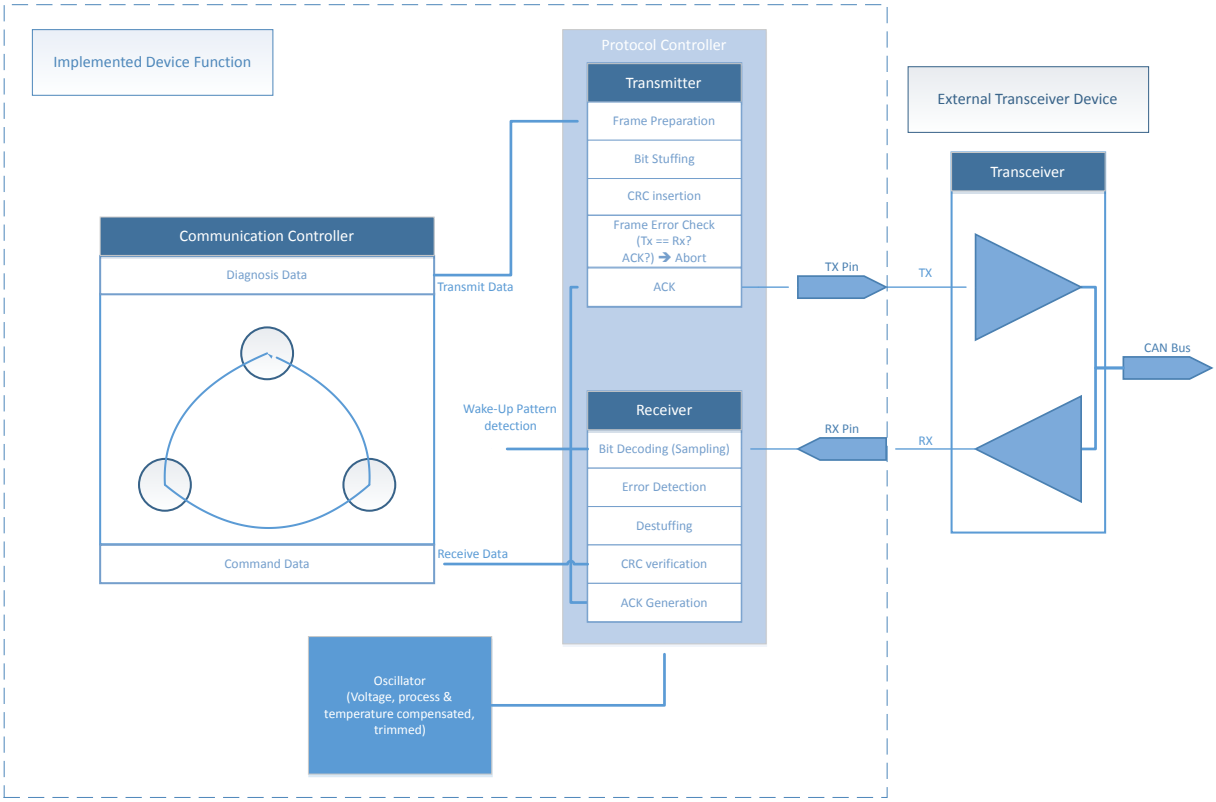


The implementation is done entirely in hardware. It consists of two parts shown in the Figure 21:

- A CAN FD light compatible protocol controller with an accurate oscillator for generating and sampling the data bits.
- A communication protocol controller that sends and receives data to and from the protocol controller and controls the communication.

Each responder has its own 9-bit wide ID.

Figure 21. CAN FD light compatible communication and protocol controller



5.4 Data link layer

The LDLL16EN supports data exchange at a bit rate of 1Mb/s.

The communication is checked for safety reasons: a CRC value is sent with each data frame, supporting ASIL B requirements.

After every frame all recipients send an acknowledge bit so at least one is received by the sender so it can detect if it is still connected to the network.

Since all participants of the network are connected to the same wire, a transmitter is able to detect if it is not correctly operating, consequently entering passive state not to disturb the bus communication.

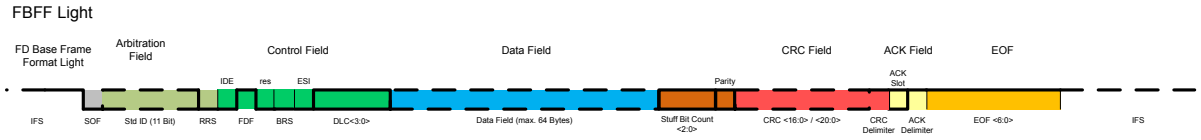
The data sampling clock is generated in each receiver individually, therefore a minimum edge density of the data stream is guaranteed such that at least every 10th bit a recessive to dominant edge is present so a synchronization of the receiver to the data stream is possible.

Also a wake up over the network is implemented.

5.4.1 CAN FD light compatible frame format

The CAN FD base format is used for the CAN FD light compatible protocol without extended ID implemented as shown in the Figure 22.

Figure 22. CAN FD Base Frame Format (FBFF)



The bits in the control field are fixed: FD frame (FDF) is always recessive. Not supported are extended ID (EID, IDE bit always dominant), bit rate switch (BRS, always dominant) and error state indication (ESI, always dominant).

The data field can be up to 64 bytes long, the number of bytes is encoded in the data length code (DLC) field. Depending on the number of data bytes either CRC17 or CRC21 is calculated. Only one CRC delimiter bit is sent and accepted since the data bit rate is the same as the arbitration bit rate.

The arbitration and data bit rate are both 1 Mb/s. The bit rate is not switched.

5.4.2 Wake up

The responders support a power down mode out of which they can be woken up by the wake-up frame shown in the Table 10.

5.4.3 Error frames

No error frames are sent by the responders. Error frames may be sent by the commander but are ignored by the responders.

5.4.4 Collisions

Since the communication is always controlled and initiated by the commander, the bus participants do not arbitrate. Collisions lead to data frame errors.

5.4.5 Error handling

Network participant disconnect

Since all participants share the same bus, various mechanisms allow the detection of a disconnected device.

After each sent frame at least one acknowledge is expected from a receiver. If this acknowledge is not received it can be assumed that the sender is not connected to the network.

Broadcast frames can be transmitted within a given interval. Responders not receiving a broadcast frame after a defined time may have lost their connection to the commander.

The commander may expect an answer from the addressed responder after having sent a diagnosis request within a given time frame. If the answer is not received the communication with the addressed responder may have been lost.

Sender bus block

The responders check the bus for permanent recessive or dominant states. Both states indicate a bus block and the sender may not be able to transmit any messages.

Frame errors

Each received frame is verified in regard to these features:

- CRC: the correctness of the received CRC for each frame is checked
- CRC Delimiter: after the CRC, one recessive bit as CRC delimiter has to be received
- Bit Stuffing: The correct position of the stuff bits is checked

The checks permanent dominant and permanent recessive are made by the external transceiver.

Invalid messages are not resent.

Error recovery: upon reception of a valid unicast frame, the transceiver transmitter is enabled again.

5.5 Data handling

5.5.1 Overview

As described in the Section 5.3: Protocol overview, two basic message types are used: broadcast messages, addressed to all responders without any responder answer; unicast messages, addressed to an individual responder followed by responder feedback. The responder ID is 9 bits wide.

In case of "Unicast communication" (see the Section 5.7: Unicast frames), a commander can access all device registers using a CAN ID equal to a responder ID0, while the ID of the responder answer is always equal to (responder ID0 | 0x200). A specific protocol is embedded into the data of the unicast frames to specify register address and type of operation (read/write/clear). In case of "Broadcast communication" (see the Section 5.6: Broadcast frames), a commander can send a CAN FD frame with 64 data bytes to several responders. Each broadcast data frame has a specific chain ID (bits 0-5 of CAN ID field, see the Section 5.6.3: Chain initialization) which allows to distinguish between 64 different groups of responders.

Each responder assigned to this chain ID group can pick 16 data bytes from this frame (data position is configurable) and update all duty cycle or current values registers accordingly. The selection between duty cycle or current value update is done by bit 6 of CAN ID field. The Chain ID and data position of each responder is configurable using broadcast initialization frame.

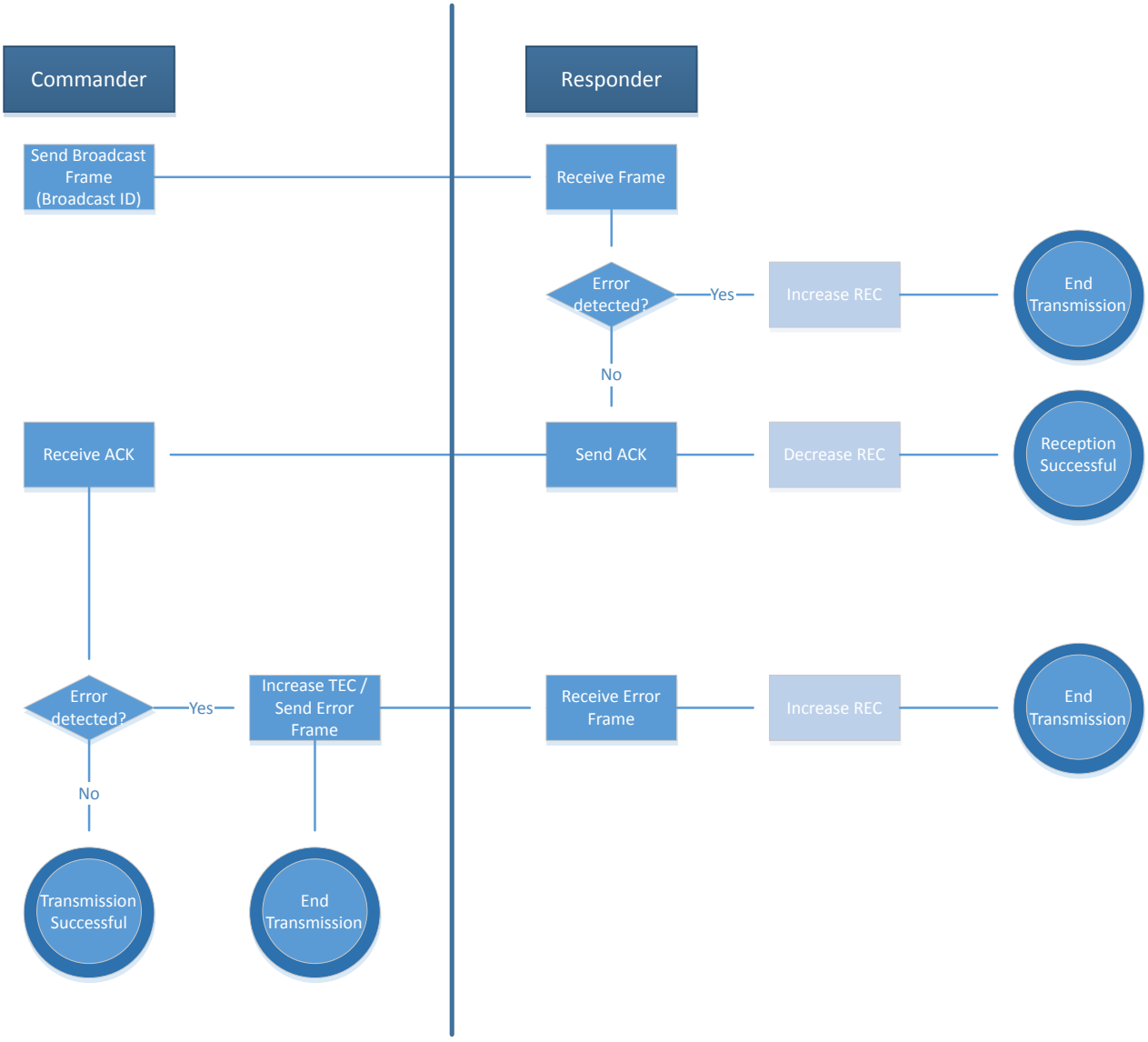
5.6 Broadcast frames

5.6.1 Frame format

Broadcast frames are transmitted to all responders in the network. The broadcast frame contains in its ID the number of the chain that is addressed. Each responder belonging to this chain picks its data from the maximum 64 bytes transferred by this frame. Each LDLL16EN device can pick 16 bytes of data. The position from where it picks the data is defined during Chain Initialization.

The Figure 23 shows the communication flow of a broadcast frame.

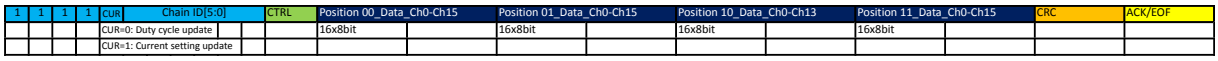
Figure 23. Broadcast message flow



5.6.2 Broadcast frame for current setting and PWM duty cycle setting

As shown in the Figure 24, a broadcast frame uses the ID starting with '1' followed by three '1's and the chain number. Bit 6 "CUR" defines whether the data contains PWM duty cycle data (0) or current setting data (1). The six-bit chain number allows the assignment of 64 chains with up to four responders consisting of 16-channel entities each.

Figure 24. Broadcast frame



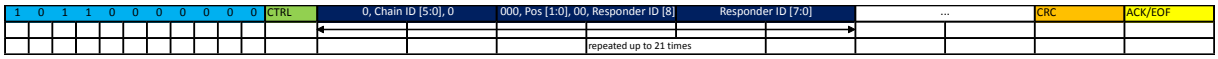
In each 16-byte data package data for Ch15, respectively the highest channel number, is the MSB, data for Ch0, respectively the lowest channel number, is the LSB.

This broadcast frame is ignored by the responder as long as its reset bit RSTB is not cleared.

5.6.3 Chain initialization

A specific broadcast frame is sent to all responders to inform them about the chain they belong to and their position within this chain, so each responder is able to grab data intended for it.

Figure 25. Broadcast chain initialization



The ID for this chain initialization frame is "1_0110_0000000". For every responder three bytes are used to identify the chain it belongs to, its position and the addressed responder with the following data structure for each responder:

- MSB: 0, chain ID[5:0], 0
- Next byte: 000, Pos[1:0], 00, responder ID[8]
- LSB: responder ID[7:0]
- Position 00: responder picks data bytes 0-15
- Position 01: responder picks data bytes 16-31
- Position 10: responder picks data bytes 32-47
- Position 11: responder picks data bytes 48-63

Note: If a device has several responder IDs (that is a 32-channel device has two responder IDs), those responder IDs must be assigned to different chain IDs.

Responder IDs of the same device cannot be initialized in a single broadcast frame.

As reported in Figure 34, it is possible to initialize up to 21 responders within one chain initialization broadcast frame.

Chain initialization is executed on the responder, even if its reset bit RSTB is set. Chain initialization does not clear reset bit RSTB.

5.6.4 Go to sleep/wake up pattern

For sending the network to sleep and waking it up again a dedicated ID is defined.

The reserved WUP ID is "1_000_011_1100". A frame with this ID and without data (DLC = 0) is the command to send all responders into sleep/standby mode. This is shown in the Figure 26.

Figure 26. Send-To-Sleep command

For waking up all the responders, in the network the data in the payload satisfy the wake-up pattern requirements of ISO11898-2 with t_{CAN_FILTER} (short) at 1 Mb/s.

This wake up pattern is repeated in the eight data bytes of the frame shown in the Table 10. The responders recognize the dominant-recessive-dominant pulse in which the three individual pulses are longer than the specified filter time. These pulses are contained in the data field.

If the frame does not contain any data, it serves as “Go-To-Sleep”-command for all responders in the network. If it contains at least one data byte, it acts as a wake-up pattern for all responders.

Table 10. Wake up pattern (WUP) frame

ID	CTRL	DLC	DATA BYTE 1	DATA BYTE 2-8
"1_000_011_1100"	"001000"	1000	1111_1110	0000_1111

In conclusion:

ID = "1_000_011_1100" and DLC = 0 → send-to-sleep command

ID = "1_000_011_1100" and DLC ≠ 0 → wake-up pattern frame

5.6.5 Synchronization frame

The synchronization frame must be sent by the commander after each responder reply, but only if the addressed devices change in the next commander frame.

Due to the frequency offset between the responding responder and the commander, some other responders may not be able to receive frames sent by the commander correctly after a responder reply. Therefore, the frame in the Figure 27 has to be sent by the commander to ensure the correct synchronization of all responders to the commander. The responders synchronize on this frame but drop the content because it does not contain an ID that the responders recognize.

Figure 27. Synchronization frame

Table 11. Synchronization frame

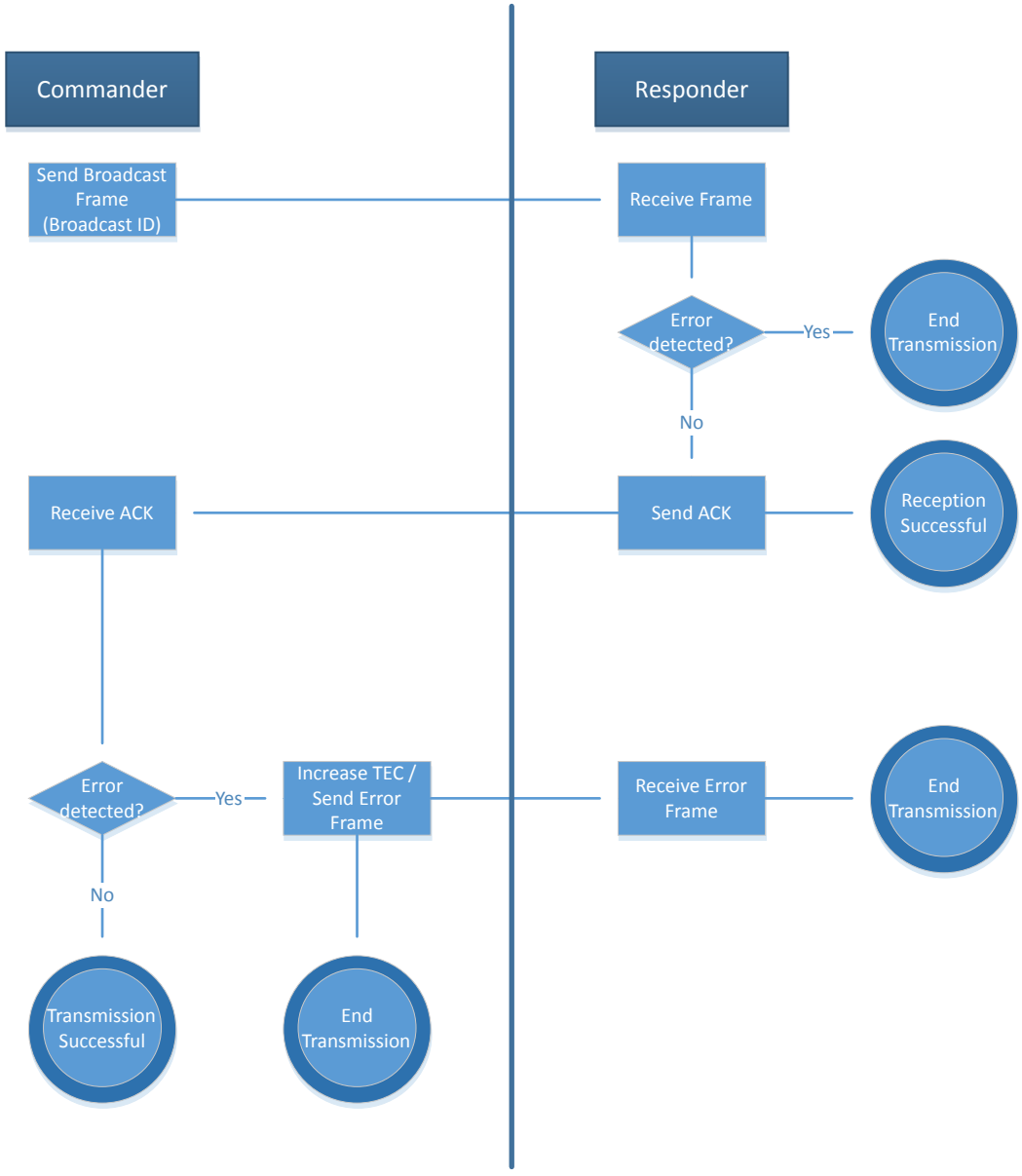
ID	CTRL	DLC
"1_010_101_0101"	"001000"	0000

5.7 Unicast frames

5.7.1 Unicast request frame

The commander may request an action from a particular responder by sending a unicast request frame, which uses the responder ID in the CAN FD ID field preceded by "0" to distinguish the commander request from the responder reply. The MSB of all CAN FD IDs used for unicast frames in the network is "0" to distinguish between unicast and broadcast frames.

Figure 28. Unicast request communication between commander and responders



In case the unicast frame contains data, the first data byte contains OP code (bits 7-6) and register address (bits 5-0). The operation code represents the instruction to be performed; while the following 6 bits represent the address on which the operation will be performed.

The next four data bytes contain the optional data.

Table 12. Unicast frame data - operating code and register address

	Command byte (8-bit)							
	Operating code		Address					
Bit	7	6	5	4	3	2	1	0
Name	OC1	OC0	A5	A4	A3	A2	A1	A0

The operation code is used to distinguish among different accesses modes to the registers of the responder device.

Table 13. Unicast frame data - registers access mode

Bit 7 - OC1	Bit 6 - OC0	Meaning
0	0	<Write Mode>
0	1	<Read Mode>
1	0	<Read and Clear Mode>
1	1	<Read Device Information>

A write operation leads to a modification of the addressed data by the payload if a write access is allowed (for example control register, valid data).

A read operation instructs the responder to answer with a frame containing a global status byte and the data present in the addressed register at communication start. Read operation instructions executed on specific addresses initiate the responder to reply with a frame containing data present in the addressed register and the three subsequent registers. This command is called burst read. In any case, the payload data of the commander request will be ignored and internal data will not be modified.

A read and clear operation will instruct the responder to reply with a frame containing a global status byte and the data present in the addressed register after the execution of the clear command. Furthermore, a read and clear operation leads to a clearance of the addressed register status bits. The bits to be cleared are defined firstly by address and secondly by the payload bits set to "1".

A read device information operation accesses the ROM device data (see ROM memory map).

Besides write, read, read and clear, there are two advanced operation codes. Both of them can be used to clear all status registers, while one can be used to set all control registers to their default value.

A "set all control registers to default" and "clear all status registers" command is performed when an OpCode "11" at address b'111111 is performed. A "clear all status registers" command is performed when an OpCode '10' at address b'111111 is performed.

The payload is the data transferred to the responder device with every unicast communication. The payload always follows the OpCode and the address bits.

For write access the payload represents the new data written to the address registers.

For read operation the payload is not used. For functional safety reasons it is recommended to set the unused payload to "0".

For read and clear operation, the payload indicates the clearance of specific bits in the status register. The bits to be cleared are defined firstly by address and secondly by the payload bits set to "1".

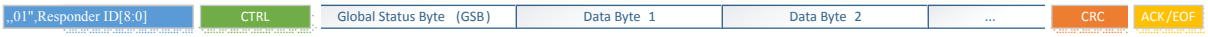
Figure 29. Unicast diagnosis request frame

As shown in the Figure 29, the commander addresses a responder by its "Responder ID" in CAN FD ID.

5.7.2 Unicast response frame

The responders answer with a diagnosis response frame to the commander's diagnosis request frame (see the Figure 30). The CAN FD frame ID is the responder ID preceded by "01" to distinguish the responder reply from the commander request. The commander must send a synchronization frame, according to the Section 5.6.5: Synchronization frame, after each responder reply (but only if the addressed devices change in the next commander frame), to ensure the responders are synchronized to the commander and the frames sent by the commander are correctly received by all responders.

Figure 30. Unicast diagnosis response frame



5.7.3 Global status byte (GSB)

Table 14. Global status byte

	Bit							
	7	6	5	4	3	2	1	0
Name	GSBN	RSTB	x	FE2	FE1	DE	GW	FS

The global status byte is described here below.

Table 15. Global status byte field description

Bit #	Name	Description
7	GSBN	Global status bit not This bit is a NOR combination of the remaining bits of this register: RSTB nor FE2 nor FE1 nor DE nor GW nor FS
6	RSTB	Reset bit The RSTB indicates a device reset. In case this bit is set, all internal RAM control and configuration registers are set to default and kept in that state until the bit is cleared. Any valid unicast frame requiring GSB in the response frame clears the reset bit after the responder sent its response frame. No data can be written to RAM configuration and control registers as long as the reset bit is set. Chain initialization command is executed, but reset bit not cleared
5	x	Not used 0
4	FE2	Functional error 2 The FE2 indicates the logical OR combination of the following errors: Any output channel exceeding the LED short circuit threshold (when enabled): SHT_CHx, or Any output channel in open-load: OL_CHx, or Any output channel in short circuit with preregulator: OUT_SHT_VPREG_CHx
3	FE1	Functional error 1 The FE1 reports the following error: Thermal shutdown: TSD
2	DE	Device error The DE indicates the logical OR combination of the following errors: Short circuit on external NTC: NTC_FAULT, or Power good threshold not reached: PG_NOT_VP_REG, or Supply undervoltage fault: VS_UV, or Open or short circuit fault on DAC reference resistor: RDAC_FAULT
1	GW	Global warning The GW is a logical OR combination of warning flags: Thermal warning: TW, or NTC derating active: NTC_DER_ACT
0	FS	Fail-safe: The fail-safe bit is set, when the device operates in fail-safe/stand-alone mode

The subsequent data bytes are the data transferred from the responder device with every communication to the commander.

5.7.4 Unicast frame - no data

If the unicast frame does not contain any data the addressed responder transmits the global status byte.

Figure 31. Unicast frame w/o data - commander request and responder answer

	ID field bits															
	10	9	8	7	6	5	4	3	2	1	0					
Commander request =	0	0	Responder ID[8:0]									CTRL	CRC		ACK/EOF	
Responder answer =	0	1	Responder ID[8:0]									CTRL	GSB		CRC	ACK/EOF

5.7.5 Unicast frame - single RAM read

The data frame comprises 5 bytes. The MSB of the commander request data frame contains the OP code and address of the register. The following 4 bytes are "don´t care" data. The responder answer contains the GSB and the register content of the register addressed by the commander at the time of the responder answer communication start. The LDLL16EN registers are arranged with 4 data byte per register (see the Section 6: FTP and RAM memory mapping).

Figure 32. Unicast frame with single RAM read - commander request and responder answer

	ID field bits																	
	10	9	8	7	6	5	4	3	2	1	0		OP Code + Address						
Commander request =	0	0	Responder ID[8:0]									CTRL	"01" + Address	Do not care 3	Do not care 2	Do not care 1	Do not care 0	CRC	ACK/EOF
Responder answer =	0	1	Responder ID[8:0]									CTRL	GSB	Data Byte 3	Data Byte 2	Data Byte 1	Data Byte 0	CRC	ACK/EOF

5.7.6 Unicast frame - single RAM read and clear

The data frame comprises 5 bytes. The MSB of the commander request data frame contains the OP code and address of the register. The following 4 bytes specify the bits of the addressed register to be cleared. Bits to be cleared must be set at "1" in the commander request. The responder answer contains the GSB and the register content of the register addressed by the commander at the time of the responder answer after the execution of the Clear command.

Figure 33. Unicast frame with single RAM read and clear - commander request and responder answer

	ID field bits																	
	10	9	8	7	6	5	4	3	2	1	0		OP Code + Address						
Commander request =	0	0	Responder ID[8:0]									CTRL	"10" + Address	Byte 3: bits to be cleared "1"	Byte 2: bits to be cleared "1"	Byte 1: bits to be cleared "1"	Byte 0: bits to be cleared "1"	CRC	ACK/EOF
Responder answer =	0	1	Responder ID[8:0]									CTRL	GSB	Data Byte 3	Data Byte 2	Data Byte 1	Data Byte 0	CRC	ACK/EOF

5.7.7 Unicast frame - single ROM read

The OP code for this instruction is 11 "Read device information". It is used for internal traceability and testing purposes and is not needed for the application.

5.7.8 Unicast frame - burst read mode RAM register

A burst read mode is supported when a single RAM Read request is executed on a specific RAM address. The RAM addresses eligible to burst read mode are specified in the Section 6: FTP and RAM memory mapping. The responder answers to a valid burst read mode RAM register command with 16 bytes of data. The four most significant data bytes correspond to the data stored in the register addressed by the commander request. The 12 following bytes correspond to the data stored on the next three consecutive addresses.

Therefore, the commander request frame contains five data bytes, while the responder answer frame contains 12 data bytes.

Figure 34. Unicast frame with burst read mode RAM register - commander request and responder answer

	ID field bits																	
	10	9	8	7	6	5	4	3	2	1	0		OP Code + Address (Status Register Addresses eligible for burst read)					
Commander request =	0	0	Responder ID[8:0]									CTRL	"01" + Address	Do not care 3	Do not care 2	Do not care 1	Do not care 0	CRC	ACK/EOF
Responder answer =	0	1	Responder ID[8:0]									CTRL	Data Byte 0	Data Byte 1	Data Byte 2	Data Byte 3	=>		
												=>	Data Byte 4	Data Byte 5	Data Byte 6	Data Byte 7	=>		
												=>	Data Byte 8	Data Byte 9	Data Byte 10	Data Byte 11	=>		
												=>	Data Byte 12	Data Byte 13	Data Byte 14	Data Byte 15	CRC	ACK/EOF	

5.7.9 Unicast frame - single RAM write

The MSB of the commander request data frame contains the OP code and address of the register. The responder answer contains only the GSB.

Figure 35. Unicast frame with single RAM write - commander request and responder answer

	ID field bits																	
	10	9	8	7	6	5	4	3	2	1	0		OP Code + Address					
Commander request =	0	0	Responder ID[8:0]									CTRL	"00" + Address	Data Byte 3	Data Byte 2	Data Byte 1	Data Byte 0	CRC	ACK/EOF
Responder answer =	0	1	Responder ID[8:0]									CTRL	GSB	CRC	ACK/EOF				

Therefore, the commander request frame contains five data bytes, while the responder answer frame contains only one data byte.

5.7.10 Unicast frame - 3x RAM write

This instruction allows to write to three different RAM addresses with one CAN FD frame. Only OP code “00” is allowed in this mode. The commander frame request contains 16 data bytes. The MSB of the commander request data frame contains the OP code and address of the register, followed by four data bytes to be written to the addressed register. Next five data bytes contain again the OP code, address, and data to be written. Next five data bytes contain again the OP code, address, and data to be written. LSB is "Don´t care". This write mode allows therefore a fast programming of configuration registers lowering the bit overhead and bus-load.

The responder answer contains only the GSB.

Figure 36. Unicast frame with 3x RAM write - commander request and responder answer

	ID field bits																		
	10	9	8	7	6	5	4	3	2	1	0		OP Code + Address						
Commander request =	0	0	Responder ID[8:0]									CTRL	"00" + Address	Data Byte 3	Data Byte 2	Data Byte 1	Data Byte 0	=>	
												=>	"00" + Address	Data Byte 3	Data Byte 2	Data Byte 1	Data Byte 0	=>	
												=>	"00" + Address	Data Byte 3	Data Byte 2	Data Byte 1	Data Byte 0	Do not care	CRC	ACK/EOF
Responder answer =	0	1	Responder ID[8:0]									CTRL	GSB	CRC	ACK/EOF				

5.7.11 Unicast CAN FD frame - FTP read

This command allow to read a content of specified FTP address. The commander request frame contains 16 data bytes. The first byte contains the OP code (Ah - FTP read) and 4 bit FTP row address. Next 15 bytes are do not care. The responder answers with 16 data byte frame containing FTP row data. This command is effective only if device is in FTP programming mode. Otherwise, no answer is sent.

Table 16. Unicast CAN FD frame - FTP read

	ID field bits															
	10	9	8	7	6	5	4	3	2	1	0		OP Code + Address					
Commander request =>	0	0	Responder ID[8:0]									CTRL	"1010" + FTP Row Addr.	Do not care 14	Do not care 13	Do not care 12	=>	
												=>	Do not care 11	Do not care 10	Do not care 9	Do not care 8	=>	
												=>	Do not care 7	Do not care 6	Do not care 5	Do not care 4	=>	
												=>	Do not care 3	Do not care 2	Do not care 1	Do not care 0	CRC	ACK/ EOF
Responder answer =>	0	1	Responder ID[8:0]									CTRL	Do not care	Data Byte 14	Data Byte 13	Data Byte 12	=>	
												=>	Data Byte 11	Data Byte 10	Data Byte 9	Data Byte 8	=>	
												=>	Data Byte 7	Data Byte 6	Data Byte 5	Data Byte 4	=>	
												=>	Data Byte 3	Data Byte 2	Data Byte 1	Data Byte 0	CRC	ACK/ EOF

5.7.12 Unicast CAN FD frame - FTP write

This command is used to write data in specified FTP address. The commander request frame contains 16 data bytes. The first byte contains the OP code (Bh - FTP write) and 4 bit FTP row address. Next 15 bytes are FTP data. The FTP write operation is performed within TFTT_WR time. During this time, no commands should be sent on the CAN bus. The FTP write command is effective only if device is in FTP programming mode.

Table 17. Unicast CAN FD frame - FTP write

	ID field bits																
	10	9	8	7	6	5	4	3	2	1	0		OP Code + Address				
Commander request =>	0	0	Responder ID[8:0]									CTRL	"1011" + FTP Row Addr.	Data Byte 14	Data Byte 13	Data Byte 12	=>
												=>	Data Byte 11	Data Byte 10	Data Byte 9	Data Byte 8	=>
												=>	Data Byte 7	Data Byte 6	Data Byte 5	Data Byte 4	=>
												=>	Data Byte 3	Data Byte 2	Data Byte 1	Data Byte 0	CRC	ACK/EOF

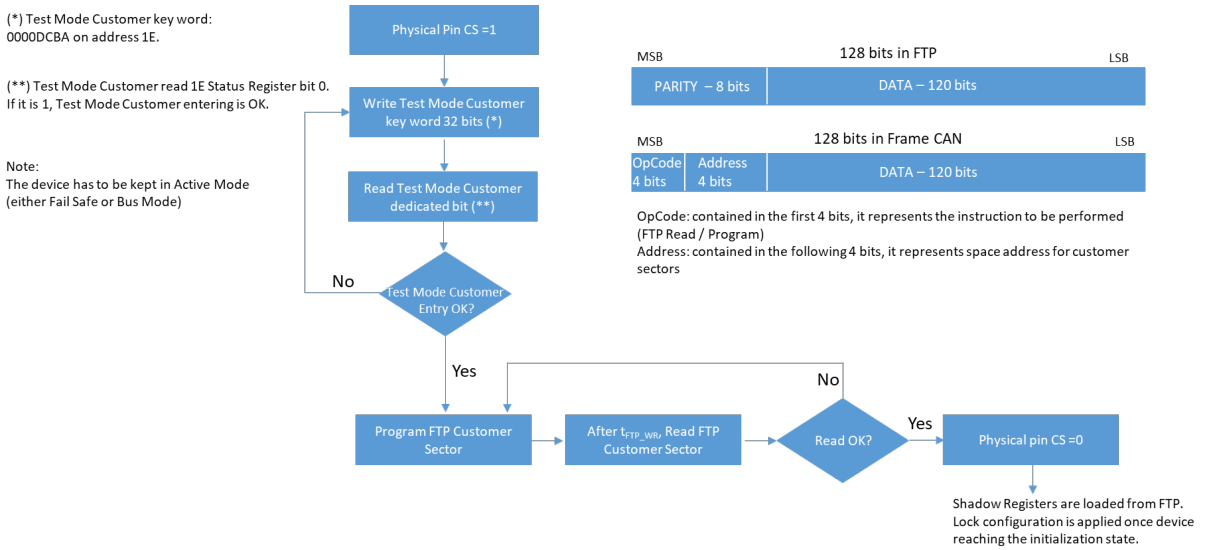
6 FTP and RAM memory mapping

The LDLL16EN is equipped with a 2-kbit EEPROM, used also to store device configuration data. Part of this memory shall be managed by the customer.

The device can operate in standalone mode (no microcontroller used) thanks to full configurability by few time programmable (FTPs) memory registers. In application, the FTPs can be programmed (up to N_{FTP} cycles) via the CAN FD light compatible interface, even if the device does not integrate any counter taking note about the FTP writing cycles. By the way, for safety reason, any FTP sector can be locked to avoid unintentional writing.

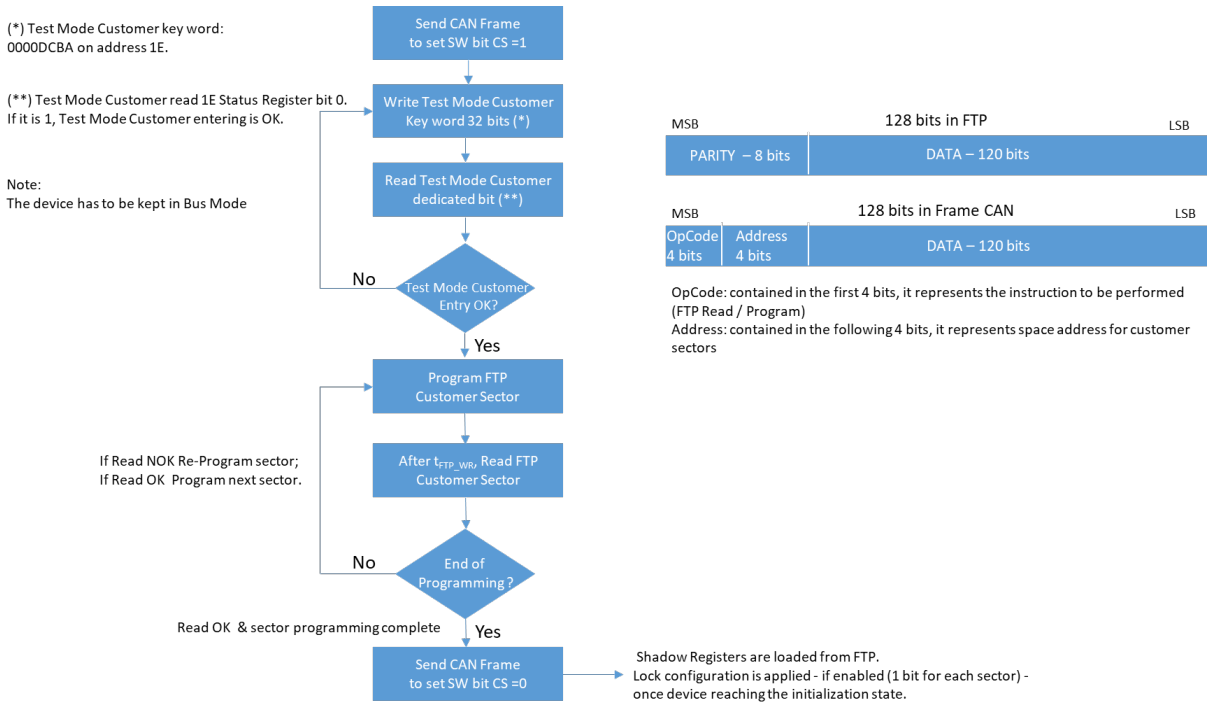
The user can program FTPs setting the CS pin to "1" via HW or via SW.

Figure 37. FTP access through CAN bus - programming by physical pin CS



OpCode: FTP Read = Ah, FTP Write = Bh

Figure 38. FTP access through CAN bus - programming by setting SW bit CS



OpCode: FTP Read = Ah, FTP Write = Bh
Besides FTP memory, the device is also equipped with a RAM memory type.
Here below the memory mapping is reported.

Table 18. RAM memory map

Address	Name	Access	Content
Configuration and control			
00h			Reserved
01h	PWM_DUTY_ALL	Read/Write	Linear 8 bit global PWM duty cycle
02h	PWM_DUTY_CH0_3	Read/Write/Broadcast write	Exponential 8 bit individual PWM duty cycle channel 0-3
03h	PWM_DUTY_CH4_7	Read/Write/Broadcast write	Exponential 8 bit individual PWM duty cycle channel 4-7
04h	PWM_DUTY_CH8_11	Read/Write/Broadcast write	Exponential 8 bit individual PWM duty cycle channel 8-11
05h	PWM_DUTY_CH12_15	Read/Write/Broadcast write	Exponential 8 bit individual PWM duty cycle channel 12-15
06h			Reserved
07h			Reserved
08h			Reserved
09h			Reserved
0Ah	CUR_SET_CH0_3	Read/Write/Broadcast write	8 bit analog current setting channel 0-3
0Bh	CUR_SET_CH4_7	Read/Write/Broadcast write	8 bit analog current setting channel 4-7
0Ch	CUR_SET_CH8_11	Read/Write/Broadcast write	8 bit analog current setting channel 8-11
0Dh	CUR_SET_CH12_15	Read/Write/Broadcast write	8 bit analog current setting channel 12-15
0Eh			Reserved
0Fh			Reserved
10h			Reserved
11h			Reserved
12h	DIN_MAP_CH0_15	Read/Write	Direct input mapping channel 0-15
13h			Reserved
14h			Reserved
15h	CONFIG_1	Read/Write	Device configuration register 1
16h	CONFIG_2	Read/Write	Device configuration register 2
17h	CONFIG_3	Read/Write	Device configuration register 3
18h	CONFIG_4	Read/Write	Device configuration register 4
19h	WD_TRIG	Read/Write	Watchdog trigger
Status			
1Ah	Chain_IDPOS	Read	ChainID and position number responder ID0
1Bh			Reserved
1Ch			Reserved
1Dh			Reserved
1Eh	CAN_FTP	Read	Bit indicating FTP programming mode status

Address	Name	Access		Content
1Fh	VLED_ON_CH0_3	Burst read from address 1Fh		8-bit output on-state voltage channel 0-3
20h	VLED_ON_CH4_7		Read	8-bit output on-state voltage channel 4-7
21h	VLED_ON_CH8_11		Read	8-bit output on-state voltage channel 8-11
22h	VLED_ON_CH12_15		Read	8-bit output on-state voltage channel 12-15
23h				Reserved
24h				Reserved
25h				Reserved
26h				Reserved
27h	OUT_STATUS_CH0_15	Burst read from address 27h		Output status bit channel 0-15
28h	SHT_CH0_15		Read/Read &Clear	Short circuit detection flag channel 0-15
29h	OL_CH0_15		Read/Read &Clear	Open-load detection flag channel 0-15
2Ah	OUT_SHT_VPREG_CH 0_15		Read/Read &Clear	Output shorted to VPREG detection flag channel 0-15
2Bh	VLEDON_RFR_CH0_15	Read		VLED_ON refresh information bit channel 0-15
2Ch	STATUS_1	Burst read from address 2Ch		Device status register 1, ADC voltage on VS, VPRE_REG_A, VPRE_REG_B, T_J
2Dh	STATUS_2		Read	Device status register 2, ADC voltage on NTC, channel lowest output voltage corresponding to VPRE_REG_A and VPRE_REG_B
2Eh	STATUS_3		Read/Read &Clear	Device status register 3, various status bits
2Fh	FTP_STATUS_1		Read	Device FTP status 1, read only status of various FTP configuration bits
30h	FTP_STATUS_2	Read		Device FTP status 2, read only status of FTP configuration fail-safe output permanent enable channel 0-15
34h	FTP_PARITY_ERROR	Read		16 parity error bits - 1 bit per FTP Row (0 = ok, 1 = error)
Reserved				
31h-3Fh (except 34h)				Reserved for ST testing and trimming

6.1 Registers description

6.1.1 Channel PWM duty cycle

Channel PWM duty cycle 0x01h register

Address 01h

Access R/W

Data Byte 3								Data Byte 2								Data Byte 1								Data Byte 0							
bit 31	bit 30	bit 29	bit 28	bit 27	bit 26	bit 25	bit 24	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
-																-								PWM_DUTY_ALL							

Table 19. Channel PWM duty cycle 0x01h field description

Bit	Name	Default	Description
31-16	-	0000h	Not used
15-8	-	0h	Not used
7-0	PWM_DUTY_ALL	FTP	Linear Global PWM dimming for outputs mapped to DIN adjustable in 1/256 steps 00h: 0.0% 7Fh: 49.8% FFh: 100%

Channel PWM duty cycle 0x02h register

Address 02h

Access R/W/BW

Data Byte 3								Data Byte 2								Data Byte 1								Data Byte 0							
bit 31	bit 30	bit 29	bit 28	bit 27	bit 26	bit 25	bit 24	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
PWM_DUTY_CH3								PWM_DUTY_CH2								PWM_DUTY_CH1								PWM_DUTY_CH0							

Table 20. Channel PWM duty cycle 0x02h field description

Bit	Name	Default	Description
31-24	PWM_DUTY_CH3	00h	Exponential individual PWM dimming for channel 3 according to law embedded in the Figure 9 00h: 0% - channel off 01h: 0.10% 7Fh: 3.09% FFh: 100% - channel on in DC
23-16	PWM_DUTY_CH2	00h	Exponential individual PWM dimming for channel 2 according to law embedded in the Figure 9 00h: 0% - channel off 01h: 0.10% 7Fh: 3.09%

Bit	Name	Default	Description
			FFh: 100% - channel on in DC
15-8	PWM_DUTY_CH1	00h	Exponential individual PWM dimming for channel 1 according to law embedded in the Figure 9 00h: 0% - channel off 01h: 0.10% 7Fh: 3.09% FFh: 100% - channel on in DC
7-0	PWM_DUTY_CH0	00h	Exponential individual PWM dimming for channel 0 according to law embedded in the Figure 9 00h: 0% - channel off 01h: 0.10% 7Fh: 3.09% FFh: 100% - channel on in DC

Channel PWM duty cycle 0x03h register

Address 03h

Access R/W/BW

Data Byte 3								Data Byte 2								Data Byte 1								Data Byte 0							
bit 31	bit 30	bit 29	bit 28	bit 27	bit 26	bit 25	bit 24	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
PWM_DUTY_CH7								PWM_DUTY_CH6								PWM_DUTY_CH5								PWM_DUTY_CH4							

Table 21. **Channel PWM duty cycle 0x03h field description**

Bit	Name	Default	Description
31-24	PWM_DUTY_CH7	00h	Exponential individual PWM dimming for channel 7 according to law embedded in the Figure 9 00h: 0% - channel off 01h: 0.10% 7Fh: 3.09% FFh: 100% - channel on in DC
23-16	PWM_DUTY_CH6	00h	Exponential individual PWM dimming for channel 6 according to law embedded in the Figure 9 00h: 0% - channel off 01h: 0.10% 7Fh: 3.09% FFh: 100% - channel on in DC
15-8	PWM_DUTY_CH5	00h	Exponential individual PWM dimming for channel 5 according to law embedded in the Figure 9 00h: 0% - channel off 01h: 0.10% 7Fh: 3.09% FFh: 100% - channel on in DC
7-0	PWM_DUTY_CH4	00h	Exponential individual PWM dimming for channel 4 according to law embedded in the Figure 9

Bit	Name	Default	Description
			00h: 0% - channel off 01h: 0.10% 7Fh: 3.09% FFh: 100% - channel on in DC

Channel PWM duty cycle 0x04h register

Address 04h

Access R/W/BW

Data Byte 3								Data Byte 2								Data Byte 1								Data Byte 0							
bit 31	bit 30	bit 29	bit 28	bit 27	bit 26	bit 25	bit 24	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
PWM_DUTY_CH11								PWM_DUTY_CH10								PWM_DUTY_CH9								PWM_DUTY_CH8							

Table 22. Channel PWM duty cycle 0x04h field description

Bit	Name	Default	Description
31-24	PWM_DUTY_CH11	00h	Exponential individual PWM dimming for channel 11 according to law embedded in the Figure 9 00h: 0% - channel off 01h: 0.10% 7Fh: 3.09% FFh: 100% - channel on in DC
23-16	PWM_DUTY_CH10	00h	Exponential individual PWM dimming for channel 10 according to law embedded in the Figure 9 00h: 0% - channel off 01h: 0.10% 7Fh: 3.09% FFh: 100% - channel on in DC
15-8	PWM_DUTY_CH9	00h	Exponential individual PWM dimming for channel 9 according to law embedded in the Figure 9 00h: 0% - channel off 01h: 0.10% 7Fh: 3.09% FFh: 100% - channel on in DC
7-0	PWM_DUTY_CH8	00h	Exponential individual PWM dimming for channel 8 according to law embedded in the Figure 9 00h: 0% - channel off 01h: 0.10% 7Fh: 3.09% FFh: 100% - channel on in DC

Channel PWM duty cycle 0x05h register

Address 05h

Access R/W/BW

Data Byte 3								Data Byte 2								Data Byte 1								Data Byte 0							
bit 31	bit 30	bit 29	bit 28	bit 27	bit 26	bit 25	bit 24	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
PWM_DUTY_CH15								PWM_DUTY_CH14								PWM_DUTY_CH13								PWM_DUTY_CH12							

Table 23. Channel PWM duty cycle 0x05h field description

Bit	Name	Default	Description
31-24	PWM_DUTY_CH15	00h	Exponential individual PWM dimming for channel 15 according to law embedded in the Figure 9 00h: 0% - channel off 01h: 0.10% 7Fh: 3.09% FFh: 100% - channel on in DC
23-16	PWM_DUTY_CH14	00h	Exponential individual PWM dimming for channel 14 according to law embedded in the Figure 9 00h: 0% - channel off 01h: 0.10% 7Fh: 3.09% FFh: 100% - channel on in DC
15-8	PWM_DUTY_CH13	00h	Exponential individual PWM dimming for channel 13 according to law embedded in the Figure 9 00h: 0% - channel off 01h: 0.10% 7Fh: 3.09% FFh: 100% - channel on in DC
7-0	PWM_DUTY_CH12	00h	Exponential individual PWM dimming for channel 12 according to law embedded in the Figure 9 00h: 0% - channel off 01h: 0.10% 7Fh: 3.09% FFh: 100% - channel on in DC

6.1.2 Channel current setting

Channel current setting 0x0Ah register

Address 0Ah

Access R/W/BW

Data Byte 3								Data Byte 2								Data Byte 1								Data Byte 0							
bit 31	bit 30	bit 29	bit 28	bit 27	bit 26	bit 25	bit 24	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CUR_SET_CH3								CUR_SET_CH2								CUR_SET_CH1								CUR_SET_CH0							

Table 24. Channel current setting 0x0Ah field description

Bit	Name	Default	Description
31-24	CUR_SET_CH3	FTP	Linear individual analogue dimming for channel 3 in 1/256 steps 00h: 6.3 mA FFh: 100 mA
24-16	CUR_SET_CH2	FTP	Linear individual analogue dimming for channel 2 in 1/256 steps 00h: 6.3 mA FFh: 100 mA
15-8	CUR_SET_CH1	FTP	Linear individual analogue dimming for channel 1 in 1/256 steps 00h: 6.3 mA FFh: 100 mA
7-0	CUR_SET_CH0	FTP	Linear individual analogue dimming for channel 0 in 1/256 steps 00h: 6.3 mA FFh: 100 mA

Channel current setting 0x0Bh register

Address 0Bh

Access R/W/BW

Data Byte 3								Data Byte 2								Data Byte 1								Data Byte 0							
bit 31	bit 30	bit 29	bit 28	bit 27	bit 26	bit 25	bit 24	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CUR_SET_CH7								CUR_SET_CH6								CUR_SET_CH5								CUR_SET_CH4							

Table 25. Channel current setting 0x0Bh field description

Bit	Name	Default	Description
31-24	CUR_SET_CH7	FTP	Linear individual analogue dimming for channel 7 in 1/256 steps 00h: 6.3 mA FFh: 100 mA
24-16	CUR_SET_CH6	FTP	Linear individual analogue dimming for channel 6 in 1/256 steps 00h: 6.3 mA FFh: 100 mA

Bit	Name	Default	Description
15-8	CUR_SET_CH5	FTP	Linear individual analogue dimming for channel 5 in 1/256 steps 00h: 6.3 mA FFh: 100 mA
7-0	CUR_SET_CH4	FTP	Linear individual analogue dimming for channel 4 in 1/256 steps 00h: 6.3 mA FFh: 100 mA

Channel current setting 0x0Ch register

Address 0Ch

Access R/W/BW

Data Byte 3								Data Byte 2								Data Byte 1								Data Byte 0							
bit 31	bit 30	bit 29	bit 28	bit 27	bit 26	bit 25	bit 24	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CUR_SET_CH11								CUR_SET_CH10								CUR_SET_CH9								CUR_SET_CH8							

Table 26. Channel current setting 0x0Ch field description

Bit	Name	Default	Description
31-24	CUR_SET_CH11	FTP	Linear individual analogue dimming for channel 11 in 1/256 steps 00h: 6.3 mA FFh: 100 mA
24-16	CUR_SET_CH10	FTP	Linear individual analogue dimming for channel 10 in 1/256 steps 00h: 6.3 mA FFh: 100 mA
15-8	CUR_SET_CH9	FTP	Linear individual analogue dimming for channel 9 in 1/256 steps 00h: 6.3 mA FFh: 100 mA
7-0	CUR_SET_CH8	FTP	Linear individual analogue dimming for channel 8 in 1/256 steps 00h: 6.3 mA FFh: 100 mA

Channel current setting 0x0Dh register

Address 0Dh

Access R/W/BW

Data Byte 3								Data Byte 2								Data Byte 1								Data Byte 0							
bit 31	bit 30	bit 29	bit 28	bit 27	bit 26	bit 25	bit 24	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CUR_SET_CH15								CUR_SET_CH14								CUR_SET_CH13								CUR_SET_CH12							

Table 27. Channel current setting 0x0Dh field description

Bit	Name	Default	Description
31-24	CUR_SET_CH15	FTP	Linear individual analogue dimming for channel 15 in 1/256 steps 00h: 6.3 mA FFh: 100 mA
24-16	CUR_SET_CH14	FTP	Linear individual analogue dimming for channel 14 in 1/256 steps 00h: 6.3 mA FFh: 100 mA
15-8	CUR_SET_CH13	FTP	Linear individual analogue dimming for channel 13 in 1/256 steps 00h: 6.3 mA FFh: 100 mA
7-0	CUR_SET_CH12	FTP	Linear individual analogue dimming for channel 12 in 1/256 steps 00h: 6.3 mA FFh: 100 mA

6.1.3 Channel mapping on DIN

Channel mapping on DIN register

Address 12h

Access R/W

Data Byte 3								Data Byte 2								Data Byte 1								Data Byte 0							
bit 31	bit 30	bit 29	bit 28	bit 27	bit 26	bit 25	bit 24	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
-	DIN_MAP_CH15	-	DIN_MAP_CH14	-	DIN_MAP_CH13	-	DIN_MAP_CH12	-	DIN_MAP_CH11	-	DIN_MAP_CH10	-	DIN_MAP_CH9	-	DIN_MAP_CH8	-	DIN_MAP_CH7	-	DIN_MAP_CH6	-	DIN_MAP_CH5	-	DIN_MAP_CH4	-	DIN_MAP_CH3	-	DIN_MAP_CH2	-	DIN_MAP_CH1	-	DIN_MAP_CH0

Table 28. Channel mapping on DIN field description

Bit	Name	Default	Description
Odd Bits	-	00h	Not used
30	DIN_MAP_CH15	FTP	Mapping of channel to direct input 0: channel NOT mapped to direct input, group 0 1: channel mapped to direct input , group 1
28	DIN_MAP_CH14	FTP	
26	DIN_MAP_CH13	FTP	
24	DIN_MAP_CH12	FTP	
22	DIN_MAP_CH11	FTP	
20	DIN_MAP_CH10	FTP	
18	DIN_MAP_CH9	FTP	
16	DIN_MAP_CH8	FTP	
14	DIN_MAP_CH7	FTP	
12	DIN_MAP_CH6	FTP	
10	DIN_MAP_CH5	FTP	
8	DIN_MAP_CH4	FTP	
6	DIN_MAP_CH3	FTP	
4	DIN_MAP_CH2	FTP	
2	DIN_MAP_CH1	FTP	
0	DIN_MAP_CH0	FTP	

6.1.4 Device configuration 1

Device configuration register #1

Address 15h

Access R/W

Data Byte 3								Data Byte 2								Data Byte 1								Data Byte 0							
bit 31	bit 30	bit 29	bit 28	bit 27	bit 26	bit 25	bit 24	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
-					FAULT_REACT_GROUP_0	-	FAULT_REACT_GROUP_1	PHASE_DEV (Read only)			OUT_DELAY	SYNC_IO_PC	PWM_SYNC	-		PWM_FREQ								-					SHT_THR_GROUP_0			

Table 29. Device configuration #1 field description

Bit	Name	Default	Description
31-27	-	0h	Not used
26	FAULT_REACT_GROUP_0	FTP	Fault reaction mode for channels NOT mapped 0: fault on one string, all strings of the same group are turned off 1: fault on one string, no action on other strings of same group
24	FAULT_REACT_GROUP_1	FTP	Fault reaction mode for channels mapped to direct input 0: fault on one string, all strings of the same group are turned off 1: Fault on one string, no action on other strings of same group
23-21	PHASE_DEV (Read Only in RAM)	FTP	PWM phase shift in responder mode: phase shift with regards to SYNC_IO synchronized clock in 15 µs steps: 000: 0 µs 001: 15 µs 010: 30 µs ... 111: 105 µs
20	OUT_DELAY	FTP	Enable/Disable of gradual output delay: 0: gradual delay disabled 1: gradual delay enabled
19	SYNC_IO_PC	FTP	Provider/Consumer SYNC_IO: Synchronization of PWM frequency and phase between provider and consumer devices 1: consumer mode selected. SYNC_IO isinput. Clock frequency and phase signal on the SYNC_IO line is used to synchronize own clock 0 (default): provider mode selected. SYNC_IO is output. Device clock frequency with scaler and phase signal is transferred to the SYNC_IO line
18	PWM_SYNC	0	Reset bit for internal PWM counter: 0: PWM counter running 1: PWM counter reset to zero; bit is automatically cleared directly after reset
17-11	-	000h	Not used

Bit	Name	Default	Description
10-8	PWM_FREQ	FTP	PWM frequency: 000: 200 Hz 001: 300 Hz 010: 400 Hz 011: 500 Hz 100: 700 Hz 101: 1000 Hz 110: 1200 Hz 111: 1400 Hz
7-4	-	0000h	Not used
3-0	SHT_THR_GROUP_0	FTP	Short circuit detection threshold for channels NOT mapped: Adjustable in 556 mV steps 0h: 0.556 V 1h: 1.112 V 2h: 1.668 V ... Fh: 8.9 V

6.1.5 Device configuration 2

Device configuration register #2

Address 16h

Access R/W

Data Byte 3								Data Byte 2								Data Byte 1								Data Byte 0							
bit 31	bit 30	bit 29	bit 28	bit 27	bit 26	bit 25	bit 24	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
-				-				-				SHT_THR_GROUP_1				-								PG_TH_VPREG							

Table 30. Device configuration #2 field description

Bit	Name	Default	Description
31-20	-	0h	Not used
19-16	SHT_THR_GROUP_1	FTP	Short circuit detection threshold for channels mapped to direct input: Adjustable in 556 mV steps 0h: 0.556 V 1h: 1.112 V 2h: 1.668 V ... Fh: 8.9 V
15-8	-	0h	Not used
7-0	PG_TH_VPREG	FTP	Power good threshold for VPREG adjustable in 78.4 mV steps - from 00h to 32h codes the threshold value is clamped to 4 V: 32h: 4.00 V 7Fh: 10.20 V DFh:17.84 V FFh: 20.40 V

6.1.6 Device configuration 3

Device configuration register #3

Address 17h

Access R/W

Data Byte 3								Data Byte 2								Data Byte 1								Data Byte 0							
bit 31	bit 30	bit 29	bit 28	bit 27	bit 26	bit 25	bit 24	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
-	-	DITHERING			VNTC_TH			-					DIN_EN	-	OL_EN	-				DIAG_BLANK_GROUP_1		DIAG_BLANK_GROUP_0		-	SHT_DET_EN	-	SHT_EN	-	SHT_OFF_GROUP_0	-	SHT_OFF_GROUP_1

Table 31. Device configuration #3 field description

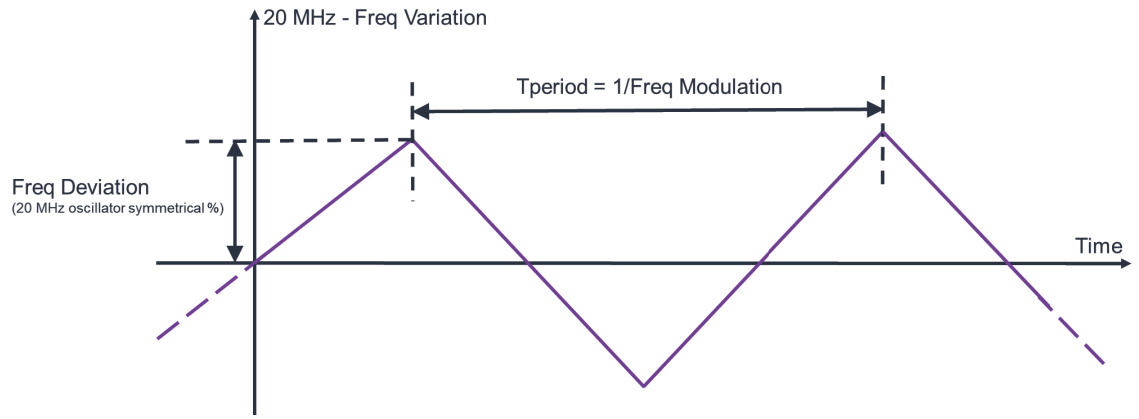
Bit	Name	Default	Description
31-30	-	0000	Not used
29-27	DITHERING	FTP	See the Table 32
26-24	VNTC_TH	FTP	NTC voltage threshold related to the start of derating See the Table 64
23-19	-	0	Not used
18	DIN_EN	0	DIN enable in bus mode 0: DIN disabled 1: DIN enabled
17	-	0	Not used
16	OL_EN	FTP	Enable open-load fault propagation of group 1 on FAULT pin 0: open-load propagation to FAULT pin disabled 1: open-load propagation to FAULT pin enabled
15-12	-	0	Not used
11-10	DIAG_BLANK_GROUP_1	FTP	Diagnostic blanking time after rising edge (incl PWM) for group 1 - channels mapped to DIN 00: 5 µs 01: 10µs 10: 20µs 11: 50 µs
9-8	DIAG_BLANK_GROUP_0	FTP	Diagnostic blanking time after rising edge (incl PWM) for group 0 - channels NOT mapped 00: 5 µs 01: 10µs 10: 20µs 11: 50 µs
7	-	0	Not used
6	SHT_DET_EN	FTP	Short circuit detection enable bit 0: short circuit detection disabled

Bit	Name	Default	Description
			1: short circuit detection enabled
5	-	0	Not used
4	SHT_EN	FTP	Enable short circuit fault propagation on FAULT pin – for channels mapped on DIN 0: short circuit propagation to FAULT pin disabled 1: short circuit propagation to FAULT pin enabled
3	-	0	Not used
2	SHT_OFF_GROUP_0	FTP	Output deactivation in case of short circuit detection for group 0 (channels NOT mapped) 0: output deactivation disabled 1: output deactivation enabled
1	-	0	Not used
0	SHT_OFF_GROUP_1	FTP	Output deactivation in case of short circuit detection for group 1 (mapped to DIN) 0: output deactivation disabled 1: output deactivation enabled

Table 32. Dithering

DITHERING [2÷0]	Rejection [dB]	Freq [kHz]	Df [%]
000	0	Inf	0
001	-7.38	156	1.6
010	-11.68	78	3.2
011	-13.28	52	4.8
100	-14.58	39	6.4
101	-15.48	32	8
110	-16.28	25	9.6
111	-16.78	22	11.2

Figure 39. 20 MHz oscillator, dithering - modulation curve



6.1.7 Device configuration 4

Device configuration register #4

Address 18h

Access R/W

Data Byte 3								Data Byte 2								Data Byte 1								Data Byte 0							
bit 31	bit 30	bit 29	bit 28	bit 27	bit 26	bit 25	bit 24	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
-																													CS_EN	GOSTBY	BUSMODE

Table 33. Device configuration #4 field description

Bit	Name	Default	Description
31-3	-	0	Not used Must remain unchanged (set to '0')
2	CS_EN	0	Chip select enable to enter FTP programming mode 0: chip select disabled 1: chip select enabled
1	GOSTBY	0	See the Table 34
0	BUSMODE	0	

Table 34. State transition bits

GOSTBY	BUSMODE	State
0	0	Reset → fail-safe/stand-alone
0	1	Normal mode/bus mode
1	0	Initialization → standby mode
1	1	Reset → fail-safe/stand-alone

6.1.8 Watchdog

Watchdog register

Address 19h

Access R/W

Data Byte 3								Data Byte 2								Data Byte 1								Data Byte 0							
bit 31	bit 30	bit 29	bit 28	bit 27	bit 26	bit 25	bit 24	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
-																															WD_TRIG

Table 35. Watchdog field description

Bit	Name	Default	Description
31-1	-	0	Not used
0	WD_TRIG	0	Watchdog trigger In order to keep device in normal mode/bus mode, this bit must be cyclically toggled within a period configured by WD_CONF bits to refresh the watchdog

6.1.9 Position and chain identifier for responder ID

Position and chain identifier for responder ID register

Address 1Ah

Access R

Data Byte 3								Data Byte 2								Data Byte 1								Data Byte 0							
bit 31	bit 30	bit 29	bit 28	bit 27	bit 26	bit 25	bit 24	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
-																								ChainID_ResponderID0						POS_ResponderID0	

Table 36. Position and chain identifier for responder IDx field description

Bit	Name	Default	Description
31-8	-	0	Not used
7-2	ChainID_ResponderID0	000000	6-bit chain identifier for responder ID0
1-0	POS_ResponderID0	0	2-bit position identifier in chain for responder ID0

6.1.10 Channel output on-state voltage

Channel output on-state voltage 0x1Fh register

Address 1Fh

Access Burst Read

Data Byte 3								Data Byte 2								Data Byte 1								Data Byte 0							
bit 31	bit 30	bit 29	bit 28	bit 27	bit 26	bit 25	bit 24	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
VLED_ON_CH3								VLED_ON_CH2								VLED_ON_CH1								VLED_ON_CH0							

Table 37. Channel output on-state voltage 0x1Fh field description

Bit	Name	Default	Description
31-24	VLED_ON_CH3	00h	8-bit output on-state voltage channel 3 in 1/256 steps 00h: 0 mV 01h: 78 mV 7Fh: 9.96 V FFh: 20 V
23-16	VLED_ON_CH2	00h	8-bit output on-state Voltage Channel 2 in 1/256 steps 00h: 0 mV 01h: 78 mV 7Fh: 9.96 V FFh: 20 V
15-8	VLED_ON_CH1	00h	8-bit output on-state voltage channel 1 in 1/256 steps 00h: 0 mV 01h: 78 mV 7Fh: 9.96 V FFh: 20 V
7-0	VLED_ON_CH0	00h	8-bit output on-state voltage channel 1 in 1/256 steps 00h: 0 mV 01h: 78 mV 7Fh: 9.96 V FFh: 20 V

Channel output on-state voltage 0x20h register

Address 20h

Access Burst read from 1Fh/Read

Data Byte 3								Data Byte 2								Data Byte 1								Data Byte 0							
bit 31	bit 30	bit 29	bit 28	bit 27	bit 26	bit 25	bit 24	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
VLED_ON_CH7								VLED_ON_CH6								VLED_ON_CH5								VLED_ON_CH4							

Table 38. Channel output on-state voltage 0x20h field description

Bit	Name	Default	Description
31-24	VLED_ON_CH7	00h	8-bit output on-state voltage channel 7 in 1/256 steps 00h: 0 mV 01h: 78 mV 7Fh: 9.96 V FFh: 20 V
23-16	VLED_ON_CH6	00h	8-bit output on-state voltage channel 6 in 1/256 steps 00h: 0 mV 01h: 78 mV 7Fh: 9.96 V FFh: 20 V
15-8	VLED_ON_CH5	00h	8-bit output on-state voltage channel 5 in 1/256 steps 00h: 0 mV 01h: 78 mV 7Fh: 9.96 V FFh: 20 V
7-0	VLED_ON_CH4	00h	8-bit output on-state voltage channel 4 in 1/256 steps 00h: 0 mV 01h: 78 mV 7Fh: 9.96 V FFh: 20 V

Channel output on-state voltage 0x21h register

Address 21h

Access Burst Read from 1Fh/Read

Data Byte 3								Data Byte 2								Data Byte 1								Data Byte 0							
bit 31	bit 30	bit 29	bit 28	bit 27	bit 26	bit 25	bit 24	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
VLED_ON_CH11								VLED_ON_CH10								VLED_ON_CH9								VLED_ON_CH8							

Table 39. Channel output on-state voltage 0x21h field description

Bit	Name	Default	Description
31-24	VLED_ON_CH11	00h	8-bit output on-state voltage channel 11 in 1/256 steps 00h: 0 mV 01h: 78 mV 7Fh: 9.96 V FFh: 20 V

Bit	Name	Default	Description
23-16	VLED_ON_CH10	00h	8-bit output on-state voltage channel 10 in 1/256 steps 00h: 0 mV 01h: 78 mV 7Fh: 9.96 V FFh: 20 V
15-8	VLED_ON_CH9	00h	8-bit output on-state voltage channel 9 in 1/256 steps 00h: 0 mV 01h: 78 mV 7Fh: 9.96 V FFh: 20 V
7-0	VLED_ON_CH8	00h	8-bit output on-state voltage channel 8 in 1/256 steps 00h: 0 mV 01h: 78 mV 7Fh: 9.96 V FFh: 20 V

Channel output on-state voltage 0x22h register

Address 22h

Access Burst Read from 1Fh/Read

Data Byte 3								Data Byte 2								Data Byte 1								Data Byte 0							
bit 31	bit 30	bit 29	bit 28	bit 27	bit 26	bit 25	bit 24	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
VLED_ON_CH15								VLED_ON_CH14								VLED_ON_CH13								VLED_ON_CH12							

Table 40. Channel output on-state voltage 0x22h field description

Bit	Name	Default	Description
31-24	VLED_ON_CH15		8-bit output on-state voltage channel 15 in 1/256 steps 00h: 0 mV 01h: 78 mV 7Fh: 9.96 V FFh: 20 V
23-16	VLED_ON_CH14		8-bit output on-state voltage channel 14 in 1/256 steps 00h: 0 mV 01h: 78 mV 7Fh: 9.96 V FFh: 20 V
15-8	VLED_ON_CH13	00h	8-bit output on-state voltage channel 13 in 1/256 steps 00h: 0 mV 01h: 78 mV 7Fh: 9.96 V FFh: 20 V
7-0	VLED_ON_CH12	00h	8-bit output on-state voltage channel 12 in 1/256 steps

Bit	Name	Default	Description
			00h: 0 mV 01h: 78 mV 7Fh: 9.96 V FFh: 20 V

6.1.11 Channel output status

Channel output status register

Address 27h

Access Burst Read

Data Byte 3								Data Byte 2								Data Byte 1								Data Byte 0							
bit 31	bit 30	bit 29	bit 28	bit 27	bit 26	bit 25	bit 24	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
-																OUT_STATUS_CH8-15								OUT_STATUS_CH0-7							

Table 41. Channel output on-state voltage 0x22h field description

Bit	Name	Default	Description
31-16	-	0	Not used
15	OUT_STATUS_CH15	0	Output status bit 0: channel gate off 1: channel gate on (regardless of the PWM OFF phase)
14	OUT_STATUS_CH14	0	
13	OUT_STATUS_CH13	0	
12	OUT_STATUS_CH12	0	
11	OUT_STATUS_CH11	0	
10	OUT_STATUS_CH10	0	
9	OUT_STATUS_CH9	0	
8	OUT_STATUS_CH8	0	
7	OUT_STATUS_CH7	0	
6	OUT_STATUS_CH6	0	
5	OUT_STATUS_CH5	0	
4	OUT_STATUS_CH4	0	
3	OUT_STATUS_CH3	0	
2	OUT_STATUS_CH2	0	
1	OUT_STATUS_CH1	0	
0	OUT_STATUS_CH0	0	

6.1.12 Channel short circuit status

Channel short circuit status register

Address 28h

Access Burst Read from 27h/Read/Read and Clear

Data Byte 3								Data Byte 2								Data Byte 1								Data Byte 0							
bit 31	bit 30	bit 29	bit 28	bit 27	bit 26	bit 25	bit 24	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
-																SHT_CH8-15								SHT_CH0-7							

Table 42. Channel short circuit status field description

Bit	Name	Default	Description
31-16	-	0	Not used
15	STH_CH15	0	Short circuit status bit 0: no fault on channel 1: fault validated on channel SHT_CHx are R&C bits
14	STH_CH14	0	
13	STH_CH13	0	
12	STH_CH12	0	
11	STH_CH11	0	
10	STH_CH10	0	
9	STH_CH9	0	
8	STH_CH8	0	
7	STH_CH7	0	
6	STH_CH6	0	
5	STH_CH5	0	
4	STH_CH4	0	
3	STH_CH3	0	
2	STH_CH2	0	
1	STH_CH1	0	
0	STH_CH0	0	

6.1.13 Channel open-load status

Channel open-load status register

Address 29h

Access Burst Read from 27h/Read/Read and Clear

Data Byte 3								Data Byte 2								Data Byte 1								Data Byte 0							
bit 31	bit 30	bit 29	bit 28	bit 27	bit 26	bit 25	bit 24	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
-																OL_CH8-15								OL_CH0-7							

Table 43. Channel open-load status field description

Bit	Name	Default	Description
31-16	-	0	Not used
15	OL_CH15	0	
14	OL_CH14	0	
13	OL_CH13	0	
12	OL_CH12	0	
11	OL_CH11	0	
10	OL_CH10	0	
9	OL_CH9	0	Short load status bit
8	OL_CH8	0	0: no fault on channel
7	OL_CH7	0	1: fault validated on channel
6	OL_CH6	0	OL_CHx are R&C bits
5	OL_CH5	0	
4	OL_CH4	0	
3	OL_CH3	0	
2	OL_CH2	0	
1	OL_CH1	0	
0	OL_CH0	0	

6.1.14 Channel short to VPREG status

Channel short to VPREG status register

Address 2Ah

Access Burst Read from 27h/Read/Read and Clear

Data Byte 3								Data Byte 2								Data Byte 1								Data Byte 0							
bit 31	bit 30	bit 29	bit 28	bit 27	bit 26	bit 25	bit 24	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
-																OUT_SHT_VPREG_CH8-15								OUT_SHT_VPREG_CH0-7							

Table 44. Channel short to VPRE_REG_X STATUS field description

Bit	Name	Default	Description
31-16	-	0	Not used
15	OUT_SHT_VPREG_CH15	0	Output short to VPREG Status bit 0: no fault on channel 1: fault validated on channel OUT_SHT_VPREG_CHx are R&C bits
14	OUT_SHT_VPREG_CH14	0	
13	OUT_SHT_VPREG_CH13	0	
12	OUT_SHT_VPREG_CH12	0	
11	OUT_SHT_VPREG_CH11	0	
10	OUT_SHT_VPREG_CH10	0	
9	OUT_SHT_VPREG_CH9	0	
8	OUT_SHT_VPREG_CH8	0	
7	OUT_SHT_VPREG_CH7	0	
6	OUT_SHT_VPREG_CH6	0	
5	OUT_SHT_VPREG_CH5	0	
4	OUT_SHT_VPREG_CH4	0	
3	OUT_SHT_VPREG_CH3	0	
2	OUT_SHT_VPREG_CH2	0	
1	OUT_SHT_VPREG_CH1	0	
0	OUT_SHT_VPREG_CH0	0	

6.1.15 Channel VLEDON ADC status

Channel VLEDON ADC status refresh register

Address 2Bh

Access Read

Data Byte 3								Data Byte 2								Data Byte 1								Data Byte 0							
bit 31	bit 30	bit 29	bit 28	bit 27	bit 26	bit 25	bit 24	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
-																VLEDON_RFR_CH8-15								VLEDON_RFR_CH0-7							

Table 45. Channel VLEDON ADC status refresh field description

Bit	Name	Default	Description
31-16	-	0	Not used
15	VLEDON_RFR_CH15	0	VLEDON ADC status refresh bit 0: VLEDON ADC result not updated since last reading 1: VLEDON ADC result updated since last reading
14	VLEDON_RFR_CH14	0	
13	VLEDON_RFR_CH13	0	
12	VLEDON_RFR_CH12	0	
11	VLEDON_RFR_CH11	0	
10	VLEDON_RFR_CH10	0	
9	VLEDON_RFR_CH9	0	
8	VLEDON_RFR_CH8	0	
7	VLEDON_RFR_CH7	0	
6	VLEDON_RFR_CH6	0	
5	VLEDON_RFR_CH5	0	
4	VLEDON_RFR_CH4	0	
3	VLEDON_RFR_CH3	0	
2	VLEDON_RFR_CH2	0	
1	VLEDON_RFR_CH1	0	
0	VLEDON_RFR_CH0	0	

6.1.16 Device status 1

Device status register #1

Address 2Ch

Access Burst read from 2Ch

Data Byte 3								Data Byte 2								Data Byte 1								Data Byte 0							
bit 31	bit 30	bit 29	bit 28	bit 27	bit 26	bit 25	bit 24	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
T_J								-								V_{PREG}								V_S							

Table 46. Device status #1 field description

Bit	Name	Default	Description
31-24	T_J	0h	8-bit value of junction temperature in 1/256 steps 6Bh: 175 °C 82h: 140 °C A6h: 85°C CCh:25 °C F7h: -40 °C
23-16	-	00h	Not used
15-8	V_{PREG}	00h	8-bit voltage of VPREG in 1/256 steps 00h: 0 mV 01h: 78.4 mV 7Fh: 9.96 V FFh: 20 V
7-0	V_S	00h	8-bit voltage of VS in 1/256 steps 00h: 0 mV 01h: 157 mV 7Fh: 19.9 V FFh: 40 V

6.1.17 Device status 2

Device status register #2

Address 2Dh

Access Burst read from 2Ch/Read

Data Byte 3								Data Byte 2								Data Byte 1								Data Byte 0							
bit 31	bit 30	bit 29	bit 28	bit 27	bit 26	bit 25	bit 24	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
NTC_ADC								-								-								-							

Table 47. Device status #2 field description

Bit	Name	Default	Description
31-24	NTC_ADC	00h	8-bit voltage of NTC in 1/256 steps 00h: 0 mV 01h: 10 mV 7Fh: 1.25 V FFh: 2.50 V
23-0	-	00h	Not used

6.1.18 Device status 3

Device status register #3

Address 2Eh

Access Burst read from 2Ch/Read/Read and Clear

Data Byte 3								Data Byte 2								Data Byte 1								Data Byte 0							
bit 31	bit 30	bit 29	bit 28	bit 27	bit 26	bit 25	bit 24	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
-															RDAC_FAULT	WD_FAIL	VS_UV	WD_STATUS		-	DIN_STATUS	NTC_FAULT	NTC_DER_ACT	OR_OL	OR_SHT	OR_OUT_STATUS	OR_OUT_SHT_VPREG	TW	TSD	-	PG_NOT_VPREG	

Table 48. Device status #3 field description

Bit	Name	Default	Description
31-17	-	0	Not used
16	RDAC_FAULT	0	External DAC reference resistor Fault: 0: No fault on external DAC reference resistor 1: Open or short circuit fault on external DAC reference resistor
15	WD_FAIL	0	Watchdog fail: 0: watchdog trigger bit toggled within WD_CONF timeout period - watchdog fail 1: watchdog trigger bit not toggled within WD_CONF timeout period - devices enters fail-safe/stand-alone
14	VS_UV	0	V_S undervoltage fault bit: 0: VS > VS_UV 1: VS < VS_UV
13-12	WD_STATUS	00	Watchdog status bits: 00: 0% < timer status < 24% 01: 24% < timer status < 50% 01: 50% < timer status < 74% 11: timer status > 74%
11	-	0	Not used
10	DIN_STATUS	0	Direct input 0 status bit: 0: low logical level at DIN0 1: high logical level at DIN0
9	NTC_FAULT	0	NTC fault status bit: 0: no short circuit fault detected on NTC: VNTC > VNTC_SHT 1: short circuit fault detected on NTC: VNTC < VNTC_SHT
8	NTC_DER_ACT	0	NTC derating active bit status bit: 0: VNTC > VNTC_TH, no derating active 1: VNTC < VNTC_TH, NTC derating active
7	OR_OL	0	OR combination of all channels´ open-load status flags: 0: no open-load is present on any active channel

Bit	Name	Default	Description
			1: open-load present on an active channel
6	OR_SHT	0	OR combination of all channels´ short circuit status flags: 0: no short circuit is present on any active channel 1: short circuit present on an active channel
5	OR_OUT_STATUS	0	OR combination of all channels´ output status flags: 0: all output gate drivers are inactive 1: at least one output gate driver is active
4	OR_OUT_SHT_VPREG	0	OR combination of all channels´ output short to VPREG status flags: 0: no short circuit to VPREG is present on any active channel 1: short circuit to VPREG is present on any active channel
3	TW	0	Thermal warning status bit: 0: $T_J < T_{TW} – T_{TW\_HYST}$, thermal warning not active, T_J derating not active 1: $T_J > T_{TW}$, thermal warning active, T_J derating active
2	TSD	0	Thermal shutdown status bit: 0: $T_J < T_{TSD} - T_{TSD\_HYST}$, thermal shutdown not active, device not in autorestart thermal cycling 1: $T_J > T_{TSD} - T_{TSD\_HYST}$, thermal shutdown active, device in autorestart thermal cycling
1	-	0	Not used
0	PG_NOT_VPREG	1	Power good not threshold status bit VPREG: 1: VPREG < $V_{PG\_TH\_VPREG}$, Power good threshold not reached on VPREG 0: VPREG > $V_{PG\_TH\_VPREG}$, Power good threshold reached on VPREG

6.1.19 FTP status 1

FTP status register #1

Address 2Fh

Access Burst read from 2Ch/Read

Data Byte 3								Data Byte 2								Data Byte 1								Data Byte 0							
bit 31	bit 30	bit 29	bit 28	bit 27	bit 26	bit 25	bit 24	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
-									STB_CONF	POR_DELAY		WD_CONF		-	PWM_FS_ALL_EN	-															

Table 49. FTP status #1 field description

Bit	Name	Default	Description
31-23	-	-	Not used
22	STB_CONF	0	Device STB pin configuration, for flexiblw usage of the external transceiver: 0: transceiver normal mode with STB pin Low 1: transceiver normal mode with STB pin High
21-20	POR_DELAY	00	Power on reset delay time (t_{POR_DELAY}); delay time before activating outputs in fail-safe/ stand-alone mode after POR 00: 0 ms 01: 25 ms 10: 50 ms 11: 100 ms
19-18	WD_CONF	00	Watchdog timeout period t_WD 00: 50 ms 01: 100 ms 10: 200 ms 11: 25 ms
17	-	0h	Not used
16	PWM_FS_ALL_EN	0	Enable bit of internal PWM dimming in fail-safe/stand-alone mode for group 1 - channels mapped on DIN: 0: internal PWM dimming disabled 1: internal PWM dimming enabled (PWM_DUTY_ALL FTP value with PWM_FREQ FTP Value)
15-0	-	00h	Not used

6.1.20 FTP status 2

FTP status register #2

Address 30h

Access Read

Data Byte 3								Data Byte 2								Data Byte 1								Data Byte 0							
bit 31	bit 30	bit 29	bit 28	bit 27	bit 26	bit 25	bit 24	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
-																FS_OUT15-8_EN								FS_OUT7-0_EN							

Table 50. FTP status #2 field description

Bit	Name	Default	Description
31-16	-	0	Not used
15	FS_OUT15_EN	0	Output permanent on enable bit in fail-safe/stand-alone mode 0: output permanent on disabled 1: output permanent on enabled
14	FS_OUT14_EN	0	
13	FS_OUT13_EN	0	
12	FS_OUT12_EN	0	
11	FS_OUT11_EN	0	
10	FS_OUT10_EN	0	
9	FS_OUT9_EN	0	
8	FS_OUT8_EN	0	
7	FS_OUT7_EN	0	
6	FS_OUT6_EN	0	
5	FS_OUT5_EN	0	
4	FS_OUT4_EN	0	
3	FS_OUT3_EN	0	
2	FS_OUT2_EN	0	
1	FS_OUT1_EN	0	
0	FS_OUT0_EN	0	

6.2 FTP row description

6.2.1 Device FTP configuration - Row 0

Address 0x0h

Access R/W

Table 51. Row 0

Bit	Name	Default	Description
127-29	Free configurable(1)	-	-
28	Lock_Row_12	0	0: Row_12 unlocked (R/W access) 1: Row_12 locked (R only access)
27-19	Free configurable(1)		
18-16	Lock_Row_2 to Lock_Row_0	0	0: Row_x unlocked (R/W access) 1: Row_x locked (R only access)
15-10	Free configurable(1)		
9	Lock_Responder ID	0	0: Responder ID unlocked (R/W access) 1: Responder ID locked (R only access)
8-0	Responder ID	0	

1. *To pay attention not to write in the adjacent dedicated Lock bit positions.*

6.2.2 Device FTP configuration - Row 1

Address 0x1h

Access R/W

Table 52. Row 1

Bit	Name	Default	Description
127-108	Free configurable	-	-
107-104	SHT_THR_GROUP_1	0	-
103-100	Free configurable	-	-
99-96	SHT_THR_GROUP_0	0	-
95-80	DIN_MAP_CH <7-0>	0	-
79-72	FS_OUT<7-0>_EN	0	-
71-64	Free configurable	-	-
63-0	CUR_SET_CH<7-0>	0	-

6.2.3 Device FTP configuration - Row 2

Address 0x2h

Access R/W

Table 53. Row 2

Bit	Name	Default	Description
127-96	Free configurable	-	-

Bit	Name	Default	Description
95-80	DIN_MAP_CH <15-8>	0	-
79-72	FS_OUT<15-8>_EN	0	-
71-64	Free configurable	-	-
63-0	CUR_SET_CH<15-8>	0	-

6.2.5 Device FTP configuration - Row 11

Address 0xBh

Access R

Table 54. Row 11

Bit	Name	Default	Description
127-120	Reserved	-	-
119-0	ENCRYPTED TRACEABILITY CODE - 120 bits	0	Traceability Code - Read Only

6.2.6 Device FTP configuration - Row 12

Address 0xCh

Access R/W

Table 55. Row 12

Bit	Name	Default	Description
127-120	Free configurable	-	-
119-117	DITHERING	0	-
116-112	CAN BIT SAMPLING POINT	0	-
111-104	Free configurable	-	-
103-96	PG_TH_VPREG	0	-
95-93	Free configurable	-	-
92	SYNC_IO_PC	0	-
91-90	POR_DELAY	0	-
89	Free configurable	-	-
88	SHT_DET_EN	0	-
87-86	WD_CONF	0	-
85-84	Free configurable	-	-
83	STB_CONF	-	-
82-80	VNTC_TH	0	-
79-72	Free configurable	-	-
71-69	PWM_FREQ	0	-
68	OL_EN	0	-
67-66	Free configurable	-	-
65	FAULT_REACT_GROUP_1	0	-

Bit	Name	Default	Description
64	FAULT_REACT_GROUP_0	0	-
63-56	Free configurable	-	-
55	SHT_EN	0	-
54	SHT_OFF_GROUP_1	0	-
53	SHT_OFF_GROUP_0	0	-
52-44	Free configurable	-	-
43-42	DIAG_BLANK_GROUP_1	0	-
41-40	DIAG_BLANK_GROUP_0	0	-
39-37	PHASE_DEV	0	-
36	OUT_DELAY	0	-
35-33	Free configurable	-	-
32	PWM_FS_ALL_EN	0	-
31-8	Free configurable	-	-
7-0	PWM_DUTY_ALL	0	-

Table 56. CAN bit sampling point

CAN sampling point FTP value [hex]	CAN sampling point [%]
00	53.1
01	50.0
02	46.9
03	43.8
04	40.6
05	37.5
06	34.4
07	31.3
08	28.1
09	25.0
0A	21.9
0B	18.8
0C	15.6
0D	12.5
0E	9.40
0F	Not supported
10	Not supported
11	Not supported
12	Not supported
13	93.8
14	90.6
15	87.5
16	84.4
17	81.3

CAN sampling point FTP value [hex]	CAN sampling point [%]
18	78.1
19	75.0
1A	71.9
1B	68.8
1C	65.6
1D	62.5
1E	59.4
1F	56.3

7 Electrical characteristics

Unless otherwise specified, the operating battery voltage and junction temperature ranges are 5 V < V_S < 28 V, -40 °C < T_J < 150 °C.

The device is still operative and functional at higher temperatures (up to 175 °C). Voltages are referred to ground and currents are assumed positive when the current flows into the pin. The device is operated in the mentioned operating range, unless otherwise specified.

Note: Parameter limits at temperatures higher than 150 °C may change with respect to what is specified as per the standard temperature range.

Device functionality at high temperature is guaranteed by characterization.

7.1 Absolute maximum ratings

Stressing the device above the "Absolute maximum ratings" may cause permanent damage to the device.

Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 57. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_S	Input supply pin of the IC	-0.3 ÷ 40	V
V_{OUT_X}	Output pin for the CHx (x = 0÷13)	-0.3 ÷ V_{PREG}	
V_{PREG}	External preregulator voltage	0 ÷ 20	
$V_{\_IO}$	External transceiver supply voltage	-0.3 ÷ 7	
V_{3V3}	3V3 regulator (internal) output voltage	-0.3 ÷ 4.6	
V_{NTC}	NTC analog input voltage	-0.3 ÷ V_{3V3} + 0.3	
V_{DIN}	Direct input pin voltage	-0.3 ÷ 7	
V_{FAULT}	Diagnostic I/O pin voltage	-0.3 ÷ V_{3V3} + 0.3	
V_{SYNC_IO}	Synchronization I/O pin voltage	-0.3 ÷ V_{3V3} + 0.3	
V_{RX}	External transceiver interface pin – receiver voltage	-0.3 ÷ $V_{\_IO}$ + 0.3	
V_{TX}	External transceiver interface pin – transmitter voltage	-0.3 ÷ $V_{\_IO}$ + 0.3	
V_{STB}	External transceiver interface pin – standby programmable open-drain, voltage	-0.3 ÷ $V_{\_IO}$ + 0.3	
V_{CS}	Chip select input pin voltage	-0.3 ÷ 7	
V_{TESTx}	Test pin voltage	-0.3 ÷ V_{3V3} + 0.3	
V_{RDAC}	External resistor (for DACs ref) pin voltage	-0.3 ÷ V_{3V3} + 0.3	
N_{FTP}	Number of FTP writing cycles (no integrated counter taking note about the FTP writing cycles)	1000	-

7.2 ESD protection

Table 58. ESD protection

Parameter	Value	Unit
Electrostatic Discharge Test (AECQ100-002-E) - all pins	±2	kV
Electrostatic Discharge Test (AECQ100-002-E) - all output pins(1)	±4	kV
Charge Device Model (CDM-AEC-Q100-011) - all pins	±500	V
Charge Device Model (CDM-AEC-Q100-011) - corner pins	±750	V
Machine Model(2) - all pins	±150	V

1. *V_S, GND*
2. *According to Machine Model: C = 200 pF; R = 0 Ω*

7.3 Thermal characteristics

Table 59. QFN32L 5x5 package thermal data

Symbol	Parameter	Min.	Typ.	Max.	Unit
$R_{thj\text{-}amb}$(1)	Thermal resistance junction to ambient (JEDEC JESD 51-2)	-	25	-	°C/W
$R_{thj\text{-}top}$	Junction-to-top thermal resistance (JEDEC JESD 51-2)	-	2.7	-	°C/W

1. *Device soldered on 2s2p PCB thermally enhanced (slug included).*

Table 60. Thermal data, warning and shutdown

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_{STG}	Storage temperature	-55		150	°C
T_J	Operating junction temperature	-40		150	°C
T_{TW}	Junction temperature thermal warning - threshold	130	140	150	°C
T_{TW_HYST}	Junction temperature thermal warning - hysteresis		10		°C
T_{TSD}	Junction temperature thermal shutdown - threshold	160	175	190	°C
T_{TSD_HYST}	Junction temperature thermal shutdown - hysteresis		15		°C

7.4 Main electrical characteristics

Table 61. Supply

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_S	Operating battery voltage		5		28	V
V_{S_UV}	V_S undervoltage shutdown		3.75	4	4.25	V
$V_{S\_UV\_RST}$	V_S undervoltage shutdown - reset threshold			4.5	4.75	V
I_{VS_STBY}	V_S standby current consumption	Device in standby mode through: DIN = Low No CAN communication		40	65	µA
$I_{VS\_OP\_OUT\_OFF}$	V_S operating current consumption - all outputs off			10		mA

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{VS\_OP\_OUT\_ON}$	V_S operating current consumption - all outputs on	ΣI_{OUTx} = 1 A, x = [0÷15]		23		mA
$V_{\_IO}$	External CAN transceiver supply - output voltage		4.85	5	5.15	V
$I_{V\_IO, STDBY}$	External CAN transceiver supply regulator - V_IO standby current consumption	Device in standby mode through: DIN = Low No CAN communication			1	µA
$I_{V\_IO, OP}$	External CAN transceiver supply regulator - V_IO operating current consumption	RX stimulated with 500 kHz TX follows RX with 500 kHz (internal loop in test mode). No pull up between TX and VIO		160		µA
V_{3V3}	3.3 V regulator output voltage	TBD	3.2	3.3	3.4	V
I_{V3V3}	3.3 V regulator output current		50		100	mA
I_{V3V3_SHT}	3.3 V regulator short circuit current		130	170	200	mA
$V_{3V3\_POR\_H}$	3.3 V regulator power on reset - high threshold voltage		2.68	2.8	2.91	V
$V_{3V3\_POR\_L}$	3.3 V regulator power on reset - low threshold voltage		2.4	2.5	2.6	V
$V_{3V3\_POR\_HYST}$	3.3 V regulator power on reset - hysteresis			300		mV
$V_{S\_POR\_H}$	Internal preregulator power on reset - high threshold voltage		2.4	2.5	2.6	V
$V_{S\_POR\_L}$	Internal preregulator power on reset - low threshold voltage		2.2	2.3	2.4	V
$V_{S\_POR\_HYST}$	Internal preregulator power on reset–hysteresis			200		mV

7.5 Linear current sinkers

The LDLL16EN features 16 channels in low-side configuration. Output current regulation is demanded to 16 integrated linear current sinkers. Their relevant electrical characteristics are reported in the Table 62.

Table 62. Output characteristics

Symbol	Parameter		Test conditions	Min.	Typ.	Max.	Unit
I_{OUTx}	Channel output current - range			6.3		100	mA
I_{OUTx_STEP}	Channel output current - step			TBD	0.368	TBD	mA
I_{OUTx_ACC}	Channel output current - accuracy(1)		6.3 mA ≤ I_{OUTx} < 8.5 mA		±14		%
			8.5 mA ≤ I_{OUTx} < 17 mA		±11		
			17 mA ≤ I_{OUTx} < 52 mA		±9		
			52 mA ≤ I_{OUTx} ≤ 100 mA		±8		
ΔI_{OUTx}	Channel to channel output current – deviation within the same device		6.3 mA ≤ I_{OUTx} < 8.5 mA		±15		%
			8.5 mA ≤ I_{OUTx} < 17 mA		±13		
			17 mA ≤ I_{OUTx} < 52 mA		±10		
			52 mA ≤ I_{OUTx} < 100 mA		±9		
I_{OUTx_LEAK}	Channel output current - leakage		T_J = 125 °C V_{OUTx} = 20 V OUTx channel off			1	µA
V_{OUTx_DROP}	Channel output voltage - drop(2)		I_{OUTx} = 100 mA T_J = 125 °C	1			V
t_{GD}	Gradual delay for each output		All channels enabled	TBD	1.8	TBD	µs
t_{SR_ON}	Slew rate - turn on time for each channel			TBD	1	TBD	µs
t_{SR_OFF}	Slew rate - turn off time for each channel			TBD	1	TBD	µs
$V_{SHT\_TH\_GROUP\_X\_min}$	Short circuit threshold - minimum voltage				0.556		V
$V_{SHT\_TH\_GROUP\_X,max}$	Short circuit threshold - maximum voltage				8.9		V
$V_{SHT\_TH\_GROUP\_X,step}$	Short circuit threshold - step voltage				556		mV
$V_{OUT\_SHT\_PREG\_TH}$	Short circuit between output and external pre-regulator - threshold voltage				1		V
$V_{PG\_TH\_VPREG\_min}$	Minimum V_{PREG} power good threshold - for OL detection enabling				4(3)		V
$V_{PG\_TH\_VPREG\_max}$	Maximum V_{PREG} power good threshold - for OL detection enabling				20		V
$V_{PG\_TH\_VPREG\_step}$	V_{PREG} power good thresholdstep				78.4		mV
V_{OL_TH}	Open-load - voltage threshold				240		mV
V_{NTC_TH}	NTC threshold voltage - derating start				See the Table 64		
V_{NTC_SHT}	NTC threshold voltage - short detection			TBD	245	TBD	mV
N_Fails	Number of detected failures (also non-consecutive) - counter cycles	Short Circuit			15		
		Open-load			8		

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
N_Fails_reset	Number of NOT detected failures (consecutive) - counter reset			3		

1. *Upon the usage of the suggested resistance on RDAC pin.*
2. *Minimum voltage drop from device OUTx to device GND to guarantee programmed current regulation.*
3. *Any V_{PREG} value from 00h to 32h codes is clamped to 4 V.*

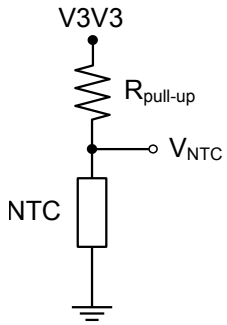
Table 63. PWM characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
PWM_FREQ_MIN	PWM minimum frequency			200		Hz
PWM_FREQ_MAX	PWM maximum frequency			1400		Hz
PWM_FREQ_ACC	PWM frequency accuracy		-5		5	%
PWM_PHASE_SHIFT_MIN	PWM minimum phase shift - consumer mode			0		µs
PWM_PHASE_SHIFT_MAX	PWM maximum phase shift - consumer mode			105		µs
PWM_PHASE_SHIFT_STEP	PWM phase shift step - consumer mode			15		µs
$t_{PWM\_ON\_OFF}$	Minimum PWM on-time and off-time vs frequency	PWM_FREQ = 200 Hz	5			µs
		PWM_FREQ = 300 Hz	3.3			µs
		PWM_FREQ ≥400 Hz	2.5			µs
$t_{STARTUP\_PWM\_VS}$	Start-up time for light function availability - PWM dimming through power line	Device in fail-safe DIN_MAP_CHx = 01 (all outputs mapped to direct input) DIN connected to power supply = 12.5 V through resistor divider CURR_SET_GROUP_X = TBD (all outputs current set to TBD mA) Power supply dimming frequency = 200 Hz power supply dimming duty cycle = 50%			700	µs

Table 64. NTC derating start configuration - voltage vs temperature

Bit 2	Bit 1	Bit 0	Derating start temp. [°C]	V_{NTC_TH} [V]
0	0	0	55	2.034
0	0	1	60	1.908
0	1	0	65	1.783
0	1	1	70	1.66
1	0	0	80	1.423
1	0	1	90	1.207
1	1	0	95	1.106
1	1	1	100	1.013

Figure 40. NTC circuitry



VNTC_TH is the NTC voltage (V_{NTC}) corresponding to the derating start temperature

$R_{pull-up}$ = 2.2 kΩ, NTC = 10 kΩ ±1%, at 25 °C.

NTC part number: NCU18XH103F6SRB

NTC chip type temperature characteristics: B-constant = 3380 K ±0.7%

7.6 Digital timings, digital I/O and ADC characteristics

Table 65. Digital timings

Symbol	Parameter	Test conditions		Min.	Typ.	Max.	Unit
t_{WD}	Watchdog timeout period	Guaranteed by scan	00(default)	45	50		ms
			01	90	100		
			10	180	200		
			11	22.5	25		
$t_{AUTORESTART}$	Auto-restart time in fail-safe/stand-alone mode	Guaranteed by scan		45	50	55	ms
t_{FILTER}	Filtering time - Time needed for DIN overtaking control on bus mode (after DIN rising edge when DIN_EN set in bus mode)	Guaranteed by scan			32		µs
$t_{BUS\_CONTROL}$	Timeout for bus control re-activation after last falling edge on DIN	Guaranteed by scan			10		ms
t_{RX_IDLE}	Timeout for RX pin in recessive state				550		µs
t_{WAKE_UP}	Time for a complete wake up (V_{3V3} > $V_{3V3\_POR\_H}$)	DIN high for t > t_{WAKEUP} Cap on V_{3V3} = 1 µF V_{3V3} > $V_{3V3\_POR\_H}$			30		µs
t_{STDBY}	Time needed for a transition to standby mode (V_{3V3} < $V_{3V3\_POR\_L}$)	DIN low Cap on V_{3V3} = 1 µF V_{3V3} < $V_{3V3\_POR\_L}$			15		ms
$t_{STARTUP}$	Time needed for the transition from the initialization to standby phase - transition state, V_S > $V_{S\_POR\_H}$	Guaranteed by scan				500	µs
t_{POR_DELAY}	Time needed after POR, before configuring the device (all outputs kept off during this time)	Guaranteed by scan	00		0		ms
			01		25		
			10		50		
			11		100		
$t_{DIAG\_BLANK\_GROUP\_X}$	Blanking time - for diagnostic validation	Guaranteed by scan	00		5		us
			01		10		
			10		15		
			11		20		
t_{FTP_WR}	FTP memory writing time	Guaranteed by scan			12		ms
t_{DIN_FALL}	DIN falling edge settling time - for fault clearing	Guaranteed by scan			10		ms

Note: Digital timings guaranteed by scan.

Table 66. ADC characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit
ADC_{RES}	ADC resolution		8		bit
ADC_{CONV_TIME}	ADC conversion time		1.6		µs
ADC_{FS_VOUTx}	ADC full scale for V_{OUTx}		20		V
ADC_{STEP_VOUTx}	ADC step for V_{OUTx}		78.4		mV
ADC_{FS_VPREG}	ADC full scale for V_{PREG}		20		V
ADC_{STEP_VPREG}	ADC step for V_{PREG}		78.4		mV
ADC_{FS_VS}	ADC full scale for V_S		40		V
ADC_{STEP_VS}	ADC step for V_S		157		mV
ADC_{FS_VNTC}	ADC full scale for V_{NTC}		2.5		V
ADC_{STEP_VNTC}	ADC step for V_{NTC}		10		mV
ADC_{FS_TJ}	ADC full scale for T_J		2.5		V
ADC_{STEP_TJ}	ADC step for T_J		10		mV
ADC_{GAIN_ERR}	Full path gain error for measurements via V_{OUTx}, V_{PREG}, V_S, V_{NTC}	TBD		TBD	%
$ADC_{INTRINSIC\_ACCURACY}$	ADC reading accuracy for NTC, T_J - including offset, INL, DNL	-3		3	LSB
$ADC_{VOLTAGE\_ACCURACY}$	ADC reading accuracy for V_{OUTx}, V_{PREG}, V_S - including offset, INL, DNL	-6		6	LSB

Table 67. Digital I/O characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DIN_L} V_{FAULT_L} $V_{SYNC\_IO\_L}$ V_{CS_L}	Low logic level			0.3 * V_{3V3}	V
V_{DIN_H} V_{FAULT_H} $V_{SYNC\_IO\_H}$ V_{CS_H}	High logic level	0.7 * V_{3V3}		V_{3V3}	V
R_{PullUp_FAULT}	FAULT pin - integrated pull up resistor		500		kΩ
I_{FAULT}	FAULT pin - sinking current (FAULT active low)			10	mA
R_{ON_FAULT}	FAULT pin - open drain NMOS RDSon (FAULT active low)			100	Ω
$ILEAK_{FAULT}$	FAULT pin - open drain NMOS leakage (no FAULT active)			1	µA

7.7 CAN FD light compatible - external shared transceiver interface pins

This section describes the electrical characteristics of the interface pins to an external stand-alone shared transceiver: RX input pin, TX and STB output pins.

RX input pin

Table 68. RX input pin

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{RXLOW}	Input voltage dominant level threshold	1.0	1.45	(2.0)	V
V_{RXHIGH}	Input voltage recessive level threshold	(1.2)	1.85	2.3	V
V_{RXHYS}	VRXHIGH-VRXLOW	0.2	0.4	0.6	V
R_{RXPU}	RX pull up resistor	20	60	110	kΩ
C_{RX}	RX Input capacitance; guarantee by design			5	pF

TX output pin

The TX pin is an open drain output, which also actively pulls high (recessive) during data transmission, except for the ACK delimiter.

Table 69. TX output pin

Symbol	Parameter	Operating condition	Min.	Typ.	Max.	Unit
V_{TXLOW}	Output voltage dominant level	Active mode, I_{TX} = 5.6 mA	0.05	0.2	0.5	V
V_{TXHIGH}	Output voltage recessive level	Active mode, I_{TX} = -2 mA	V_IO -0.5	V_IO -0.2	V_IO - 0.05	V
$t_{r,TX}$	TX rise time; guarantee by design	C_L = 50 pF, 30% - 70% V_{TX}			25	ns
$t_{f,TX}$	TX fall time; guarantee by design	C_L = 50 pF, 70% - 30% V_{TX}			25	ns
C_{TX}	TX utoput capacitance; guarantee by design				5	pF

STB output pin

The STB pin is a programmable open-drain pin which is either actively pulling high or low.

Table 70. STB output pin

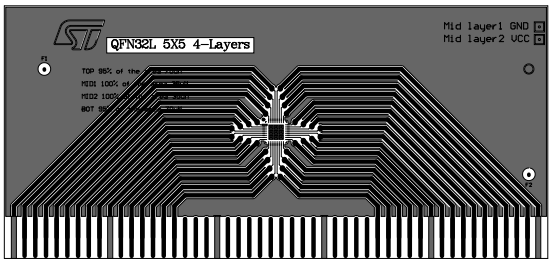
Symbol	Parameter	Operating condition	Min.	Typ.	Max.	Unit
$V_{STBHIGH}$	Output voltage high level	Active mode, I_{STB} = -2 mA; when actively pulling low	V_IO-0.5	V_IO -0.2	V_IO - 0.05	V
V_{STBLOW}	Output voltage low level	Active mode, I_{STB} = 2 mA; when actively pulling high	0.05	0.2	0.5	V
$t_{r,STB}$	STB rise time (1)	C_L = 50 pF, 30% - 70% V_{STB}			250	ns
$t_{f,STB}$	STB fall time (1)	C_L = 50 pF, 70% - 30% V_{STB}			250	ns

1. *Guarantee by design.*

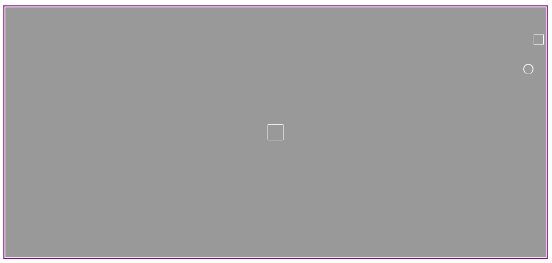
8 Package and PCB thermal data

8.1 QFN32L thermal data

Figure 41. **QFN32L on four-layers PCB**

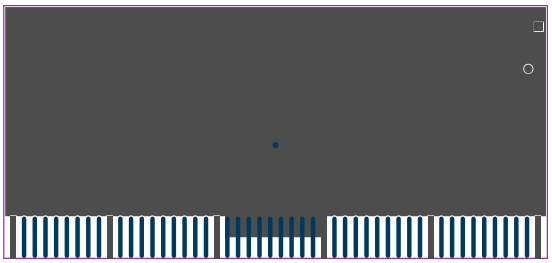


Top layer: 95% of the area



Cu on mid1 layer: 1% of the area

Cu on mid2 layer: 1% of the area



Bottom layer: 95% of the area

Table 71. **PCB properties**

Dimension	Value
Board finish thickness	1.6 mm ±10%
Board dimension	129 mm x 60 mm
Board material	FR4
Copper thickness (outer layers)	0.070 mm
Copper thickness (inner layers)	0.035 mm
Thermal vias separation	1.2 mm
Thermal via diameter	0.3 mm ±0.08 mm
Copper thickness on vias	0.025 mm

9 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

9.1 QFN32L 5x5 mm package information

Figure 42. QFN32L 5x5 mm package outline

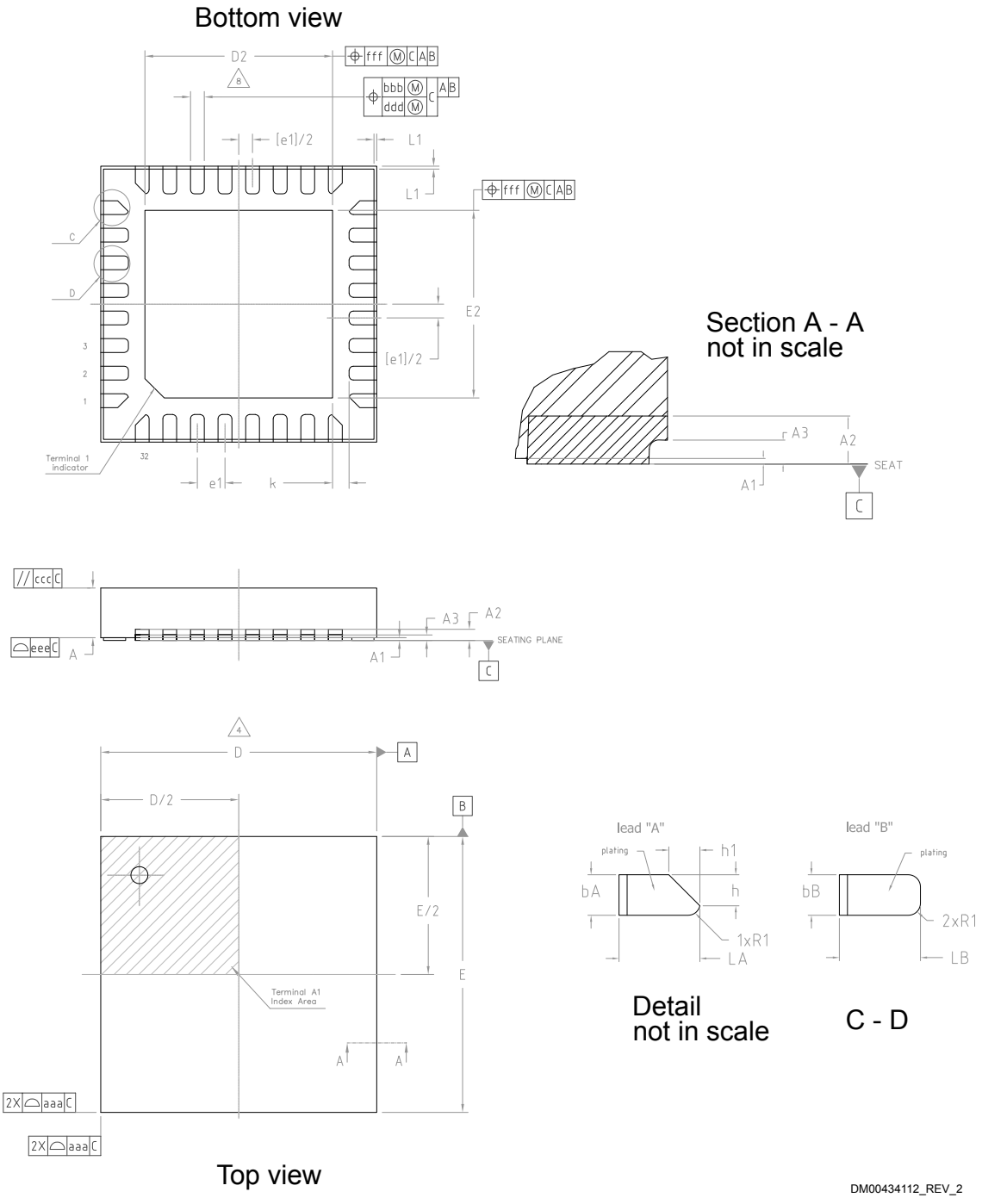


Table 72. **QFN32L 5x5 mechanical data**

Ref.	Dimension		
	Millimeters		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1	0		0.05
A2		0.2 REF	
A3	0.1		
D		5.00 BSC	
D2	3.40	3.50	3.60
E		5.00 BSC	
E2	3.40	3.50	3.60
e1		0.5 BSC	
k	0.20		
L1			0.05
La	0.40	0.50	0.50
bA	0.20	0.25	0.30
h		0.19 REF	
h1		0.19 REF	
LB	0.45	0.5	0.55
bB	0.20	0.25	0.30
N		32	
R1			0.1

Table 73. **Tolerance of form and position**

Symbol	Tolerance
aaa	0.15
bbb	0.10
ccc	0.10
ddd	0.05
eee	0.08
fff	0.10

Revision history

Table 74. **Document revision history**

Date	Revision	Changes
19-Oct-2022	1	Initial release.
01-Mar-2024	2	Updated: *Section Features; Figure 2. Functional block diagram;Table 1. Pin list description; Section 3.1: General descriptionSection 3.3: Channel driver drop-out voltage; Section 3.3: Channel driver drop-out voltage ; Section 4.3.5: LED current derating;Section 4.3.7: Channel output – LED short circuit detection; Section 5.1: External CAN transceiver ; Section 5.1: External CAN transceiver; Table 2. Minimum channel drop-out voltage at maximum current vs T_J; Table 61. Supply; Table 68. RX input pin; Table 69. TX output pin; Table 70. STB output pin.* Added: *Section 6.2.1: Device FTP configuration - Row 0; Section 6.2.2: Device FTP configuration - Row 1; Section 6.2.3: Device FTP configuration - Row 2; Section 6.2.5: Device FTP configuration - Row 11; Section 6.2.6: Device FTP configuration - Row 12.*
30-May-2024	3	Added *Section 5.7.11: Unicast CAN FD frame - FTP read* and *Section 5.7.12: Unicast CAN FD frame - FTP write*. Updated *Table 51. Row 0, Table 52. Row 1* and *Table 53. Row 2*. Minor text changes.
20-Sep-2024	4	Updated *Section Features* on cover page. Updated *Table 62. Output characteristics*, *Section 5.4.5: Error handling*, *Table 65. Digital timings*, *Table 69. TX output pin* and *Table 70. STB output pin*. Minor text changes.
08-Nov-2024	5	Updated Section Features on cover page.

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