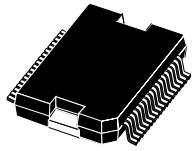
LEOPOL1

Datasheet

Rad-hard 5 A step-down converter in plastic package



PowerSO-36

Connected slug-down

Maturity status link
LEOPOL1

Features

- Operating input voltage from 3 V to 12 V
- Output current @ 5.5 V up to 62 MeV.cm²/mg: 5 A
- Output voltage range: 0.8 V to 0.85 x Vin
- Configurable soft-start
- Current sharing with multiple devices
- Out-of-phase synchronization
- Full protection set: overtemperature, overcurrent, overvoltage
- Undervoltage lockout
- High dissipation PowerSO-36 package: R_{thjc} < 2 °C/W
- Operating temperature range: -40 to +125 °C
- Compliant with ST's LEO specification, including
  - Wisker free Nickel/Palladium/Gold lead finishing
  - Gold wires
  - Characterized outgassing: RML < 1% - CVCM < 0.1%
- Target radiation performance:
  - 50 krad(Si) Total Ionizing Dose
  - TNID immune at 3.10^{11} proton/cm²
  - SEL free up to 62 MeV.cm²/mg

Applications

- Power management in satellites for Low Earth Orbit (LEO)
- FPGA, MPU, ASIC, and MCU power supply
- Power management in radiative and other harsh environments

Description

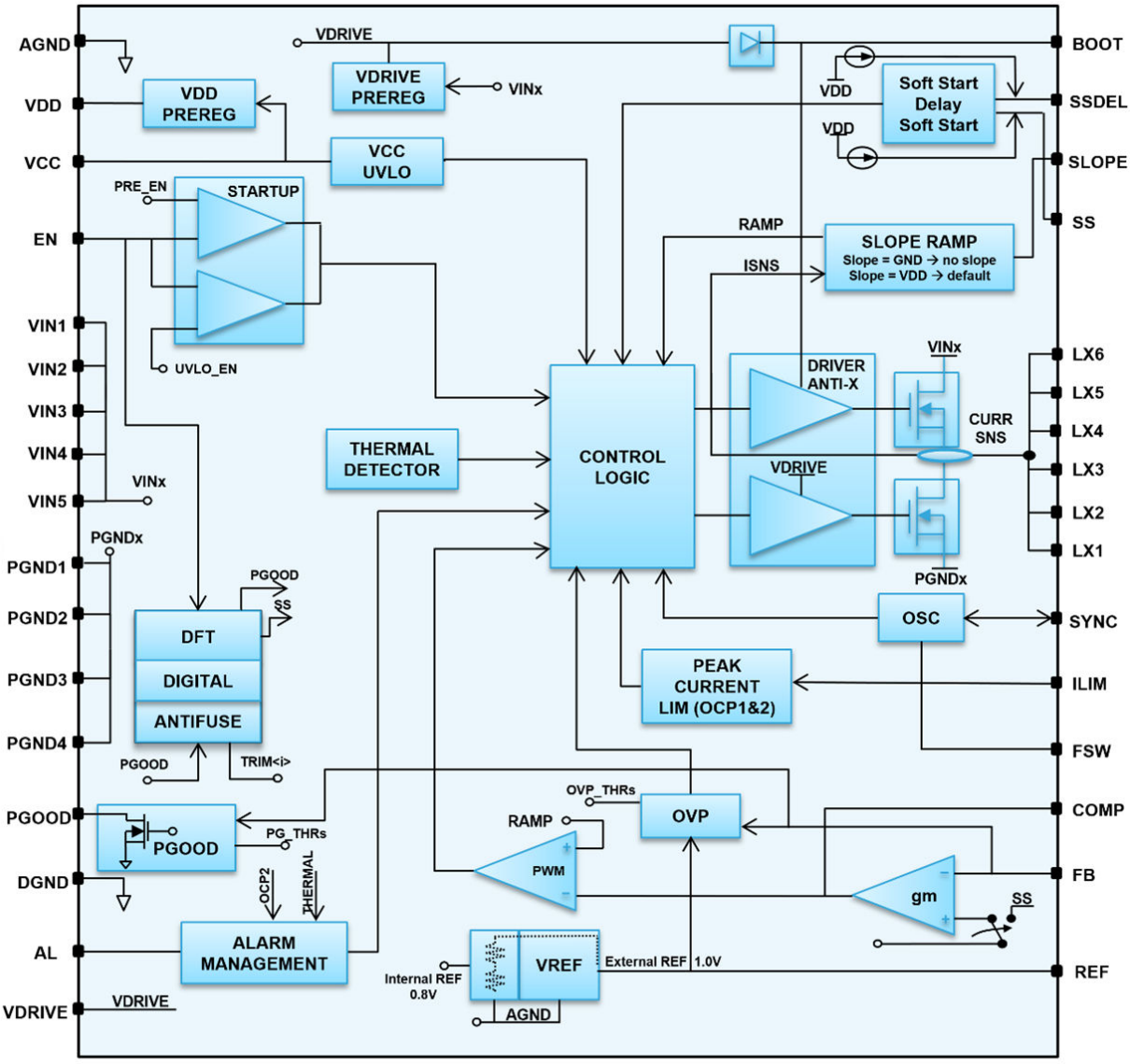
The LEOPOL1 is a single-phase, step-down monolithic switching regulator with high-precision internal voltage reference and integrated power MOSFETs for synchronous conversion able to provide, at ground level (no single effect events), up to 7 A with up to 12-volt power supply, and up to 5 A from a 5.5 volt supply in a radiative environment up to 62 MeV.cm²/mg.

The LEOPOL1 can operate over a large temperature range of -40 °C to +125 °C. Designed using a BCD Silicon-On-Insulator (SOI) technology, it features an intrinsic radiation hardness, further enhanced through hardening by design, optimized to meet the radiation hardness required for Low Earth Orbit space crafts at an effective cost. Its PowerSO-36 package features a slug-down pad allowing a very low thermal resistance for a superior dissipation including in the absence of convection. It uses golden bonding and NiPdAl-lead-finishing to prevent whiskers. It complies with ASTM-E-595 and ESCC-Q-ST-70-02C outgassing standards for parts to be used in a vacuum.

The LEOPOL1 is compliant with the ST LEO generic specification, for space-ready rad-hard plastic products. This AEC-Q100 based specification offers radiation hardness and the capability to support large quantities, together with a trade-off optimized for LEO space crafts between quality assurance and cost of ownership (details on the ST LEO generic specification can be found in TN1432).

1 Diagram

Figure 1. **Block diagram**



2 Pin configuration

Figure 2. **Pin out (top view)**

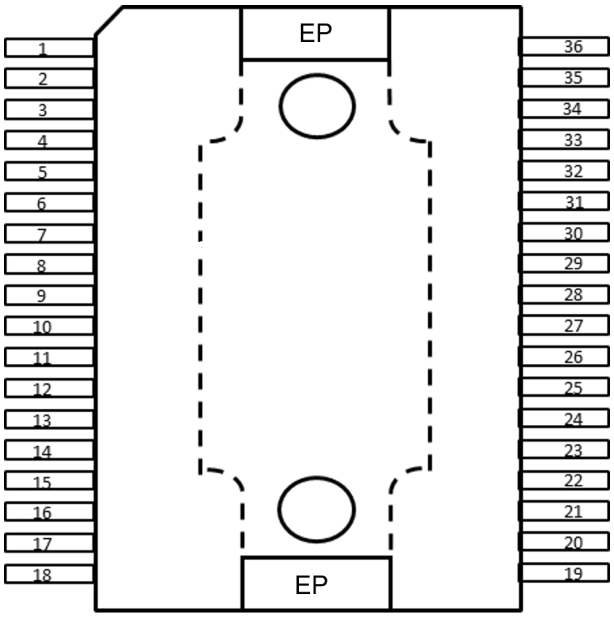


Table 1. **Pin description**

Pin N°	Symbol	Description
1	EP	Slug down exposed pad. Pin 18, 19, and 36 are also connect to it. The exposed pad should be connected to PGND to maximize disspation.
2	AGND/DGND	Signal ground. This is the ground for IC control loop, bias, and internal voltage reference. Connect to PCB ground plane through multiple vias.
3	VDD	IC internal supply output. Bypass to GND with a 1 µF ceramic capacitor. Maximum load allowed on this pin is 100 µA. No current injection is allowed.
4	VCC	Filtered input power for control circuitry. Filter and bypass to GND with 4.7 Ω - 1 µF R-C network.
5	EN	Enable pin, active high.
6, 7, 8, 9, 10	VIN	Power supply input. Bypass to PGND close to the IC package with capacitors with a low ESR (MLCC 3 x 47 µF + 2 x 10 µF is suggested).
11, 12, 13, 14	PGND	Power ground. This is the reference ground for the internal power MOSFET's driver and VIN input rail. Connect to PCB ground plane through multiple vias.
15	PGOOD	Power Good signal, open drain. Pulled up to VIN or lower rail. This pin goes to a high state if VOUT stays inside +/-10% of target output voltage.
16	AL	Alarm pin. Bypassing to GND with a capacitor provides a timing alarm window proportional to capacitor value.
17	VDRIVE	Internal generated and filtered rail for power MOS driver supply of the low-side and the high-side through bootstrap capacitor. One external capacitor (1 µF) is required. Maximum load allowed on this pin is 100 µA. No current injection is allowed.
18, 19	EP	Slug down exposed pad. Pin 1 and 36 are also connect to it. The exposed pad should be connected to PGND to maximize disspation1
20	REF	Control loop voltage reference. Bypass to GND with a ceramic capacitor (1 µF). Maximum load allowed on this pin is 100 µA. No current injection is allowed.
21	FB	Remote sensing input pin. Connect to the central tap of a resistor divider between VOUT and GND in order to program the output voltage level.

Pin N°	Symbol	Description
		Maximum load/sink allowed on this pin is 1 µA.
22	COMP	Loop compensation pin. Connect to GND through an R-C network, for loop compensation.
23	FSW	Switching frequency programming pin. Connect FSW to GND through a resistor RFSW (and optional capacitor < 1 nF for filtering purposes). Connect to GND for slave mode operation (refer to SYNC pin description). Pull up to VDD or higher rail (3.6 V max.) to set default frequency (500 kHz).
24	ILIM	First and second level current limit thresholds programming. ILIM1 and ILIM2 can be adjusted through a single resistor. Connect ILIM to GND through a resistor to program a current limit ILIM1 lower than 10 A and ILIM2 = (1.3* ILIM1). An optional capacitor < 1 nF can be connected for filtering purposes in parallel to resistor. Pull up to VDD or higher rail (3.6 V max.) for ILIM1 = 10 A and ILIM2 = 13 A (typ.).
25	SYNC	Synchronization clock input (slave mode) or output (master mode) for 2 ICs' synchronization. Max. allowed capacitive load (equivalent) for slave devices is 150 pF.
26, 27, 28, 29, 30, 31	LX	Regulator switching node. Connect directly to the inductor.
32	SS	Soft-start programming pin. Connect to GND through a ceramic capacitor in order to program the proper turn-on timing.
33	SLOPE	Current sensing additional ramp programming. Connect to GND through a resistor (and capacitor < 1 nF for filtering purposes) for control loop compensation tuning. Pull up to VDD or higher rail (3.6 V max.) to enable the internal default slope compensation.
34	SSDEL	Soft-start delay programming pin. A capacitor must be connected between this pin and GND to program the switching regulator turn-on delay.
35	BOOT	Bootstrap pin. It provides a power supply for the floating high-side driver. Connect to LX through a bootstrap capacitor (100 nF suggested).
36	EP	Slug down exposed pad. Pin 1, 18 and 19 are also connect to it. The exposed pad should be connected to PGND to maximize dissipation.

3 Application circuit

Figure 3. **Typical application diagram**

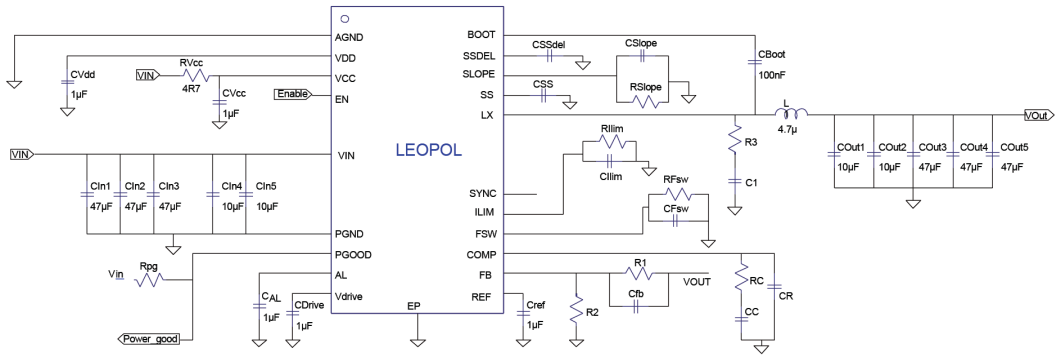


Table 2. **External components**

Reference	Description	Suggested P/N
L	Inductance, 4.7 µH, low DCR	
C_{in1}, C_{in2}, C_{in3},	Capacitor, 47 µF, 25 V, Ceramic low ESR	GRM32ER61C476KE15L
C_{in4}, C_{in5}	Capacitor, 10 µF, 25 V, Ceramic low ESR	GRM32ER71H106KA12L
C_{out1}, C_{out2}	Capacitor, 10 µF, 25 V, Ceramic low ESR	GRM32ER71H106KA12L
C_{out3}, C_{out4}, C_{out5}	Capacitor, 47 µF, 25 V, Ceramic low ESR	GRM32ER61C476KE15L
C_{drive}, C_{Vdd}	Capacitor, 1 µF, 6.3 V, Ceramic low ESR	
C_{Vcc}	Capacitor, 1 µF, 25 V, Ceramic low ESR	
C_{SSdel}, C_{SS}	Capacitor, 10 nF ÷ 1 µF, 6.3 V, Ceramic	
C_{Slope}	Capacitor, 1 nF or less, 6.3 V, Ceramic (optional)	
C_{Ilim}	Capacitor, 1 nF or less, 6.3 V, Ceramic (optional)	
C_{Fsw}	Capacitor, 1 nF or less, 6.3 V, Ceramic (optional)	
C_{fb}	Capacitor, 100 pF ÷ 10 nF, 25 V, Ceramic	
C_{ref}	Capacitor, 1 µF, 6.3 V, Ceramic	
C_{boot}	Capacitor, 100 F, 6.3 V, Ceramic	
C_C	Capacitor, 4.7 nF, 6.3 V, Ceramic	
C_R	Capacitor, 15 pF, 6.3 V, Ceramic	
R_{Vcc}	Resistor, 4.7 Ω, ¼ W, 5%,	
R_{PG}	Resistor, > 4.7 kΩ, ¼ W, 10%,	
R_{SLOPE}	Resistor, 15 kΩ, ¼ W, 5%,	
R_{Ilim}	Resistor, ¼ W, 5% or less	
R_{Fsw}	Resistor, ¼ W, 5% or less	
R_1	Resistor, ¼ W, 5% or less	
R_2	Resistor, ¼ W, 5% or less	
R_C	Resistor, 27 Ω, ¼ W, 5% or less	

4 Maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DD}	Internal supply voltage	AGND - 0.3 to AGND + 3.6	V
V_{IN}	Power supply voltage	PGND - 0.3 to PGND + 15	V
V_{CC}	Analog supply voltage	AGND - 0.3 to AGND + 15	V
V_{DRIVE}	Power MOS driver supply voltage	AGND - 0.3 to AGND + 3.6	V
V_{EN}, V_{SYNC}, V_{SS}, V_{SSDEL}, V_{SLOPE}, V_{ILIM}, V_{COMP}, V_{FB}	Signal pins	AGND - 0.3 to AGND + 3.6	V
V_{BOOT}	Boot pin voltage (VBOOT-VLX)	PGND - 0.3 to PGND + 18	V
V_{LX}	Switching node	PGND - 0.3 to VIN + 0.3	V
V_{PG}	Power Good pin voltage	AGND - 0.3 to VCC + 0.3	V
V_{REF}	Reference voltage	AGND - 0.3 to AGND + 3.6	V
T_{JMAX}	Absolute maximum junction temperature	175	°C
V_{HBM}	ESD capability, human body model	2 K	V
T_{STG}	Storage temperature range	-40 to +150	°C
T_{OP}	Operating junction temperature range	-40 to +125	°C

Table 4. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance junction-case	2	°C/W
R_{thJA}	Thermal resistance junction-ambient (2s2p Jedec board)	25	°C/W

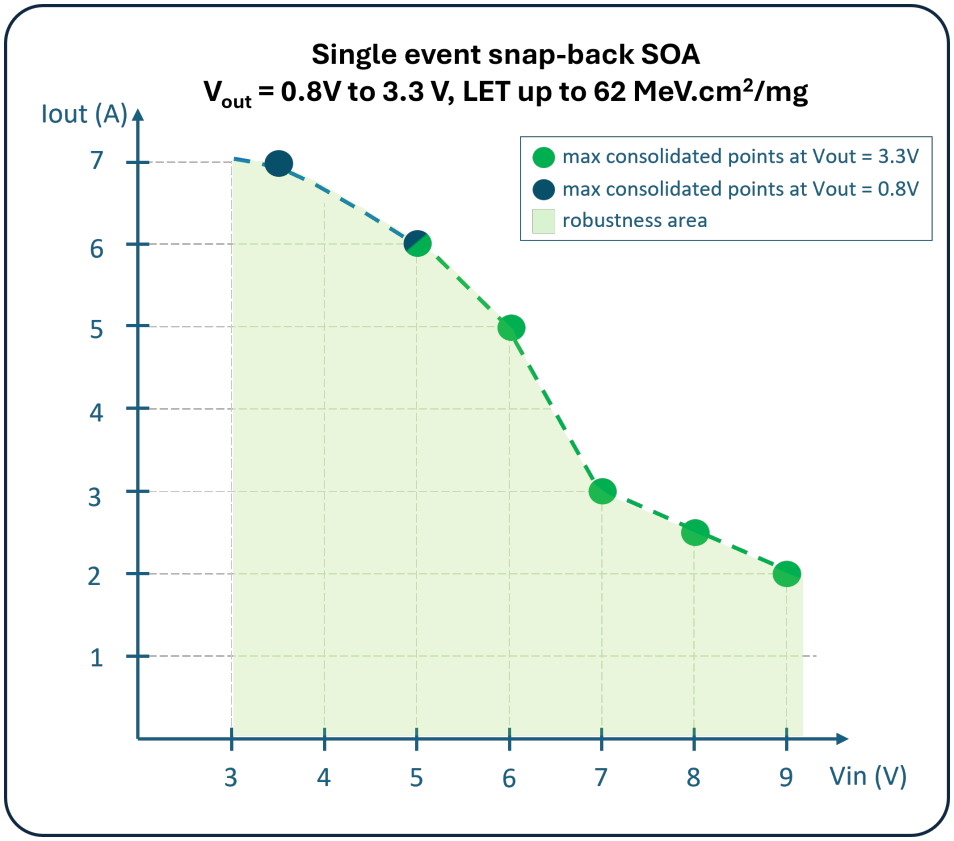
Table 5. Recommended operating conditions

Symbol	Parameter	Value			Unit
		Min.	Typ.	Max.	
V_{IN}, V_{CC}	Input voltage range	3.0		12 (1)	V
V_{OUT}	Output voltage range	0.8		V_{CC} x 0.85	V
V_{FSW}	Default frequency mode		VDD		V
	Slave mode		GND		V
R_{FSW}	Programmed frequency mode	50		500	kΩ
V_{SLOPE}	Default slope compensation		VDD		V
P_D	Dissipated power			TBD	W
I_{OUT}	Output current			7 (1)	A
T_{AMB}	Operating ambient temperature	-40		125	°C
F_{SW}	Switching frequency	100		1000	kHz

1. *Check SOA for max. value under SEE.*

The LEOPOL1 provides up to 7 A and up to 12 V in a non-radiative environment. Figure 4 provides the safe operation area (SOA) of the product operation under 62 MeV.cm^2/mg particles.

Figure 4. LEOPOL1 SEL SOA



5 Electrical characteristics

Table 6 provides the complete pre-rad electrical characteristics. Unless otherwise reported in Table 7, these pre-rad data fully apply up to 50 krad(Si).

Conditions: Unless otherwise specified, $T_J = T_A = 25$ °C, $V_{IN} = V_{CC} = 5$ V, $V_{OUT} = 2.5$ V, $I_{OUT} = 3$ A, $F_{SW} = 500$ kHz, $C_{IN} = C_{OUT} = 3 \times 47$ µF ceramic low ESR + 2 x 10 µF ceramic low ESR, L = 4.7 µH, pre-radiation.

Table 6. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Supply collection						
V_{FB} (1) (2)	Feedback voltage			0.8		V
	Initial accuracy		-1		+1	%
	Temperature drift	-55 °C < T_J < +125 °C	-1.25		+1	%
I_Q	I_{VCC} + I_{VIN} quiescent current	EN = 1 V (no switching)	2.5	3.5	4.5	mA
I_{SHDN}	IVCC+IVIN shutdown current	EN = GND	250	400	550	µA
V_{CC_UVLO}	VCC undervoltage lockout upper threshold	Rising edge, device disabled below this level	2.65	2.85	3.05	V
	VCC undervoltage lockout lower threshold	Falling edge, device enabled above this level	2.45	2.65	2.85	V
	UVLO hysteresis			200		mV
Efficiency	Power efficiency	L = 2.2 µH, DCR = 6 mΩ		92		%
Switching frequency and synchronization						
F_{SW}	Default switching frequency	Voltage on F_{SW} > 2 V		500		kHz
		Initial accuracy	-10		+10	%
		Temperature drift, -55 °C < T_J < +125 °C	-10		+12	
F_{SWP}	Programmable switching frequency	R_{FSW} connected	100		1000	kHz
		Initial accuracy, R_{FSW} = 50 kΩ	450	500	550	kHz
		Temperature drift, -55 °C < T_J < +125 °C	-10		+12	%
V_{FSW}	Voltage on FSW pin	R_{FSW} connected		1		V
V_{SYNC_HI}	Sync HIGH input threshold	V_{FSW} < 0.1 V (slave configuration)	2.3			V
V_{SYNC_LOW}	Sync LOW input threshold				1	
V_{SYNC_OUT}	Sync output voltage high level	R_{FSW} connected (master configuration)		VDD		V
	Sync output voltage low level				0.4	V
	Sync output fan-out			1		mA
On-time						
$T_{ON,MIN}$	Minimum on-time			120		ns
Internal supply voltages, soft-start						
V_{REF} (2)(3)	Switching regulator reference voltage level			1		V
		Initial accuracy	-1.5		+1.5	%
		Temperature drift, -55 °C < T_J < +125 °C	-2		+2	%

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SSDEL}	Soft-start delay capacitor charging current		90	100	110	µA
V_{SSDEL_THR}	Soft-start delay voltage threshold	Delay time starts from EN > 0.7 V	0.9	1	1.1	V
I_{SS}	Soft-start capacitor charging current		45	50	55	µA
V_{DD} (3)	Internal supply bus voltage		2.6	2.7	2.8	V
V_{DRIVE} (3)	Power MOS driver supply voltage		2.85	2.95	3.1	V
Current limit						
I_{LIM1}	Default first level OCP	ILIM pin to V_{DD}		10		A
	Programmed first level OCP	Initial accuracy, R_{ILIM} = 75 kΩ	0.99	1.1	1.21	A
		Temperature drift, -55 °C < T_J < +125 °C	-20		+18	%
		Initial accuracy, R_{ILIM} = 33 kΩ	2.7	3	3.3	A
		Temperature drift, -55 °C < T_J < +125 °C	-5		+5	%
I_{LIM2}	Default second level OCP	I_{LIM} pin to V_{DD}, initial tolerance		13		A
	Programmed second level OCP	Initial accuracy, R_{ILIM} = 75 kΩ	1.21	1.43	1.70	A
		Temperature drift, -55 °C < T_J < +125 °C	-20		+25	%
		Initial accuracy, R_{ILIM} = 33 kΩ	3.5	3.9	4.3	A
		Temperature drift, -55 °C < T_J < +125 °C	-5		+5	%
V_{ILIM}	Voltage on ILIM pin	I_{LIM} programmed by external resistor	0.97	1	1.03	V
High-side and low-side integrated MOSFET						
$R_{DSon,HS}$	High-side MOS on-resistance	I_{OUT} = 1 A	10	25	30	mΩ
$R_{DSon,LS}$	Low-side MOS on-resistance		10	25	30	mΩ
Overvoltage protection and Power Good signal						
V_{OVP},T_H	OVP threshold	Initial accuracy, referred to V_{FB} = 0.8 V	0.95	1	1.05	V
	OVP reset threshold		0.78	0.85	0.92	
	OVP threshold	Temperature drift, -55 °C < T_J < +125 °C	-17		+5	%
	OVP reset threshold		-6		+18	
V_{PGOOD}	Upper rising threshold	Referred to V_{FB} = 0.8 V	106	110	115	%
	Lower falling threshold		88	90	96	
	Output voltage low level	Open drain, I_{PGOOD} = 5 mA			0.4	V
Overtemperature protection (OVP) (OTP)						
T_{OTP}	Shutdown temperature			155		°C
	Hysteresis			20		
Alarm pin (AL)						
I_{AL}	Alarm pin source/sink current	Device in fault condition		20		µA

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Enable and UVLO						
PRE_EN	Pre-enable rising threshold	Device turned ON, but not switching	0.67	0.7	0.73	V
	Pre-enable rising threshold hysteresis		0.08	0.1	0.125	
UVLO_EN	UVLO enable HIGH threshold	Device switching	1.18	1.24	1.3	
	UVLO enable hysteresis		0.1	0.2	0.3	
Enable and UVLO						
PRE_EN	Pre-enable rising threshold	Device turned ON, but not switching	0.67	0.7	0.73	V
	Pre-enable rising threshold hysteresis		0.08	0.1	0.12	
UVLO_EN	UVLO enable HIGH threshold	Device switching	1.18	1.24	1.3	
	UVLO enable hysteresis		0.1	0.2	0.3	
Slope compensation						
Slope_Comp	Voltage slope	Initial accuracy, R_{SLOPE} = 12 kΩ, F_{SW} = 500 kHz	225	250	275	mV/µs
		Temperature drift, -55 °C < T_J < +125 °C	-18		+32	%
V_{SLOPE}	Voltage at SLOPE pin	Slope programmed by external resistor		0.8		V
Error amplifier (2)						
V_{INOFF}	Input offset	F_{SW} = 500 kHz		0.3		mV
TC_{EA}	Trans-conductance	V_{COMP} = 1.35 V		0.94		mS
DCG_{EA}	DC gain	V_{FB} = 0.8 V		72		dB
I_{EA_OUT}	Output source/sink current	V_{COMP} = 1.35 V, 100 mV overdrive		220		µA
Interleaving						
I_{MATCH} (2)	Current mismatch between master and slave ICs				10	%

1. *The temperature drift refers to the measured value on the sample at T_A = 25 °C.*
2. *Specified by design and characterization - not tested in production.*
3. *Maximum load allowed on this pin is 100 µA. No current injection is allowed.*

The post-radiation limit of a few parameters is different from the pre-radiation specification. Table 7 lists these parameters and provides the limits at 50 krad(Si).

Conditions: Unless otherwise specified, $T_J = T_A = 25$ °C, $V_{IN} = V_{CC} = 5$ V, $V_{OUT} = 2.5$ V, $I_{OUT} = 3$ A, $F_{SW} = 500$ kHz, $C_{IN} = C_{OUT} = 3$ x 47 µF ceramic low ESR + 2 x 10 µF ceramic low ESR, L = 4.7 µH.

Table 7. Post radiation electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Internal supply voltages, soft-start						
I_{SSDEL}	Soft-start delay capacitor charging current		90	100	120	µA
I_{SS}	Soft-start capacitor charging current		45	50	60	µA
Current limit						
I_{LIM1}	Default first level OCP	ILIM pin to V_{DD}		10		A
	Programmed first level OCP	Initial accuracy, $R_{ILIM} = 75$ kΩ	0.88	1.1	1.21	A
		Initial accuracy, $R_{ILIM} = 33$ kΩ	2.7	3	3.3	A
Slope compensation						
Slope_Comp	Voltage slope	Initial accuracy, $R_{SLOPE} = 12$ kΩ, $F_{SW} = 500$ kHz	225	250	285	mV/µs

6 Radiation

6.1 Total ionizing dose

The LEOPOL1 is RHA guaranteed and ELDRS immune up to 50 krad(Si) as per MIL-STD-883 TM 1019 condition D.

The total ionization dose has been characterized in 2 steps:

- High and low dose rate characterization of a preliminary version of the product; in both cases on 5 biased and 5 unbiased pieces. This test has shown that the product is immune to ELDRS and that the worst-case configuration is with biased parts.
- High dose rate characterization on 5 biased parts of the final version of the product. It can be noted that:
  1. The bipolar section is identical in both versions on the LEOPOL1, allowing to support the low dose rate with the test made on the preliminary one.
  2. Only the worst-case configuration has been retested in the final version.

Unless otherwise provided in Table 7, the post-irradiation electrical and timing characteristics are the same as the pre-irradiation ones provided in Table 6.

On top of the characterization, each wafer lot is submitted to a wafer lot acceptance with a TID test at a high dose rate on 5 biased parts per wafer lot with an acceptance criterion of 0 fail.

Table 8. Total dose summary table

Type	Conditions	Result
TID	Up to 50 krad(Si) : • at / 40 krad(Si)/h) (HDR) • at 36 rad(Si)/h (LDR)	RHA guaranted and ELDRS free at 50 krad(Si)

6.2 Total non-ionizing dose

The total non-ionizing dose is tested with 50 MeV protons.

The test is performed during the product characterization and as part of the wafer lot acceptance test on 5 pieces per wafer lot with an acceptance criterion of 0 fail.

Table 9. Total non-ionization dose summary table

Type	Conditions	Result
TNID	Up to $3x10^{11}$ protons.cm² 50 MeV protons	Post TNID characteristics compliant with Table 6

6.3 Single event effect

The LEOPOL1 is characterized under heavy ions up to 62 MeV.cm^2/mg as summarized below:

- Tests performed: SESB (*), SET, SEU/SEFI
- Each test is performed on 3 samples of the final silicon in the worst-case conditions.

Table 10. SEE summary table provides the result of these tests.

Table 10. SEE summary table

Type	Conditions	Result
SESB	Test up to 62.5 MeV.cm^2/mg Temperature 25 °C Fluence: 1.10^7 ion/cm^2 Normal incidence	Immune to SESB up to 62.5 MeV.cm^2/mg
SET	Temperature 25 °C	Characterized

Single event effects are not tested in production.

(*) While components with bulk substrates may be subject to latch-up under heavy ions (low impedance path between supply and ground triggered by current injection or overvoltage), the physical phenomenon possibly observed on components with SOI substrates such as the LEOPOL1 is snap-back (transistors turned on by an avalanche breakdown or impact ionization). The test set-up to characterize both effects and their effects on components are similar, hence the common confusion between SEL and SESB. However, the worst case condition for the latter is 25 °C, while it is 125 °C for SEL.

7 Device functional description

The LEOPOL1 is a radiation hardened high efficiency synchronous step-down monolithic switching regulator capable of delivering up to 7 A continuous output current in the absence of heavy ions (refer to SOA in section 3 for maximum current supply capability with SESB immunity).

The power input voltage (V_{IN}), also in the absence of heavy ions, can range from 3 V to 12 V and, thanks to a 0.8 V internal voltage reference, the LEOPOL1 can precisely regulate the output voltage in the range of 0.8 V to 85% of V_{IN}.

Low R_{DSon} N-channel MOSFETs for both HS (high-side) and LS (low-side) and also the boot diode are embedded, for minimum external component requirement. The peak current mode control loop, with a high bandwidth error amplifier and an external compensation, enables a stable operation with a wide range of output filter configurations (including multi-layer ceramic capacitor (MLCC) solutions) ensuring a fast response to load transient. For maximum design flexibility, all the most important features are programmable.

The LEOPOL01 features a full set of protections and output voltage monitoring:

- High accuracy programmable dual level overcurrent protection (internally compensated against temperature variations)
- Overvoltage protection (not latched)
- Overtemperature protection (latched after 16 consecutive fault events)
- Undervoltage lockout on input supply rail
- Power Good open drain output, which provides real-time information about the output voltage.

The SYNC pin allows 2 devices to be synchronized with 180° phase shift switching interleaving, reducing RMS current absorption from the input filter and preventing beating frequency noise, therefore allowing a reduction in the size and cost of the input filter.

The current share configuration allows 2 devices to be easily connected, providing up to 14 A. For higher output current requirement, n devices can be connected by means of an external circuitry providing the proper 360°/n phase shifted signals.

The dedicated enable pin (EN), the programmable soft-start duration, and soft-start delay offer easy control on the power sequencing and inrush current.

The LEOPOL1 is provided in a PowerSO-36 leads plastic package.

7.1 Power section

The LEOPOL1 integrates two low on-resistance N-channel MOSFETs as low-side and high-side switches, optimized for fast switching transition and high efficiency over all the load range. The power stage is designed to deliver a continuous output current up to 7 A (in the absence of heavy ions).

The HS MOSFET drain is connected to the V_{IN} pins (power input), the LS MOSFET source is connected to the PGND pins (power ground); the HS MOSFET source and LS MOSFET drain are connected to the LX pins (see Figure 1 for details). The driving section is supplied by the V_{IN} pins through the internal voltage regulator (V_{DRIVE}) that assures the proper driving voltage over all the supply range.

Proper design should comply with the recommendations below:

- Bypass V_{IN} pins to PGND pins as close as possible to the IC package with high quality MLCC capacitors.
- Connect the bootstrap capacitor (typically a 100 nF ceramic capacitor rated to stand V_{IN} voltage) from the BOOT pin to the LX pin to supply the high-side driver.
- Do not connect an external bootstrap diode. The IC already integrates a bootstrap diode to charge the bootstrap capacitor, saving the cost of this external component.

The LEOPOL1 embodies an anti-shoot-through and adaptive deadtime control to minimize the conduction time of the low-side body diode and consequently reduce power losses.

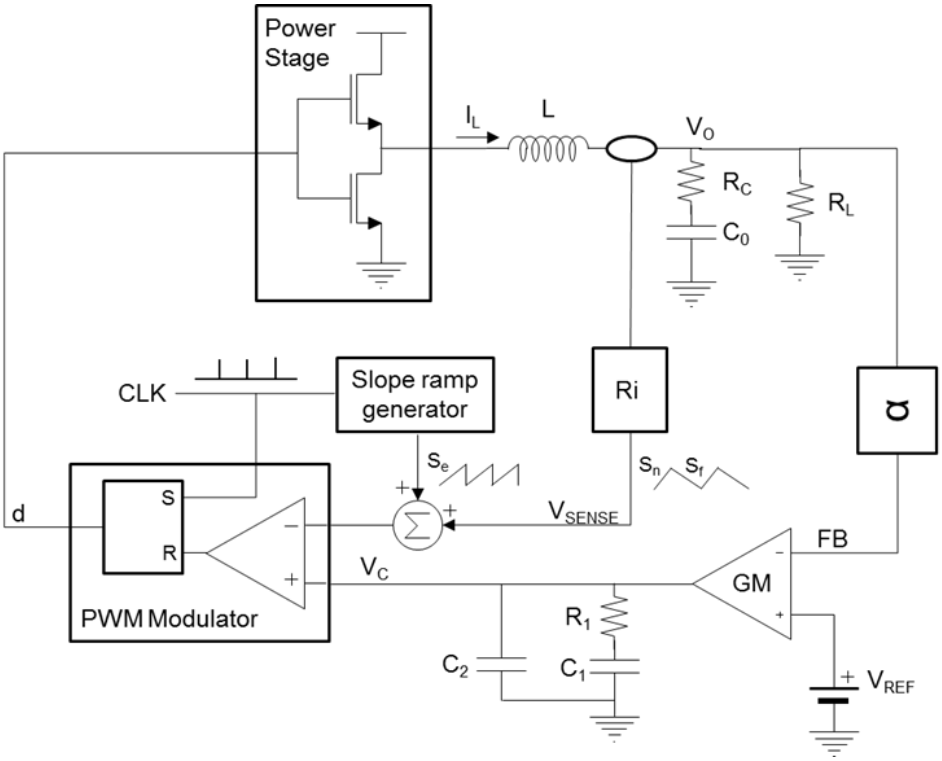
When the voltage at the LX pin drops (to check high-side MOSFET turn-off), the LS MOSFET is suddenly switched on. When the gate driving voltage of the LS drops (to check low-side MOSFET turn-off), the HS MOSFET is suddenly switched on.

The regulation stays active even if the current is negative (full PWM). In fact, if the current flowing in the inductor is negative, the voltage on the LX pin never drops. A watchdog controller is implemented to allow the LS MOSFET to turn on even in this case.

7.2 Control loop

The LEOPOL1 is a constant-frequency, peak current mode switching regulator as shown in Figure 5.

Figure 5. Peak current mode control loop model



It employs two control loops: an external loop to control the output voltage and an inner loop to control the peak current that flows through the coil. The external loop (or voltage loop) compares the feedback voltage V_{FB} with the internally generated precise reference voltage V_{REF} at 0.8 V through the error amplifier GM. The error amplifier is a trans-conductance amplifier (OTA) that multiplies the difference of input voltage by a certain gain and generates a current into the output node V_C (pin COMP).

The external compensation circuit, RC network tied between V_C and ground, converts the current generated by the error amplifier into a voltage. In the inner loop (or current loop), the current sense circuit converts the current flowing through the coil into a sense voltage V_{SENSE} with gain factor R_i (0.1 Ω). The voltages V_C and V_{SENSE} are compared by a PWM comparator and a Pulse Width Modulated (PWM) signal is generated, defining the duty cycle d. The power stage can be seen as a controlled current generator that provides the current I_L to the power stage output capacitor and load.

Finally, the voltage ramp S_e, programmable by the external R_{SLOPE} resistor, is added to the V_{SENSE} signal to stabilize the converter in case of duty cycle greater than 50% operation.

The control-to-output equivalent transfer function is described in Equation 1.

$$F(s) = \frac{V_o(s)}{V_c(s)} = \frac{R_L}{R_i} \cdot \frac{(sC_OR_C + 1)}{sC_O(R_C + R_L) + 1} \quad (1)$$

C_o and R_C are the output capacitance and its equivalent series resistance and R_o represents the output load.

In order to obtain the typical integrative loop transfer function, the signal stage must compensate for the power stage pole (due to the output capacitor and the load) and zero (above the loop bandwidth if ceramic output capacitors are selected). The signal stage transfer function is shown in Equation 2.

$$G(s) = \alpha g_m R_{OUT} \frac{(1 + R_1C_1s)}{(1 + R_{OUT}C_1s)(1 + R_1C_2s)} \quad (2)$$

where:

- g_m is the small signal gain of the trans-conductance stage
- α is the gain due to the output resistor divider (V_{REF} / V_{OUT})
- R_{OUT} is the output impedance of the amplifier (R_{OUT} ≈ 4 MΩ).

Equation 2 is calculated assuming C_1 >> C_2 and R_{OUT} >> R_1.

The external compensation network (R_1, C_1, and C_2) must be designed in order to obtain:

- One zero, matching the power stage pole (Equation 3)

Equation 3

$$C_1R_1 = C_O(R_L + R_C) \quad (3)$$

- One pole in order to delete the static output voltage error
- One pole, if necessary, matching the high frequency zero due to the output capacitor ESR, R_C (Equation 4).

Equation 4

$$C_2R_1 = C_OR_C \quad (4)$$

The resulting control loop transfer function is the product of G(s) by F(s):

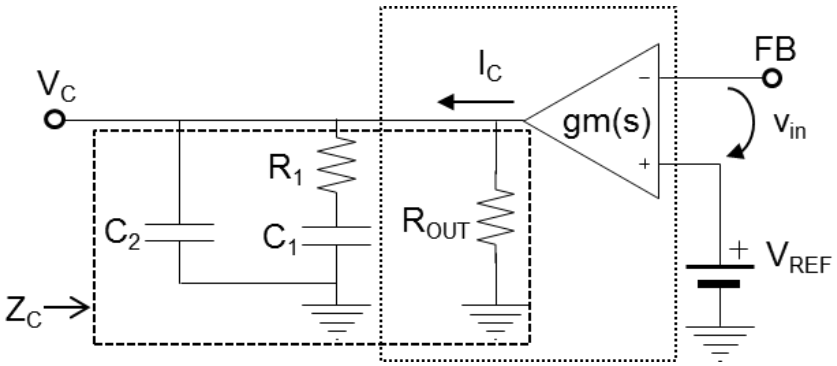
Equation 5

$$G_{LOOP}(s) = F(s)G(s) = \alpha g_m R_{OUT} \frac{R_L}{R_i} \frac{(1 + R_1C_1s)}{(1 + R_{OUT}C_1s)(1 + R_1C_2s)} \frac{(1 + R_CC_Os)}{1 + (R_C + R_L)C_Os} \quad (5)$$

This model provides good results if the control loop bandwidth is lower than about F_{SW}/10.

The error amplifier can be modeled as shown in Figure 6.

Figure 6. Simplified model of the error amplifier



It provides an output current I_C proportional to the trans-conductance gm and the input differential voltage V_{in}. The trans-conductance is a function of the frequency.

Its DC gain is given by:

Equation 6

$$A_v = gm \cdot R_{OUT} \quad (6)$$

where R_{OUT} is the output impedance of the amplifier (R_{OUT} ≈ 4 MΩ).

Finally, the transfer function of the error amplifier is given by:

Equation 7

$$\frac{V_C}{V_{in}} = gm(s) \cdot Z_C \quad (7)$$

Z_C is the equivalent impedance at the output of the error amplifier, and it can be displayed as the parallel of the output impedance and the compensation network:

Equation 8

$$Z_C = \frac{1}{C_2 s} \left\| \left(R_1 + \frac{1}{C_1 s} \right) \right\| R_{OUT} \tag{8}$$

For simplicity, the error amplifier is supposed to have a single pole, single zero at the frequency of w_{p1} and w_{z1}. Thus, its trans-conductance can be expressed as:

Equation 9

$$gm(s) = gm \cdot \frac{1 + s\frac{1}{w_{z1}}}{1 + s\frac{1}{w_{p1}}} \tag{9}$$

The typical values of w_{z1} and w_{p1} are $w_{z1} \approx 2\pi \cdot 350$ k rad/s and $w_{z1} \approx 2\pi \cdot 1.6$ M rad/s. Accurate modeling of the PWM modulator up to a high frequency is a must for a proper loop stability analysis. The linear time-invariant (LTI) model such as the Ridley model or similar is typically used for these purposes

7.3 Ridley modeling applied to LEOPOL1

A more accurate model for stability is based on the approach suggested by Ridley for a peak current mode control scheme. It is accurate up to half of the switching frequency and allows us to precisely estimate the phase margin of the complete loop.

According to the Ridley model, an extra gain $F_h(s)$, representing the high frequency correction term of the controller transfer function, must be added to the main transfer function. Thanks to this term, the sub-harmonic oscillations that appear for duty cycle values above 50% are taken into account. This extra gain comes from a second order approximation of the continuous time modeling by Ridley and is valid up to half of the switching frequency. The effect of a feedforward capacitor in the feedback net is also taken into account by α(s).

Figure 7. Global loop transfer function

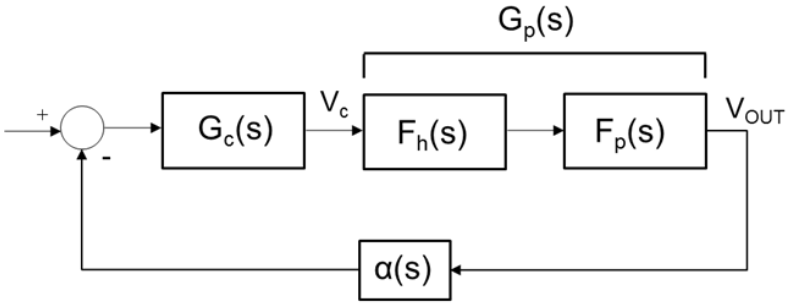


Figure 7 shows the global loop transfer function according to Ridley's modeling where:

$$G_C(s) = \frac{V_C(s)}{V_{FB}(s)} = g_m R_{OUT} \frac{1 + R_1 C_1 s}{(1 + R_{OUT} C_1 s)(1 + R_1 C_2 s)} \tag{10}$$

$$\alpha(s) = \alpha(0) \frac{1 + R_{fb1} C_{fb} s}{1 + \alpha(0) R_{fb1} C_{fb} s} \qquad \alpha(0) = \frac{R_{fb2}}{R_{fb1} + R_{fb2}} \tag{11}$$

$$F_p(s) = \frac{R_L}{R_i} \frac{1}{1 + \frac{R_L T_{SW}}{L}\left[m_c(1 - D) - 0.5\right]} \frac{1 + R_C C_O s}{1 + \frac{s}{\omega_p}} \tag{12}$$

Equation 13 (valid up to $F_{SW}/2$, high frequency correction term)

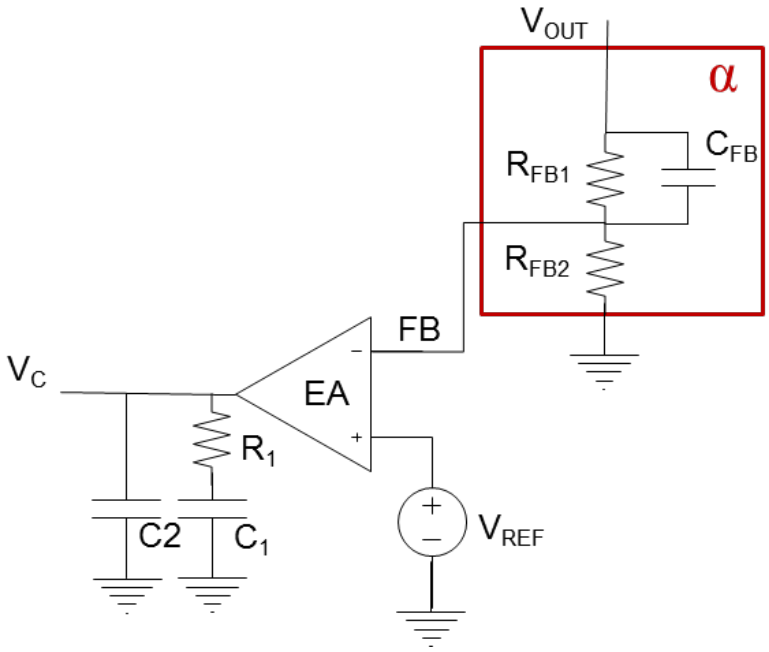
$$F_h(s) = \frac{1}{1 + \frac{s}{\omega_n Q_p} + \frac{s^2}{\omega_n^2}} \quad (13)$$

Refer to Figure 8 for $R_{FB1}/R_{FB2}/C_{FB}$ configuration. The parameters m_c, ω_n, ω_p, and Q_p can be calculated as follows:

$$\omega_p = \frac{1}{(R_L + R_C)C_O} + \frac{T_{SW}}{LC_O}\left[m_c(1-D) - 0.5\right]; \qquad Q_p = \frac{1}{\pi[m_c(1-D) - 0.5]}; \quad (14)$$

$$\boldsymbol{\omega_n = \frac{\pi}{T_{SW}} = \pi f_{SW}}; \qquad \boldsymbol{m_c = 1 + \frac{S_e}{S_n} = 1 + \frac{\frac{V_{SLOPE}}{T_{SW}}}{\frac{V_{IN} - V_{OUT}}{L} R_i}}$$

Figure 8. Feedback network with feedforward capacitor



The resulting complete open loop gain transfer function, accurate if $C_1 >> C_2$ and $R_{OUT} >> R_1$ up to $F_{SW}/2$, is:

$$G_{LOOP}(s) = \alpha(s)G_C(s)F_p(s)F_h(s) \quad (15)$$

$$G_{LOOP}(s) = \alpha(0)\frac{1 + R_{fb1}C_{fb}s}{1 + \alpha(0)R_{fb1}C_{fb}s} g_m R_{OUT} \frac{1 + R_1C_1s}{(1 + R_{OUT}C_1s)(1 + R_1C_2s)} \frac{R_L}{R_i} \frac{1}{1 + \frac{R_L T_{SW}}{L}[m_c(1-D) - 05]} \frac{1 + R_C C_O s}{1 + \frac{s}{\omega_p}} \frac{1}{1 + \frac{s}{\omega_n Q_p} + \frac{s^2}{\omega_n^2}}$$

$$G_{LOOP}(s) = G_{LOOP}(0)\frac{1 + R_{fb1}C_{fb}s}{1 + \alpha(0)R_{fb1}C_{fb}s} \frac{1 + R_1C_1s}{(1 + R_{OUT}C_1s)(1 + R_1C_2s)} \frac{1 + R_C C_O s}{1 + \frac{s}{\omega_p}} \frac{1}{1 + \frac{s}{\omega_n Q_p} + \frac{s^2}{\omega_n^2}}$$

Where:

$$G_{LOOP}(0) = g_m \alpha(0) \frac{R_{OUT} R_L}{R_i} \frac{1}{1 + \frac{R_L T_{SW}}{L}[m_c(1-D) - 05]}$$

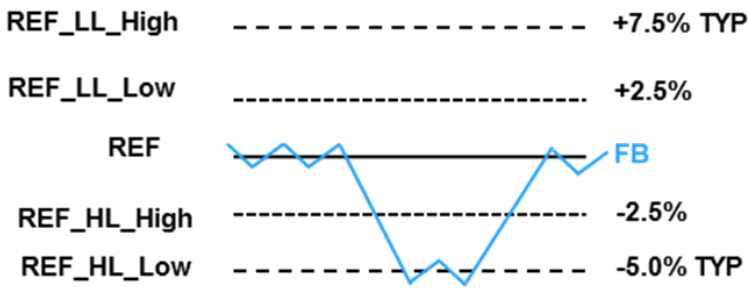
$$\alpha(0) = \frac{R_{fb2}}{R_{fb1} + R_{fb2}}$$

7.4 Fast load transient response

When fast load transient is applied to the output, the device is able to react very quickly in order to limit output voltage overshoot or undershoot. This feature is the combination of a fast error amplifier response and a proper control logic scheme that is driven by the use of two fast comparators, called HL (High Load) and LL (Low Load).

When the FB voltage goes below the REF_HL, the HL comparator forces the on-time period turning ON the power switch. Typically, REF_HL level is -5% below the nominal voltage loop reference of 800 mV. HL comparator output is latched to high level voltage until overcurrent protection occurs or the output voltage goes back again to the regulation voltage level. So, a proper voltage hysteresis is implemented: the comparator output goes low when the feedback goes back again to -2.5% of the regulation threshold (Figure 9). If during the ON-phase the current limit is reached, the minimum OFF-time period around 200 ns is applied.

Figure 9. Fast load transient response



Propagation delay time of the comparator has to be minimized to speed up device reaction to a fast step load but, once the ON-phase is triggered, the faster the coil ramp current slope, the lower the output voltage drop. For this reason, the lower inductance coil is suggested, for instance 0.8 µH is advised.

On the contrary, when the load current quickly decreases, the FB voltage can show an overshoot. The LL comparator output goes high when the FB goes above the REF_LL voltage (typically +7% above the nominal 800 mV reference) and an OFF-time is forced. The OFF-time is kept until the FB voltage goes back again to the hysteresis threshold (typically +2.5%), or the negative inductor current threshold is reached. In fact, the device naturally works in full PWM mode, but when a fast negative step load occurs, the current on the coil can quickly go below zero. Therefore, a zero-crossing comparator, with a typical threshold of -1.5 A, is implemented avoiding the inductor coil going deeply below zero. When the zero-crossing threshold is reached, the switching activity is stopped, and the power stage is forced into an open loop condition (LX is in high impedance).

The two comparators themselves are not enough to speed the loop response, but as mentioned above, also the error amplifier must be able to speed up the transient response. A fast error amplifier with dynamic bias has been designed in order to improve the load-transient response. In practice, the error amplifier must be able to quickly charge or discharge the compensation capacitor (on the COMP pin), changing its output in a non-linear shape at a step change in the input of the error amplifier itself.

So, when one of the two comparators drives the ON or OFF-time phase, bandwidth and the large signal current capability (so the large signal current gain) of the error amplifier are also increased in parallel.

Finally, this solution allows a fast load transient response with lower output capacitance with smaller output voltage drop.

7.5 Slope compensation

As well-known and documented in literature, the current mode control can produce sub-harmonic oscillations when the duty cycle d ≥ 50%. Any perturbation in the inductor current, due to fluctuations in the control loop, can persist if the converter is operating at duty cycle greater than 50%. To overcome this issue, an additional ramp is usually added to the sensed one in order to over-dump the current loop and make the regulator stable. This feature is present in the LEOPOL1 for maximum design flexibility: in order to let the LEOPOL1 control loop work properly in case of d ≥ 50%, a current slope can be programmed by the user. Adding this current slope to the sensing current ramp also makes the regulator stable in this condition.

The slope compensation ramp is programmed by connecting an external R_{SLOPE} resistor between the SLOPE pin and GND.

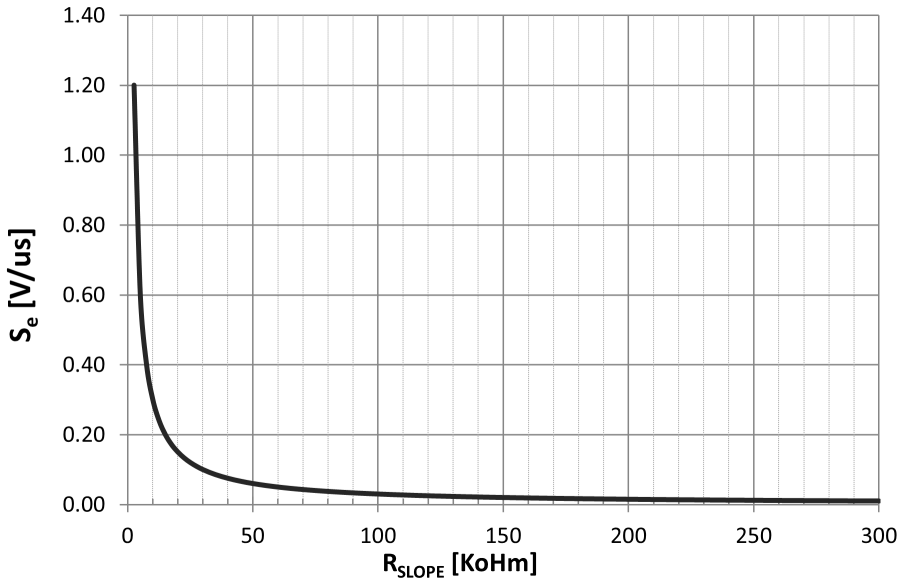
A default internal slope compensation is also implemented, and it can be enabled by pulling up the voltage on the SLOPE pin to VDD by a resistor or simply by a short.

A compact formula can be used to set the slope compensation ramp. If V_{SL_PK} is the peak value of the wanted voltage slope at the switching period T_S, the external resistor can be set as below:

$$R_{SLOPE} = \frac{3 \cdot 10e3 \cdot T_S[\mu s]}{V_{SL\_PK}[V]} = \frac{3 \cdot 10e3}{S_e\left[\frac{V}{\mu s}\right]} \quad (16)$$

where R_{SLOPE}, T_S, and the voltage slope S_e are, respectively, expressed in kΩ, µs, and Volt. Here below, for example, a graph of the voltage slope ramp versus the SLOPE pin resistor is shown, in case of a typical frequency of 500 kHz and duty cycle supposed to be 50%.

Figure 10. Slope compensation ramp vs. R_{SLOPE}, 500 kHz, d = 50%



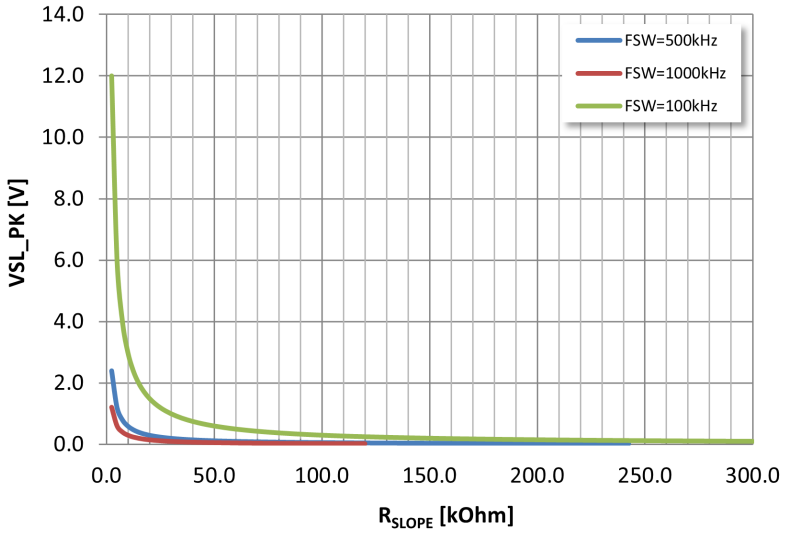
The user can therefore have maximum design flexibility. For instance, the following table summarizes the SLOPE pin programmability through the external resistor if the switching frequency is set from 100 kHz up to 1 MHz.

Table 11. Slope compensation programmability

Parameter	Description	Condition	@ $T_{ambient}$		Unit
Slope compensation programming			Min.	Max.	
V_SLOPE	Programmable slope peak voltage at Ts		0.1	1.2	V
R_{SLOPE}	External resistor range.	F_{SW} = 100 kHz	25	300	kΩ
		F_{SW} = 500 kHz	5	60	
		F_{SW} = 1 MHz	2.5	30	
S_e	Programmable slope	F_{SW} = 100 kHz	10	120	mV/µs
		F_{SW} = 500 kHz	50	600	
		F_{SW} = 1 MHz	100	1200	

Here below, for example, a graph of the voltage slope ramp peak over the SLOPE pin resistor is reported for three typical frequency values and duty cycle supposed to be 50%.

Figure 11. **Slope compensation voltage peak vs. R_{SLOPE}, d = 50%**



Concerning the default ramp, here is a compact formula as a function of the switching frequency.

$$S_{e\_DEFAULT} = V_{SL\_PK} \cdot f_{SW} = 145e + 3 \quad (17)$$

So, in the working case of a lower frequency of 100 kHz and maximum duty cycle, the maximum voltage peak on the ramp voltage due to the extra slope is supposed to be below 1.45 V.

7.6 Switching frequency setting

The regulator switching frequency can be programmed by connecting an external resistor between the FSW pin and GND.

A voltage of 1 V is present on the FSW pin, so a current of $1V/R_{FSW}$ is to be set on the resistor. This current is used to charge an internal capacitor (~20 pF). The switching frequency range of 100 kHz to 1 MHz is summarized in Table 8. R_{FSW} choice is obtained by using the following equation:

$$f_{FSW}[MHz] = \frac{1}{2*R_{SW}*20pF} = \frac{2.5 \times 10^{10}}{R_{SW}} \quad (18)$$

If the FSW pin is connected to VDD, the external programmability is turned off and the internal default frequency, tuned at 500 kHz, is enabled.

Table 12. **R_{FSW} choice**

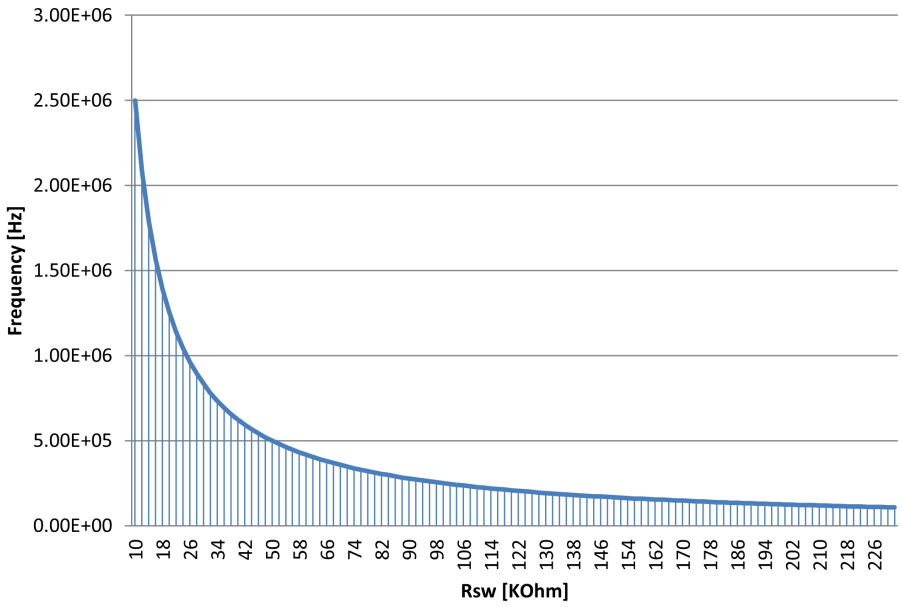
R_{FSW} [kW]	F_{SW} [kHz]
50 to 500	100 to 1000
V_{FSW} = VDD	500

To set “slave mode” configuration, the FSW pin must be shorted to ground (refer to Section 7.9 for details on Master/Slave working mode).

The internal clock is normally present to the SYNC pin with 180° phase shifting. If the device works as “MASTER” this clock is used to synchronize another device working as slave. On the contrary, if the device is set as “SLAVE” (the FSW pin shorted to ground) the SYNC pin is used as the input pin for an external clock signal, coming, for example, from another point of load used as master.

Here below, for example, a graph and the equation of the programmed frequency F_{SW} over the R_{FSW} resistor connected between the FSW pin and GND.

Figure 12. **Programmed switching frequency R_{FSW}**



7.7 Startup and soft-start

The LEOPOL1 monitors the supply voltage on the VCC pin. Once the V_{CC} voltage is above the UVLO (undervoltage lockout) rising threshold, the device waits for enable pin (EN) assertion and then begins the soft-start.

The LEOPOL1 enable pin has two thresholds in order to add flexibility to turn-on management:

- If the EN pin is kept below the PRE_EN rising threshold (0.7 V typ. with 100 mV hysteresis), the IC is fully OFF and the current consumption is typically 400 µA.
- If the EN pin is forced above the UVLO_EN rising threshold (1.24 V typ. with 200 mV hysteresis) the regulator starts switching after the SSDEL time elapses.
- If the EN pin is kept between the two above mentioned thresholds, the regulator's main blocks are turned ON (voltage reference, bias, and programming currents) and the LEOPOL1 is ready to turn on.

The filtering capacitors mounted between the functions programming pins (FSW, ILIM, and SLOPE) and GND, as shown in Figure 4, have a direct impact on the IC wake-up timing.

For this reason, to ensure that the soft-start sequence starts only when the functions programming pin voltage is stable, the soft-start delay has been added.

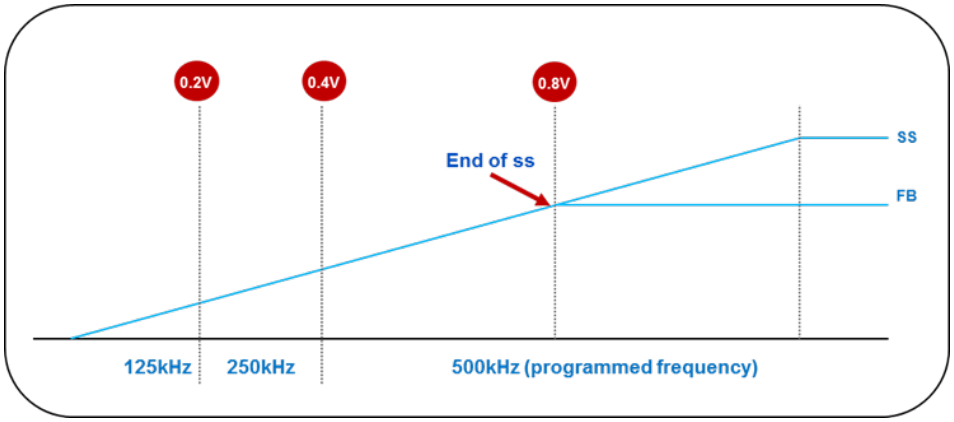
When the EN pin voltage level is above the PRE_EN threshold, a DC current (100 µA typ.) is forced in the SSDEL pin, charging the soft-start delay capacitor connected between SSDEL and GND.

Once the input voltage supply is above the V_{CC_UVLO} rising threshold (2.7 V typ.), the EN pin is forced above the UVLO_EN threshold, and SSDEL has reached the threshold (1 V typ.), the LEOPOL1 can finally start switching.

After SSDEL pin voltage reaches 1 V, the soft-start phase begins. According to the capacitor value on the SS pin, the internal loop reference slowly increases until 0.8 V, and consequently, the V_{OUT} voltage reaches the regulation value.

During the startup phase (to prevent in-rush current when the V_{OUT} voltage is too low), two switching frequency changes are implemented. As long as the SS voltage value is below 0.2 V, the switching frequency is a quarter of the programmed frequency. When the SS value is between 0.2 V and 0.4 V, the switching frequency is half of the programmed frequency. After SS reaches 0.4 V, the switching frequency nominally reaches the programmed one.

Figure 13. **Soft-start sequence**



The UVLO_EN threshold can also be exploited in order to program a higher V_{IN} turn-on level. This feature is simply implemented by connecting the EN pin to the central tap of a resistor divider between V_{IN} and GND. When doing so, the programmed V_{IN} turn-on threshold is given by the UVLO_EN threshold multiplied by the V_{IN} divider ratio.

Here below the complete flow chart of the startup sequence.

Figure 14. **Flow chart of startup sequence**

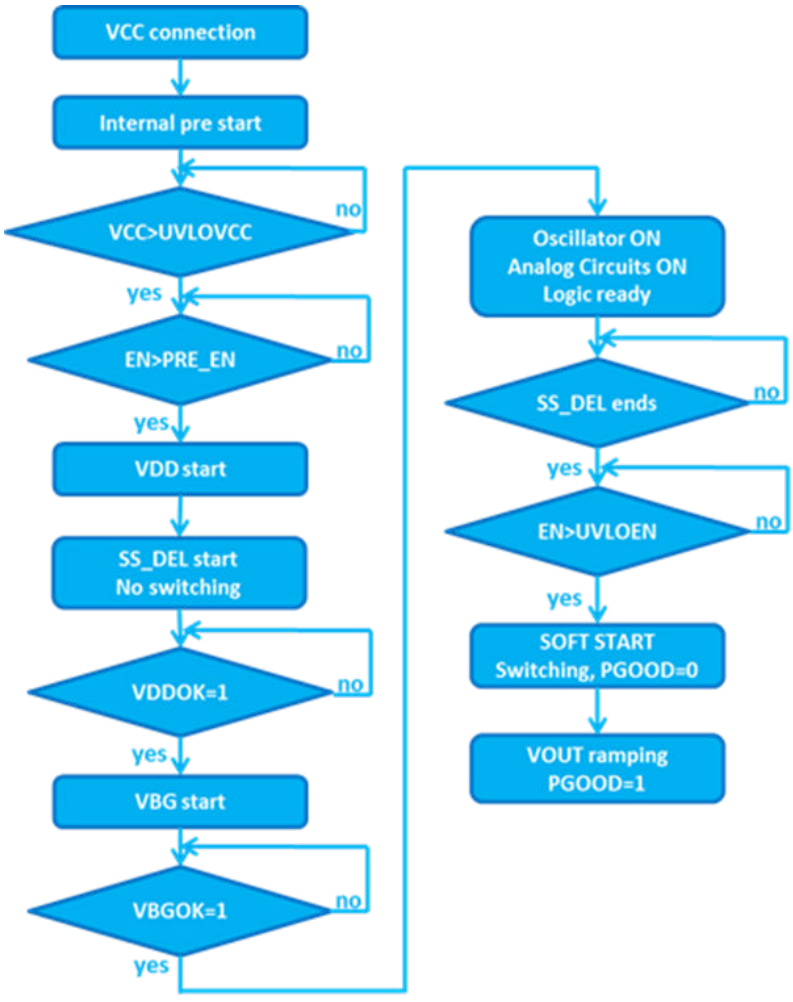
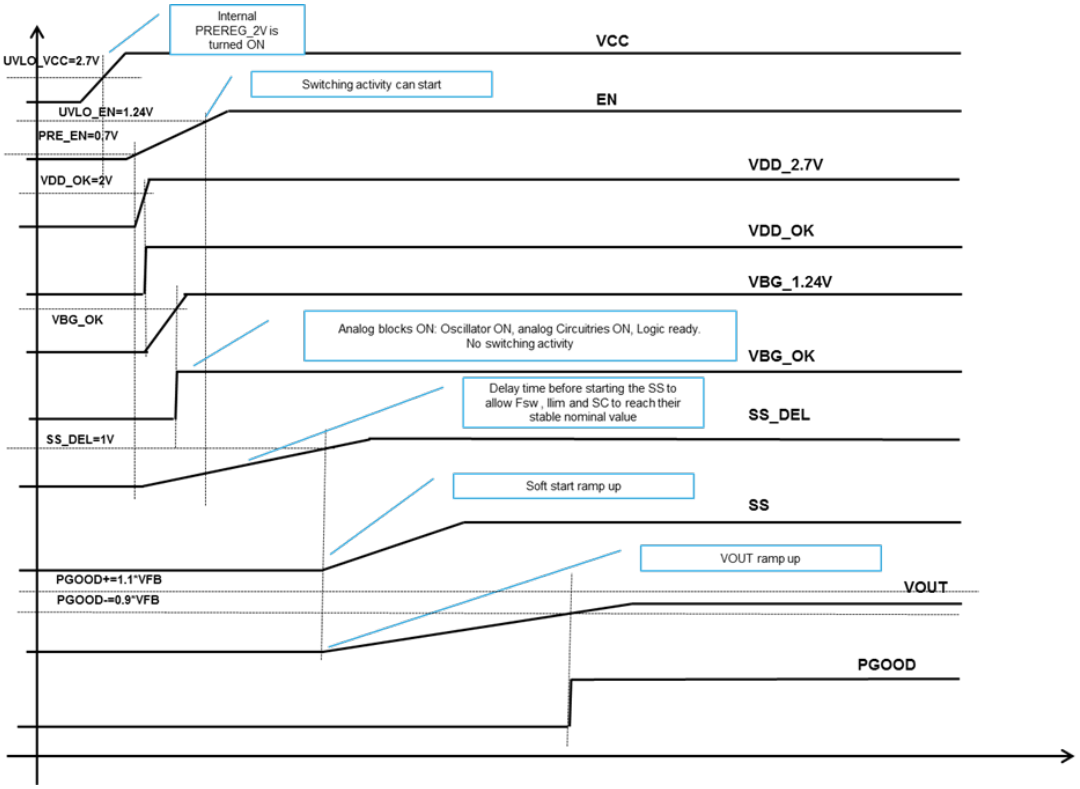


Figure 15. **LEOPOL1 startup sequence**



The output soft-start function is achieved by ramping up the SS pin voltage with a constant slew rate dV/dt. When the switching section is enabled, the SS pin charges, at a constant current, the capacitor connected between the SS and GND pins.

The SS voltage is used as a reference of the switching regulator, and the output voltage of the converter follows the ramp of the SS voltage. When the SS pin voltage is higher than 0.8 V typ., the error amplifier switches to the internal 0.8 V reference and regulates the output voltage.

During the SS period and until voltage at pin SS reaches 0.9 V, OVP is masked, PGOOD is asserted low, and a negative current protection on the low-side MOS (LS_OCP) is turned ON. If a negative current is detected during the soft-start phase or in very low load condition, the LS_OCP is detecting this and the low-side is forced OFF. This function is also called “zero-crossing detection”, because the current in the coil crosses the zero passing from positive (from GND versus the load) to negative (from the load versus GND).

When the feedback voltage enters the V_{FB} ± 10% Power Good window, the PGOOD pin is released (floating, PGOOD = high).

7.8 Turn-off

When the enable signal is forced below the UVLO_EN falling threshold (1. typ.), the PGOOD signal is pulled low, the device stops switching, and the power MOSFETs are set at high impedance.

The output capacitor is discharged through the output load.

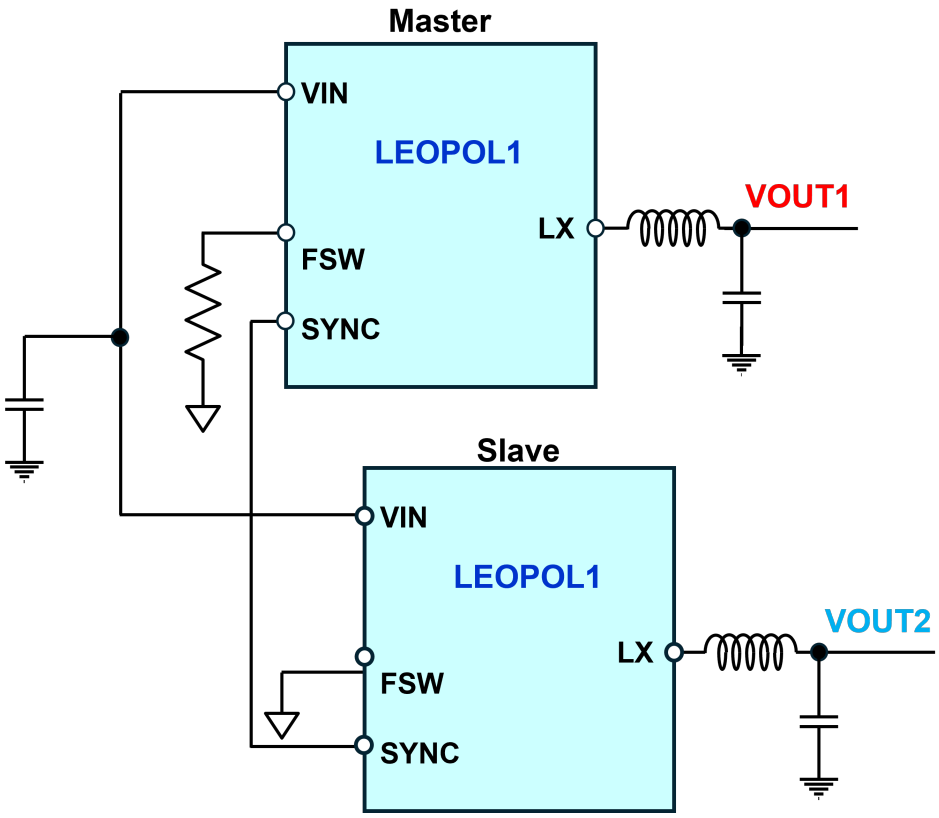
If V_{CC} goes below the V_{CC_UVLO} threshold, the device is switched off.

7.9 Synchronization

The LEOPOL1 can work in a two-synchronized ICs' configuration.

The clock synchronization is performed in case one IC is configured as master (FSW pin connected to GND through a switching frequency programming resistor) and the second one configured as slave (FSW pin shorted to GND). The main benefit of this configuration is the reduction of the input capacitor current ripple when the two devices work in an interleaved configuration.

Figure 16. **Synchronized ICs**



When two LEOPOL1s are synchronized together, they act as follows:

- Master IC
  - The SYNC pin is configured as clock output. The device provides, on the SYNC pin, its internal switching clock information with a 180° time shifting.
- Slave IC
  - The SYNC pin is configured as clock input. The device uses the clock information received on the SYNC pin to synchronize its internal switching clock.

Care must be taken to properly route the SYNC trace on the application PCB to avoid coupling with the power switching traces (for example, LX) that might generate jitter.

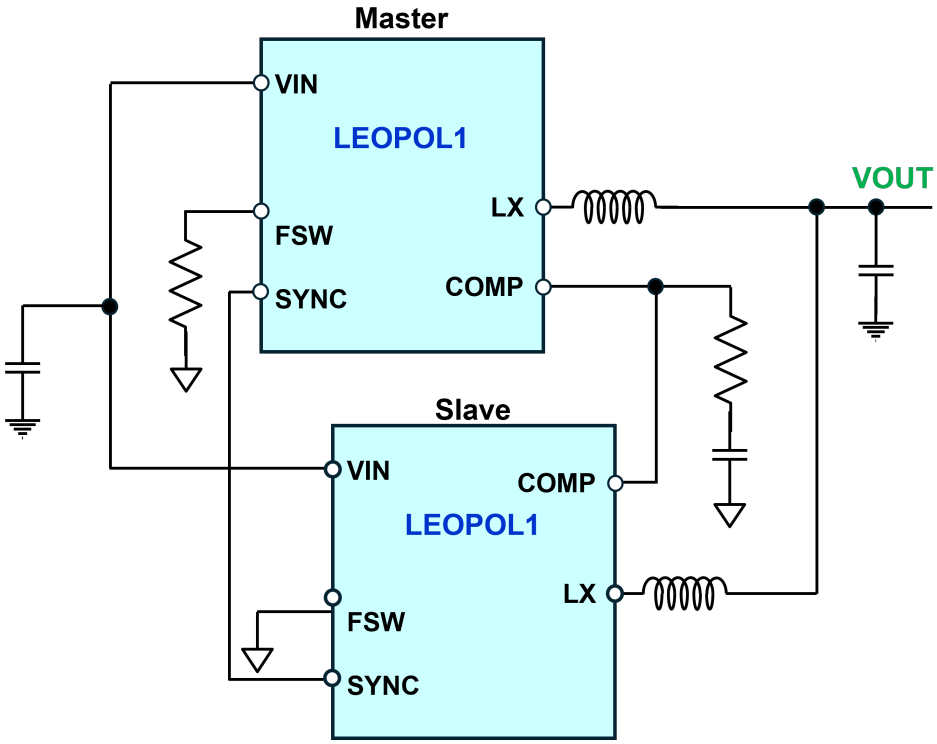
7.10 Interleaving

The LEOPOL1 can work in a two-interleaved ICs' configuration, in order to provide up to 14 A maximum load current.

IC interleaving (or parallelization) is performed in case one IC is configured as master (FSW pin connected to GND through a switching frequency programming resistor RFSW) and the second one is configured as slave (FSW pin forced to a voltage lower than 0.1 V). The two SYNC pins must be shorted together and the compensation network must be shared by the two ICs.

The main benefits of this configuration are the doubled available output current and the reduction of the output and input capacitor current ripple.

Figure 17. **Interleaved ICs**

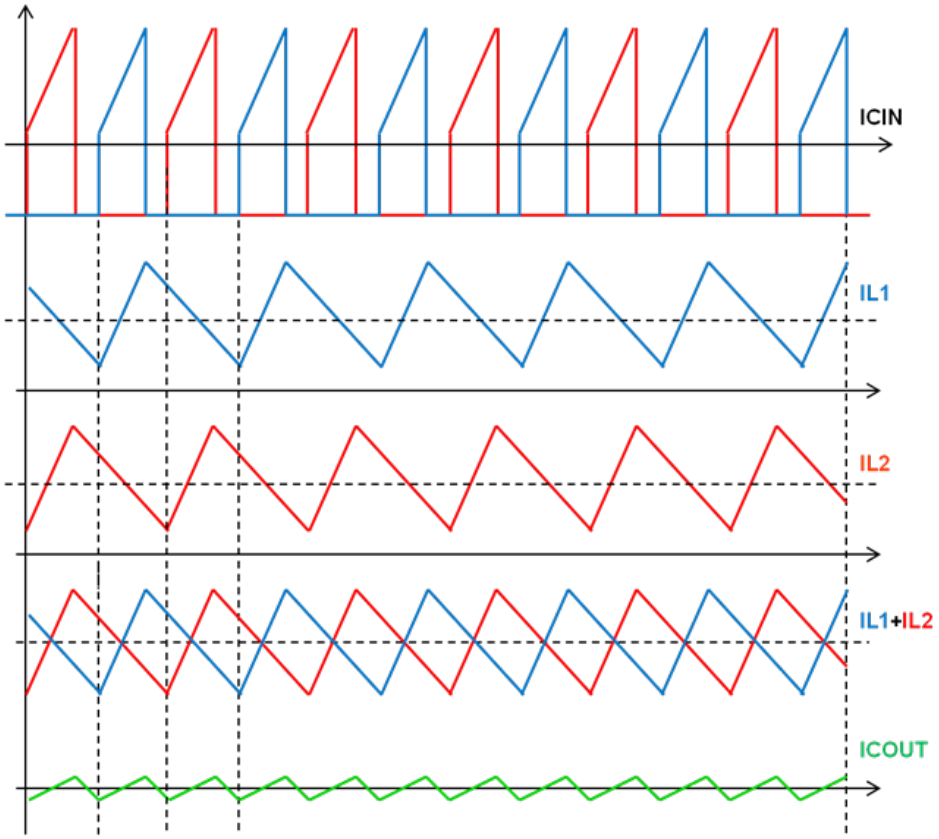


When two LEOPOL1s are interleaved, they act as follows:

- Master IC
  - The SYNC pin is configured as clock output. The device provides, on the SYNC pin, its internal switching clock information with a 180° time shifting.
- Slave IC
  - The SYNC pin is configured as clock input. The device uses the clock information received on the SYNC pin to synchronize its internal switching clock.

An example of the typical inductor and input/output currents waveforms is shown in Figure 18.

Figure 18. **Interleaved ICs current**



7.11 Fault management

The LEOPOL1 provides the following input and output voltage protections and monitoring features.

7.11.1 Power Good (PGOOD)

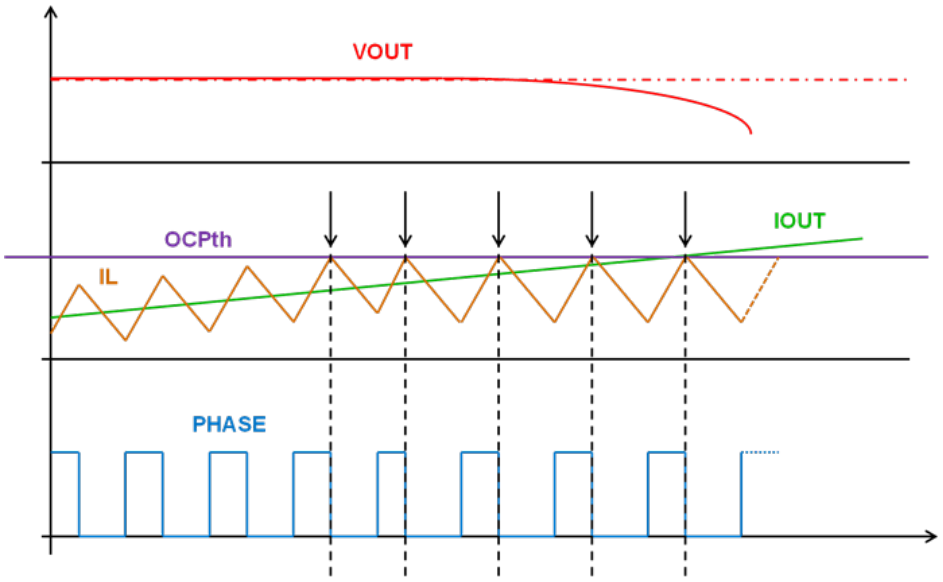
The Power Good pin (PGOOD) is an open drain output that is left floating if the output voltage is within ± 10% of the regulation window.

During startup, turn-off, and fault detection the PGOOD pin is forced low.

7.11.2 Overcurrent protection (OCP)

The LEOPOL1 is able to monitor, cycle-by-cycle, the high-side MOS current. If the measured current reaches the first level overcurrent limit threshold (I_{LIM1}), the high-side MOS is immediately turned off and the low-side MOS is turned-on, until a new clock pulse is generated. The PGOOD signal is not affected and it stays in high impedance (high level).

Figure 19. **Peak current protection (OCP1)**



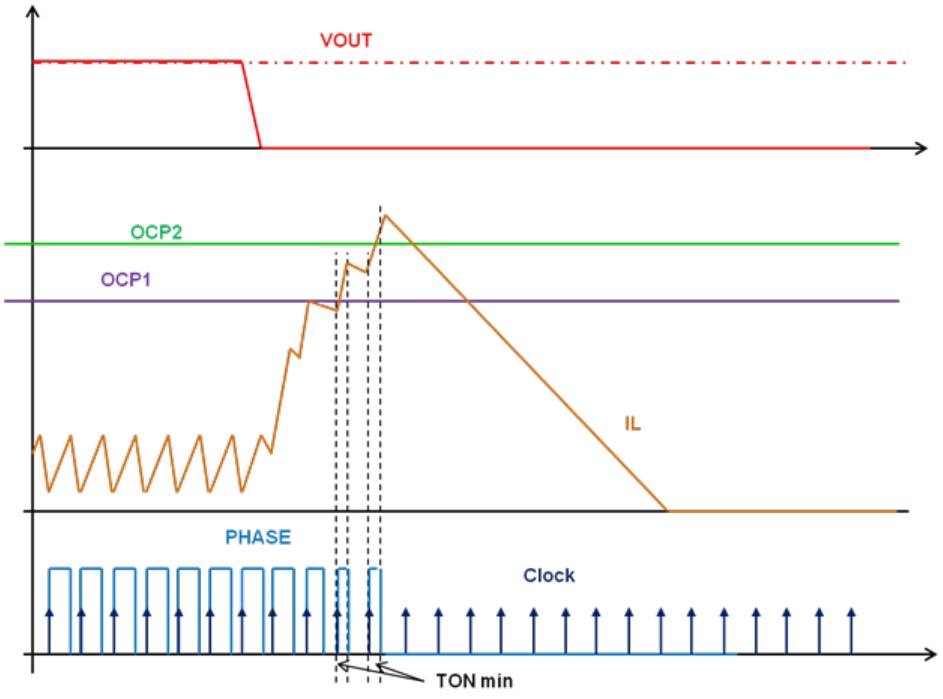
The peak current protection described above can meet some limitations in the case of an output voltage short versus GND.

In this case, the minimum high-side MOS on-time required for a precise current sensing could lead to a current increase above the OCP1 limit. In fact, since in this case, the output voltage is almost zero, the inductor current cannot decrease during the low-side MOS on-time.

To overcome this problem, the LEOPOL1 implements a second order overcurrent threshold OCP2 (refer to Figure 20). If the sensed high-side MOS current reaches the second level threshold (ILIM2), the switching regulator immediately turns off and the MOSFETs are set at high impedance. The PGOOD pin is asserted low and the SS capacitor is discharged.

Refer to Section 7.14 Alarm description for more details about alarms/faults handling.

Figure 20. **Second level overcurrent protection (OCP2)**

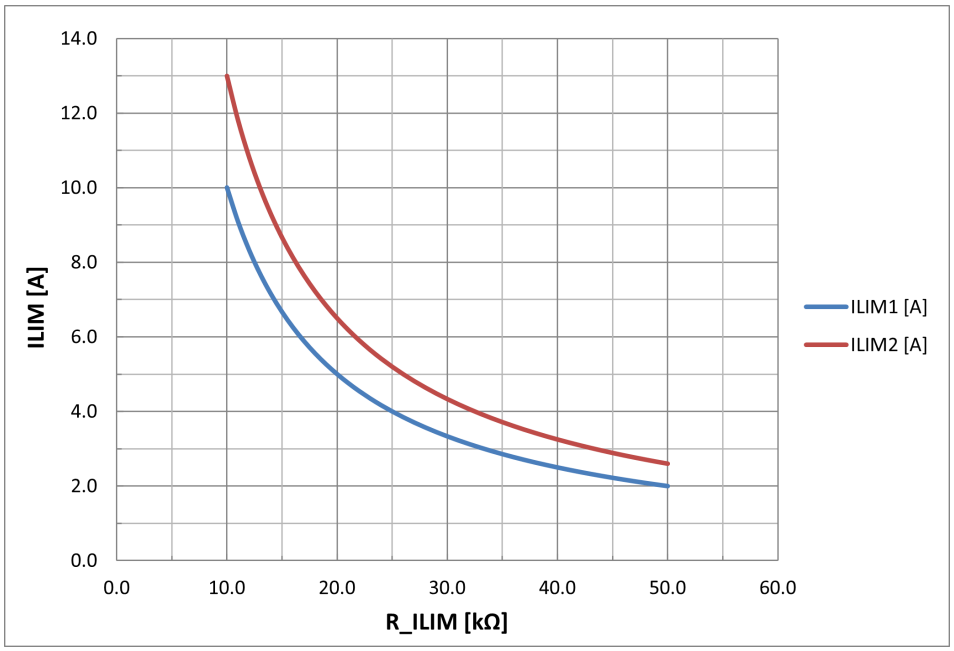


The default value for the first level overcurrent threshold is 10 A, with a second level OCP2 of 13 A (in this case the ILIM pin must be pulled up to V_{DD}).

If a resistor (R_{ILIM}) is connected between the ILIM pin and GND, the I_{LIM1} threshold can be set at a lower value, and the I_{LIM2} is consequently set at 1.3 x I_{LIM1}.

The graph below shows both programmable current limitations (I_{LIM1}, I_{LIM2}) versus the resistor R_{ILIM} connected at the ILIM pin.

Figure 21. Overcurrent protections vs. R_{ILIM}



7.12 Overvoltage protection

If the output voltage exceeds +25% of the nominal value (V_{FB} = 1 V), the internal signal OVP is asserted high. The driver stops switching and the bridge is forced in high impedance (both low and high-side MOS are turned OFF). The energy stored in the coil is discharged into the V_{IN} power supply. The whole power bridge stays in high impedance until V_{FB} < 0.85 V again.

7.13 Overtemperature protection

It is recommended to never let the device exceed the maximum allowable junction temperature. This temperature increase is mainly caused by the total power dissipated by the integrated power MOSFETs.

To avoid any damage to the device when reaching high temperature, the LEOPOL1 implements a thermal shutdown feature: when the junction temperature reaches 155 °C the device turns off both MOSFETs and the PGOOD pin is forced low.

When the junction temperature drops again to around 135 °C, the overtemperature fault condition is cleared and the PGOOD open drain pin goes again to high impedance.

Refer to the “Alarm description” section for more details about the restart sequence and alarm handling.

7.14 Alarm description

When a fault condition occurs (thermal shutdown or the 2nd level overcurrent protection), the capacitor connected to the AL pin (typ. 1 µF) is discharged and charged with a constant current (typ. 20 µA); this is used to generate a “cooling” and a “watching” time cycle.

For the “cooling” time frame $\Delta t_{cooling}$ = 16 * t_AL, while for the “watching” time frame $\Delta t_{watching}$ ~ 3 * $\Delta t_{cooling}$ where t_{AL} = C_{AL}*K/20 µA and K = 3.1 V.

In case of thermal shutdown, the cooling time is incremented by Δtfault (time required to make the device exit the fault condition – the junction temperature must decrease to T_{OTP} minus hysteresis). Time Δt_{fault} is negligible in case of 2nd level overcurrent protection.

The device cools down during the first window $\Delta t_{fault}+\Delta t_{cooling}$: switching is stopped, LX is set to high impedance, the SS pin is discharged/pulled down to GND. Afterwards, the device restarts with a soft-start sequence at the beginning of the “watching” time frame during which the logic circuitry of the alarm section starts monitoring for a possible consecutive fault.

After a first alarm is raised, an internal counter is incremented and two different scenarios can be generated:

1. No consequent alarm is raised during the “watching” time frame: in this case, the internal counter is reset and the device continues regulating. If a new alarm is raised after the watching window is over, the cycle is repeated. This mode of operation is called “Hiccup mode”.
2. Another alarm is raised during the “watching” window: in this case, the “cooling” + “watching” time cycle is restarted and the internal counter is incremented. If 16 total consecutive alarm events happen during the watching window, the device is latched and the regulation is stopped. To exit from a latched condition, an enable cycle has to be externally provided. This mode of operation is called “Latched mode”.

Table 9 - Alarm summary summarizes what happens in different alarm conditions.

Table 13. Alarm summary

Event	Description	PGOOD
OVP	Overvoltage protection: If V_{FB} > 1V, the LEOPOL1 device stops switching until V_{FB} < 0.85V. Both power MOSFETs are OFF.	low
OTP	Overtemperature protection: If T_j > 155°C, the LEOPOL1 device stops switching (both power MOSFETs are OFF) for $\Delta t_{fault}+\Delta t_{cooling}$. After this time, the device restarts in soft-start. If this event is repeated for 16 times within the watching window, the info is latched and the device can be restarted only by cycling the EN pin.	low
OCP1	Overcurrent protection 1: It is externally programmable by a resistance on pin ILIM. This signal is used only internally to limit the coil current (stopping Ton time). No alarm is given and the bridge continues to switch.	high
OCP2	Overcurrent protection 2: This threshold is about 1.3*OCP1. When this threshold is crossed, the LEOPOL1 stops switching (both power MOSFETs are OFF) for $\Delta t_{fault}+\Delta t_{cooling}$. After this time, the device restarts in soft-start. If this event is repeated for 16 times within the watching window, the info is latched and the device can be restarted only by cycling the EN pin.	low

7.15 Hiccup and latched modes configuration

Entry in hiccup or latched mode described in the previous section depends on several factors:

- Watching window duration - f(C_{AL})
- Soft-start time - f(C_{SS})
- Thermal performance of the application
- Alarm type (thermal or OCP2)
- Voltage level at AL pin

For thermal alarms, if a “Latched mode” operation is desired, the user must select a watching window duration longer than the time required by the device to trigger the thermal protection after the cooling time. This makes the alarm event counter increment without being reset, leading to a latched behavior after 16 events.

If a “Hiccup mode” operation is desired, the user must select a watching window duration shorter than the time required by the device to trigger the thermal protection after the cooling time. This selection results in a reset of the event counter after each fault and the stop/restart sequence continues in an infinite loop.

Considering that the thermal performance of the device is strongly dependent on the application conditions (PCB layout, ambient temperature, etc.…) the value of C_{AL} must be carefully evaluated in order to have the desired cooling/watching time and response to thermal alarms.

In case of OCP2 alarms, entry in hiccup or latched mode is strictly linked to the soft-start time. Similar to thermal events, in order to have a latched response to an OCP2 event, the programmed soft-start time must be shorter than the watching window duration. If a hiccup response is desired, the soft-start time must be longer than the watching window duration.

The considerations above imply that the value of both C_{SS} and C_{AL} must be chosen to fit the application conditions and get the desired response bearing in mind that the value of C_{AL} has an impact on the response to both thermal and OCP2 events.

If the user prefers a simpler approach to alarms, the behavior of the device in case of thermal or OCP2 events can be forced by driving the AL pin to the right voltage:

- Forced hiccup mode: V_{AL} = 0 V
- Forced latched mode: V_{AL} > 0.2 V.

8 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

8.1 PowerSO-36 package information

Figure 22. **PowerSO-36 package outline**

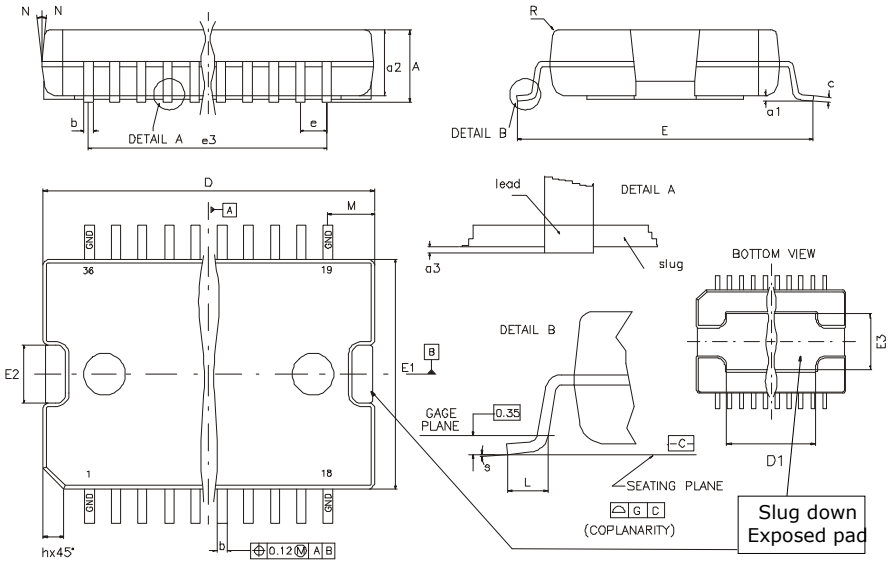


Table 14. **PowerSO-36 mechanical data**

Ref.	Dimensions (mm)		
	Min.	Typ.	Max.
A	-	-	3.60
a1	0.10	-	0.30
a2	-	-	3.30
a3	0	-	0.10
b	0.22	-	0.38
c	0.23	-	0.32
D	15.80	-	16.00
D1	9.40	-	9.80
E	13.90	-	14.50
E1	10.90	-	11.10
E2	-	-	2.90
E3	5.80	-	6.20
e	-	0.65	-
e3	-	11.05	-
G	0	-	0.10
H	15.50	-	15.90
h	-	-	1.10
L	0.8	-	1.10
N	10° (max)		
s	8° (max)		

8.2 PowerSO-36 packing information

The flight models are delivered in a 600 position tape, out of which 100 consecutive ones are filled with a product, the others being left empty. The carrier tape and tape are described in the figures below.

The development samples are delivered in 7-position sticks of the same tape.

Figure 23. PowerSO-36 carrier tape outline

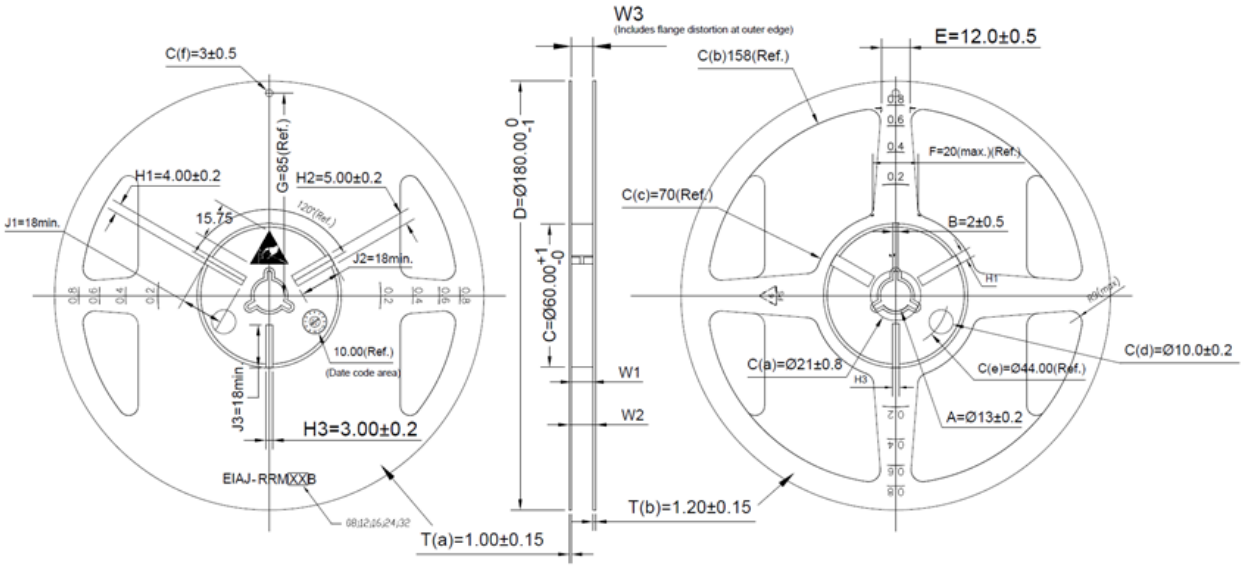
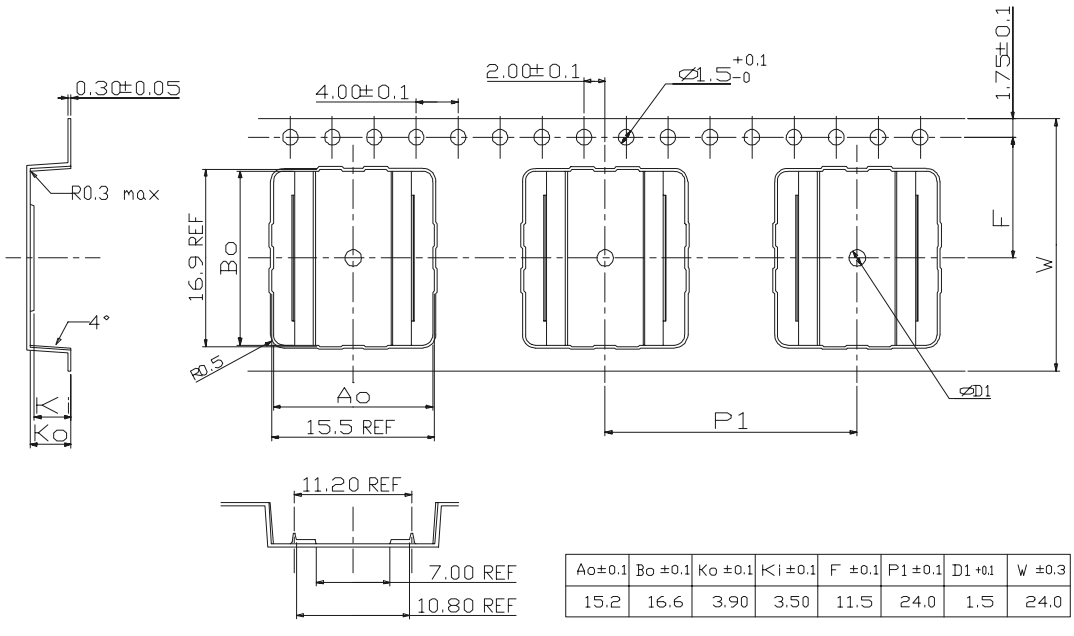


Figure 24. PowerSO-36 tape outline



Ao±0.1	Bo ±0.1	Ko ±0.1	Ki ±0.1	F ±0.1	P1 ±0.1	D1 +0.1	W ±0.3
15.2	16.6	3.90	3.50	11.5	24.0	1.5	24.0

NOTE:

1) Cumulative tolerance of 10 sprocket holes: 0.2mm
2) Camber: 1mm/100mm max

8.3 Outgassing

The outgassing data of the PowerSO-36, measured as per ASTM-E-595, are provided in Table 15 below. They are compliant with the LEO generic specification setting the maximum limits for the recovered mass loss at 1% and for the collected volatile condensable material at 0.1%.

Table 15. Outgassing

Characteristics	Value	Unit
Recovered mass loss	0.06	%
Collected volatile condensable material	0.00	%

9 Ordering information

Table 16. Ordering information

Quality level	Quality level	Package	Lead-finish	Marking (1)	Packing	Mass
LEOPOL1PDT (2)	Flight model	PS0-36	NiPdAu	LEOPOL1	Tape and reel (3)	2.0

1. *Product specific marking. See Figure 25 for the descrption of the complete marking.*
2. *Under development.*
3. *Sampling with sticks of tape.*

10 Other information

10.1 Marking

The marking of the parts is summarized for the LEO flight models and in Table 17 for the development samples (refer to TN1418 for the description of the development samples quality level).

Figure 25. PSO marking

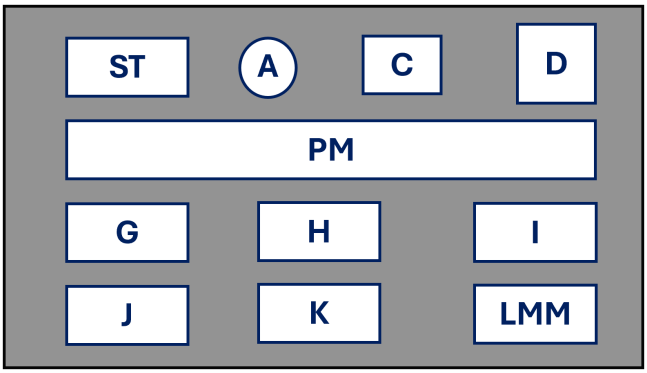


Table 17. Product marking description

Field	Description	LEOPOL1 values
ST	ST logo	
A	Pb free logo	e4 (1)
C	Sublot assembly index	Lot dependent
D	QR code	Lot dependent
PM	Specific product marking	See Table 16
G	Assembly plant	99 (Muar) (1)
H	Back end sequence (2)	xxx
I	Diffusion traceability	VA (Agrate) (1)
J	Country of origin	MYS (Malaysia) (1)
K	Test and finishing plant	99 (Muar) (1)
L	Date code year (last digit)	0 to 9
MM	Date code week	01 to 52

1. *Different values could denote that a product change notice has been issued.*
2. *Assembly flow reference.*

10.2 Product documentation

The flight models are delivered with a certificate of conformance enclosed in the shipment box. Refer to TN1432 for the list of information it provides.

Table 18. Documentation LEO

Quality level	Documentation
Development samples	-
Flight parts	Certificate of conformance (1)

1. *See TN1432 for details on the information provided in the certificate of conformance.*

Revision history

Table 19. **Document revision history**

Date	Revision	Changes
08-Aug-2024	1	Initial release.
19-Dec-2024	2	Updated Figure 4, Table 6 and Section 10.1.

Contents

List of tables

List of figures