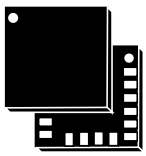
LSM6DB0

iNEMO advanced inertial module: 3D accelerometer, 3D gyroscope and signal processor

Datasheet - preliminary data



LGA-22 (3x3x1 mm)

Features

- Motion sensors:
  - ±2/±4/±8 *g* full scale
  - ±245/±500/±2000 dps full scale
  - 6-axis eco power mode down to 1.8 mA
  - 3 independent acceleration channels and 3 angular rate channels
  - Embedded temperature sensor
  - 20 Kbyte data batching
  - 6-axis and 9-axis quaternions
  - Self-test
  - ECOPACK®, RoHS and “Green” compliant
- Signal processor:
  - Brain: ARM-based, 32-bit Cortex-M0 core
  - Flash memory and SRAM including a bank with error code correction (ECC)
  - I^2C master port
  - I^2C slave port
  - SPI master/slave
  - 4-wire UART
  - 11 programmable GPIOs
  - Low-power features
  - 8 x 32-bit dual timers, watchdog timer (WDG), Cortex-M0 system tick (SysTick) timer
  - Standard 4-wire JTAG and 2-wire SWD
  - 80 MHz / 32 kHz RC / up to 80 MHz from single-ended external clock

Applications

- Sensor hubs and sensor fusion
- Significant motion-detection and gesture recognition
- Gaming and geomagnetic rotation vectors
- Pedometers, step counters and step detectors
- Calibrated compasses
- Enhanced navigation and motion tracking

Description

The LSM6DB0 is an advanced low-power high-performance smart sensor system available in a plastic 3x3x1 mm LGA (land grid array) package. The module includes a 3-axis accelerometer, 3-axis gyroscope and Cortex-M0 core with Flash, SRAM, dual timers, 2 I^2C (master/slave), 1 SPI (master/slave) and 1 UART (transmitter/receiver).

The LSM6DB0 has a full-scale acceleration range of ±2/±4/±8 *g* and an angular rate range of ±245/±500/±2000 dps. The LSM6DB0 has two operating modes in that the accelerometer and gyroscope sensors can be either activated at the same ODR or the accelerometer can be enabled while the gyroscope is in power-down.

The module collects inputs from the accelerometer, gyroscope, compass and several other sensors and elaborates/fuses together 9 or 10 axes (iNemo Engine software) which are provided to the main application processor. For example, quaternions achieve the best compromise in terms of power saving for the overall system. The LSM6DB0 is fully compliant with the Android Kitkat OS.

Table 1. Device summary

Order codes	Temp. range [°C]	Package	Packaging
LSM6DB0	-40 to +85	LGA-22	Tray
LSM6DB0TR	-40 to +85	LGA-22	Tape and reel

This is preliminary information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

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Contents

List of tables

List of figures

1 Block diagrams and pin description

1.1 Block diagrams

The LSM6DB0 includes a 3-axis accelerometer and 3-axis gyroscope combined with a low-power microprocessor ARM-based Cortex-M0. The reference block diagram is described in *Figure 1* while the motion sensor and microprocessor block diagrams are described in *Figure 2* and *Figure 3*, respectively.

Figure 1. LSM6DB0 application block diagram

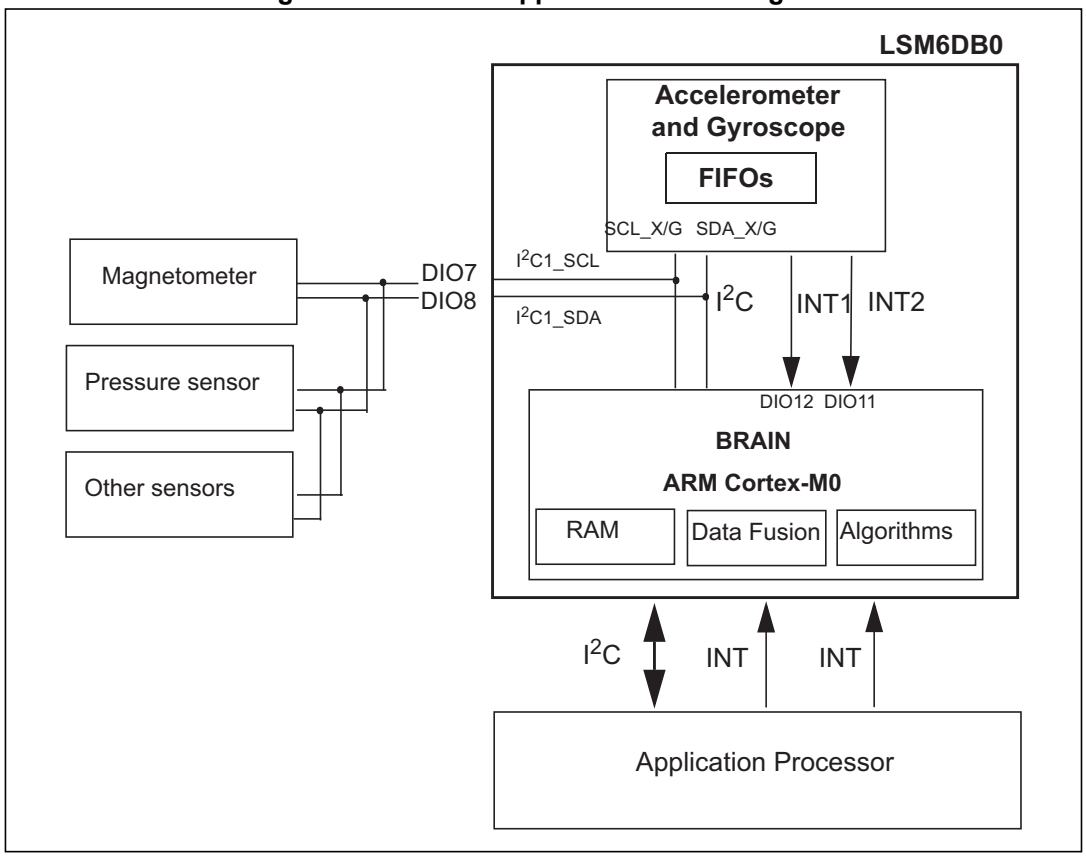


Figure 2. Accelerometer and gyroscope block diagram

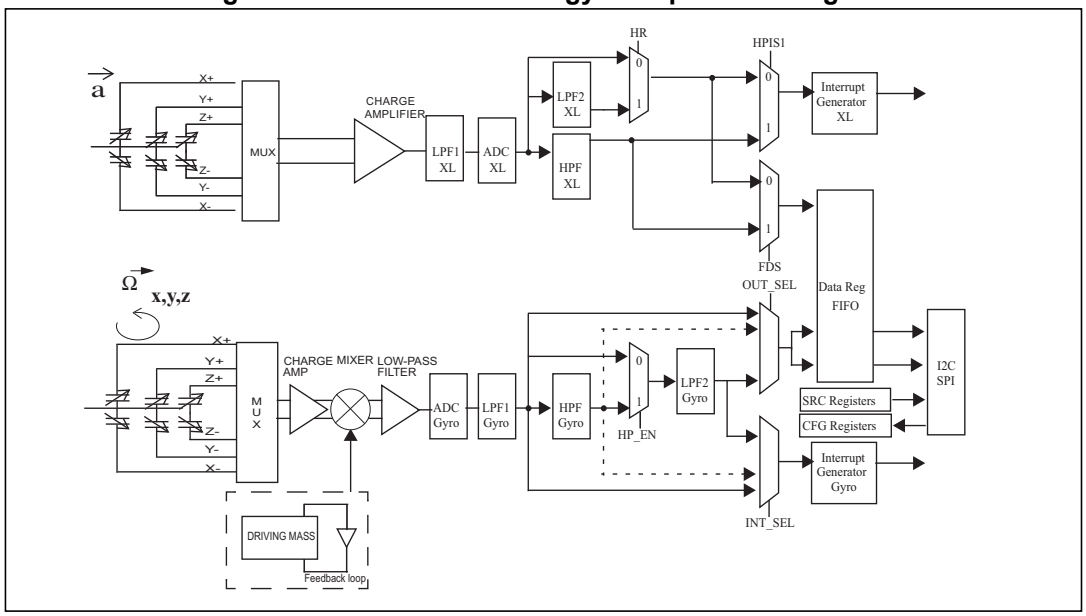
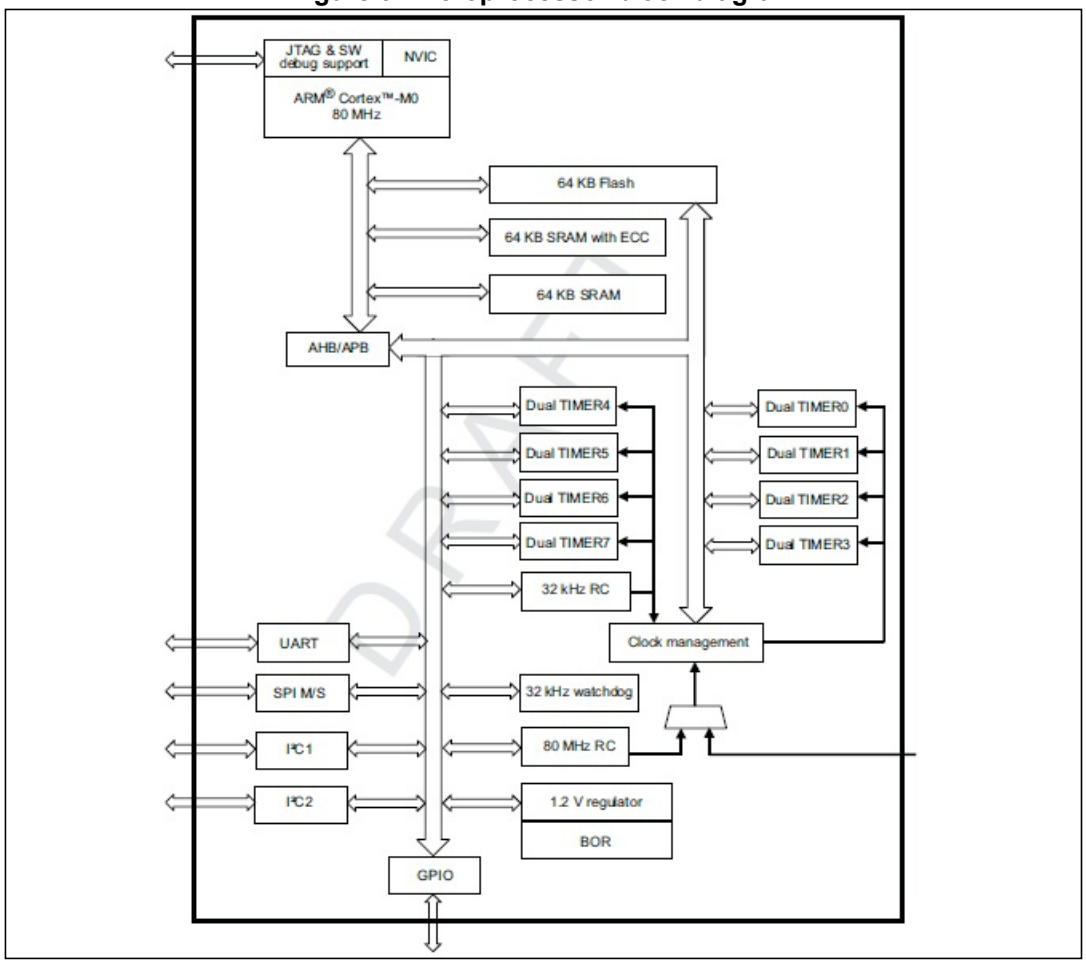


Figure 3. Microprocessor block diagram



Legend: NVIC = nested vectored interrupt controller, GPIO = general-purpose input/output

1.2 Pin description

Figure 4. Pin connections

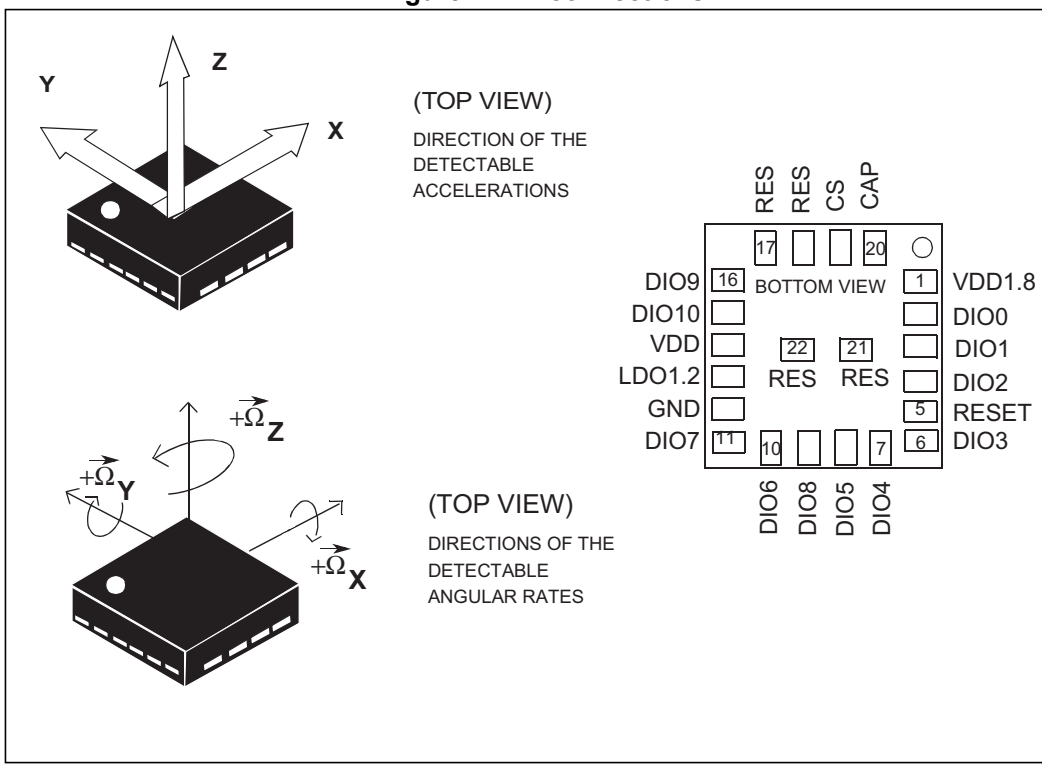


Table 2. Pin description

Pin#	Name	Function	I/O level
1	VDD1.8	Power supply for I/O pins	
2	DIO0	GPIO0 / SW_TDIO / JTAG TMS / UART_CTS	VDD1.8
3	DIO1	GPIO1 / SW_TCK / JTAG TCK / UART_RTS	VDD1.8
4	DIO2	GPIO2 / I^2C2_SCL (slave) / UART_TXD	VDD1.8
5	RESET	Microcontroller reset	VDD1.8
6	DIO3	GPIO3 / I^2C2_SDA (slave) / UART_RXD	VDD1.8
7	DIO4	GPIO4 / JTAG TDO	VDD1.8
8	DIO5	GPIO5 / JTAG TDI / Clock input	VDD1.8
9	DIO8	GPIO8 / I^2C1_SDA (master) / SPI_OUT	VDD
10	DIO6	GPIO6 / 16 MHz clock output / Clock 32KHz	VDD
11	DIO7	GPIO7 / I^2C1_SCL (master) / SPI_Clock	VDD
12	GND	0 V supply	
13	LD01.2	Connect to decoupling capacitor for 1.2 V digital regulator to GND	
14	VDD(1)	Analog and I/O pins power supply	

Table 2. Pin description (continued)

Pin#	Name	Function	I/O level
15	DIO10	GPIO10 / spi_input	VDD
16	DIO9	GPIO9 / SPI_CS	VDD
17	RES	Connect to GND	
18	RES	Connect to GND	
19	RES	Connect to VDD	
20	CAP	Connect to GND with ceramic capacitor(2)	
21	RES	Leave unconnected	
22	RES	Leave unconnected	

1. Recommended 100 nF filter capacitor.
2. 10 nF (±10%), 16 V. 1 nF minimum value has to be guaranteed under 12 V bias condition.

The INT1 and INT2 pins of the motion sensor are internally connected to the DIO12 and DIO11 pins of the microcontroller, refer to *Figure 1*.

2 LSM6DB0 application hints

Figure 5. Application circuit with I²C sensors

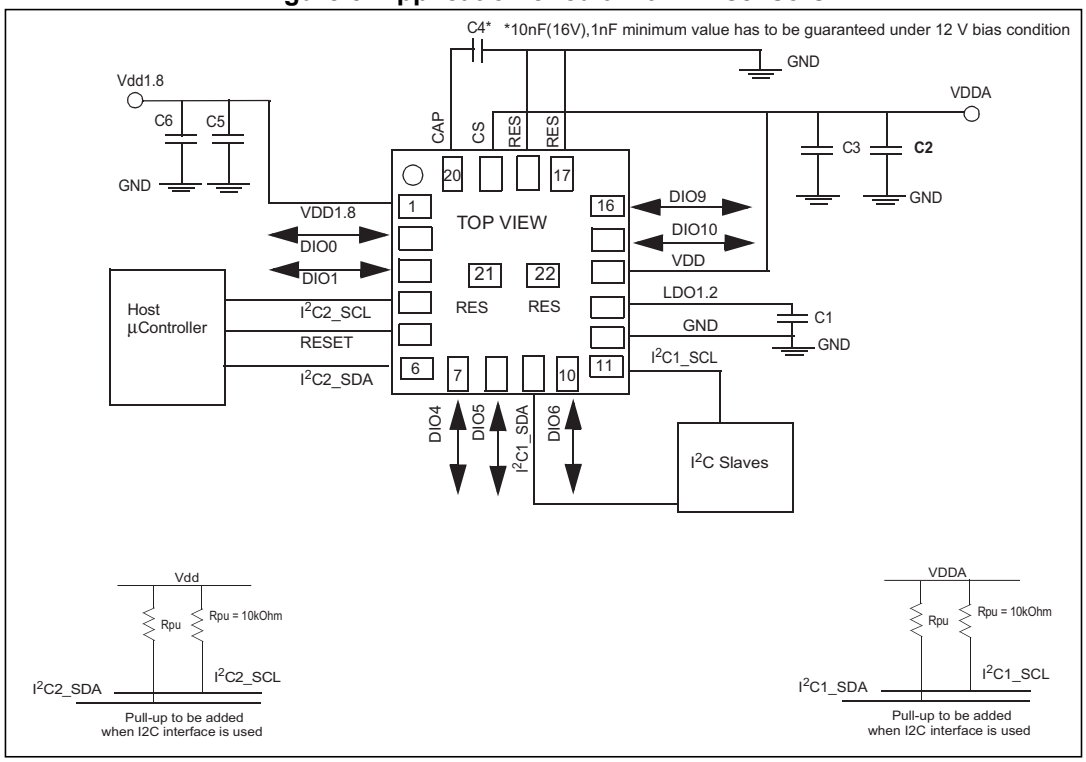


Table 3. External components

Component	Description	Value
C1	Decoupling capacitor for 1.2 V digital regulator	220 nF
C2	Decoupling capacitor for 1.8 V–3.6 V digital regulator (HF)	100 nF
C3	Decoupling capacitor for 1.8 V – 3.6 V digital regulator (LF)	10 µF
C4	10 nF (±10%), 16 V. 1 nF minimum value has to be guaranteed under 12 V bias condition	10 nF
C5	Decoupling capacitor for 1.8 V digital regulator (LF)	10 µF
C6	Decoupling capacitor for 1.8 V digital regulator (HF)	100 nF

3 LSM6DB0 features

In the LSM6DB0 a complete sensor networking has been created with three additional external sensor connections supported by the I^2C bus (eg. compass, pressure sensors, others). External data acquisition is totally configurable with a different data rate selection and different data reads for each slave sensor. To minimize the core's (Brain) power consumption, dedicated FIFO buffers are available in the inertial sensors to maximize the temporary data storage.

The LSM6DB0 can manage standard hub functionalities together with the implementation of complex algorithms for the following applications:

- Sensor batching with combination of sensors based on different ODR and related time-stamp information;
- Sensor fusion with the support of quaternions, gravity, linear acceleration and orientation data;
- Pedometers;
- Game rotation vectors;
- Geomagnetic rotation vectors (3-axis accelerometer and 3-axis magnetometer);
- Compass calibration;
- Gyroscope bias estimation and offset compensation;
- Accelerometer background calibration;
- Significant motion;
- Gesture recognition;

The device provides optimal flexibility, modularity and scalability in the customization of software routines for the customer.

The LSM6DB0 completely offloads the application processor from the computation of sensor fusion, delivering unparalleled low-power consumption at the system level. Owing to the embedded core (Brain) in the device, there is no need for an external processing unit nor storage.

The LSM6DB0 is compliant with Android Kitkat OS.

4 Mechanical characteristics

4.1 Accelerometer and gyroscope mechanical characteristics

T = 25 °C unless otherwise noted [a]

Table 4. Mechanical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.[1]	Max.	Unit
LA_FS	Linear acceleration measurement range			±2		*g*
				±4		
				±8		
G_FS	Angular rate measurement range			±245		dps
				±500		
				±2000		
LA_So	Linear acceleration sensitivity	FS = ±2 g		0.061		mg/LSb
		FS = ±4 g		0.122		
		FS = ±8 g		0.244		
G_So	Angular rate sensitivity	FS = ±245 dps		8.75		mdps/LSb
		FS = ±500 dps		17.50		
		FS = ±2000 dps		70		
LA_TyOff	Linear acceleration typical zero-*g* level offset accuracy[2]	FS = ±8 g		±90		m*g*
G_TyOff	Angular rate typical zero-rate level[3]	FS = ±2000 dps		±30		dps
LA_ODR	Linear acceleration output data rate	Gyro ON		952 476 238 119 59.5 14.9		Hz
		Gyro OFF		952 476 238 119 50 10		Hz

a. The operational power supply range is from 1.71 V to 3.6 V.

Table 4. Mechanical characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.(1)	Max.	Unit
G_ODR	Angular digital output data rate			952 476 238 119 59.5 14.9		Hz
Top	Operating temperature range		-40		+85	°C

1. Typical specifications are not guaranteed.
2. Typical zero-g level offset value after soldering.
3. Typical zero-rate level offset value after MSL3 preconditioning.

4.2 Accelerometer and gyroscope electrical characteristics

T = 25 °C unless otherwise noted.

Table 5. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.(1)	Max.	Unit
VDD	Core and I/O pins supply voltage		1.71		3.6	V
LA_Idd	Accelerometer current consumption in normal mode	ODR = 10 Hz		60		µA
		ODR = 50 Hz		160		
		ODR ³ 119 Hz		330		
G_Idd	Gyroscope current consumption in eco power mode			1.8		mA
Top	Operating temperature range		-40		+85	°C

1. Typical specifications are not guaranteed.

4.3 Microprocessor electrical characteristics

Characteristics measured in *Table 6* are for recommended operating conditions unless otherwise specified. Typical values are in reference to T_A = 25 °C, V_{DD} =1.8 V.

Table 6. DC and AC parameters

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
VDD	Operating supply voltage master serial port (DIO6 to DIO10)		1.71		3.6	V
VDD1.8	Operating supply voltage (DIO0 to DIO5)		1.75	1.8	1.95	V
Power consumption (Dhrystone without compiler options)						
I_{supply}	Supply current	Reset		50		nA
		Active (CPU, Flash, and RAM)			20	mA
		From RAM 80 MHz (0.79 DMIPS/MHz) 40 MHz (0.79 DMIPS/MHz) 20 MHz (0.79 DMIPS/MHz) 16 MHz (0.79 DMIPS/MHz) 10 MHz (0.79 DMIPS/MHz)		 10.3 5.95 3.85 3.48 2.9		
		From Flash 80 MHz (0.3 DMIPS/MHz) 40 MHz (0.43 DMIPS/MHz) 20 MHz (0.56 DMIPS/MHz) 16 MHz (0.79 DMIPS/MHz) 10 MHz (0.79 DMIPS/MHz)		 7.5 5.5 4.74 4.34 3.7		
Digital input and output (1.8 V supply)						
C_{IN}(1)	Port I/O capacitance		1.3	1.4	1.7	pF
R_{PD}(1)	Pull-down value		117	211	334	kW
T_{RISE}(1)	Rise time	0.1*V_{DD} to 0.9*V_{DD}, C_L = 50 pF	10.3		19	ns
T_{FALL}(1)	Fall time	0.9*V_{DD} to 0.1*V_{DD}, C_L = 50 pF	11		22	ns
V_{IH}(1)	Logic high-level input voltage		0.65 V_{DD}			V
V_{IL}(1)	Logic low-level input voltage				0.35 V_{DD}	V
Digital input and output (3.3 V supply)						
C_{IN}(1)	Port I/O capacitance		1.3	1.4	1.7	pF
R_{PD}(1)	Pull-down value		53	84	144	kW
R_{PU}(1)	Pull-up value		57	81	122	kW
T_{RISE}(1)	Rise time	0.1*V_{DD} to 0.9*V_{DD}, C_L = 50 pF	1.4		12	ns
T_{FALL}(1)	Fall time	0.9*V_{DD} to 0.1*V_{DD}, C_L = 50 pF	1.5		12.5	ns

Table 6. DC and AC parameters (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IH}(1)	Logic high-level input voltage		0.65 V_{DD}			V
V_{IL}(1)	Logic low-level input voltage				0.35 V_{DD}	
T_A	Operating ambient temperature range		-40		85	°C

1. Guaranteed by design

4.4 Temperature sensor characteristics

@ Vdd = 3V, T = 25 °C unless otherwise noted [b]

Table 7. Temperature sensor characteristics

Symbol	Parameter	Test condition	Min.	Typ.(1)	Max.	Unit
TODR	Temperature refresh rate	Gyro OFF(2)		50		Hz
		Gyro ON		59.5		
TSen	Temperature sensitivity(3)			16		LSB/°C
Top	Operating temperature range		-40		+85	°C

1. Typical specifications are not guaranteed.
2. When the accelerometer ODR is set to 10 Hz and the gyroscope block is turned off, the TODR value is 10 Hz.
3. The output of the temperature sensor is 0 (typ.) at 25 °C

b. The product is factory calibrated at 3.0 V.

5 Motion sensor communication interface characteristics

5.1 I²C - inter-IC control interface

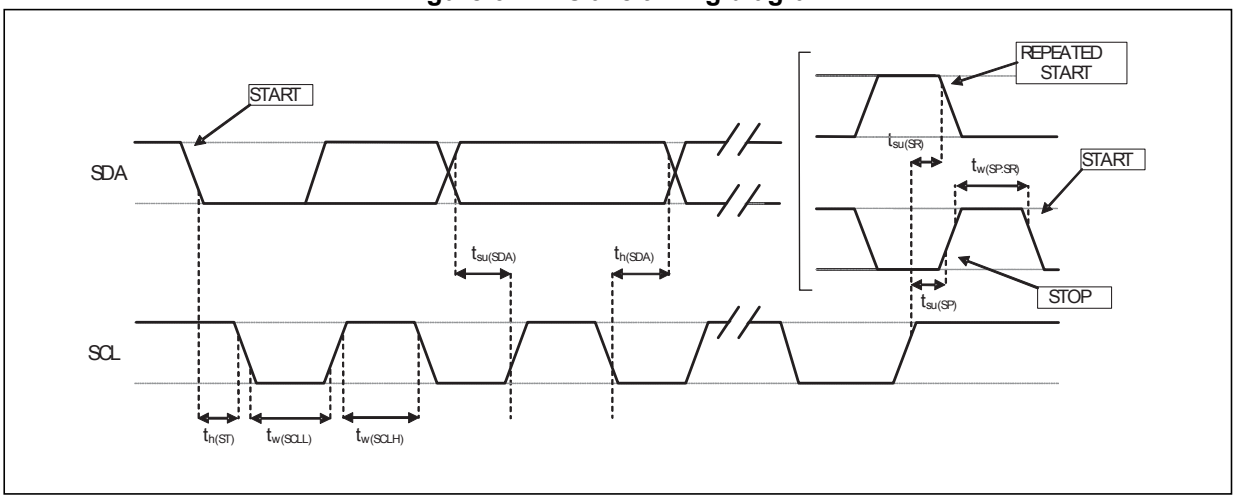
Subject to general operating conditions for Vdd and Top.

Table 8. I²C slave timing values

Symbol	Parameter	I²C standard mode (1)		I²C fast mode (1)		Unit
		Min.	Max.	Min.	Max.	
$f_{(SCL)}$	SCL clock frequency	0	100	0	400	kHz
$t_{w(SCLL)}$	SCL clock low time	4.7		1.3		µs
$t_{w(SCLH)}$	SCL clock high time	4.0		0.6		
$t_{su(SDA)}$	SDA setup time	250		100		ns
$t_{h(SDA)}$	SDA data hold time	0.01	3.45	0.01	0.9	µs
$t_{h(ST)}$	START condition hold time	4		0.6		µs
$t_{su(SR)}$	Repeated START condition setup time	4.7		0.6		
$t_{su(SP)}$	STOP condition setup time	4		0.6		
$t_{w(SP:SR)}$	Bus free time between STOP and START condition	4.7		1.3		

1. Data based on standard I²C protocol requirement, not tested in production.

Figure 6. I²C slave timing diagram



Note: Measurement points are done at 0.2·VDD and 0.8·VDD, for both ports.

6 Terminology

6.1 Sensitivity

Linear acceleration sensitivity can be determined, for example, by applying 1 *g* acceleration to the device. Because the sensor can measure DC accelerations, this can be done easily by pointing the selected axis towards the ground, noting the output value, rotating the sensor 180 degrees (pointing towards the sky) and noting the output value again. By doing so, ±1 *g* acceleration is applied to the sensor. Subtracting the larger output value from the smaller one, and dividing the result by 2, leads to the actual sensitivity of the sensor. This value changes very little over temperature and over time. The sensitivity tolerance describes the range of sensitivities of a large number of sensors.

An angular rate gyroscope is device that produces a positive-going digital output for counterclockwise rotation around the axis considered. Sensitivity describes the gain of the sensor and can be determined by applying a defined angular velocity to it. This value changes very little over temperature and time.

6.2 Zero-*g* and zero rate level

Linear acceleration zero-*g* level offset (TyOff) describes the deviation of an actual output signal from the ideal output signal if no acceleration is present. A sensor in a steady state on a horizontal surface will measure 0 *g* on both the X-axis and Y-axis, whereas the Z-axis will measure 1 *g*. Ideally, the output is in the middle of the dynamic range of the sensor (content of OUT registers 00h, data expressed as two's complement number). A deviation from the ideal value in this case is called zero-*g* offset.

Offset is to some extent a result of stress to MEMS sensor and therefore the offset can slightly change after mounting the sensor onto a printed circuit board or exposing it to extensive mechanical stress. Offset changes little over temperature, see "Linear acceleration zero-*g* level change vs. temperature" in *Table 4*. The zero-*g* level tolerance (TyOff) describes the standard deviation of the range of zero-*g* levels of a group of sensors.

Zero-rate level describes the actual output signal if there is no angular rate present. The zero-rate level of precise MEMS sensors is, to some extent, a result of stress to the sensor and therefore the zero-rate level can slightly change after mounting the sensor onto a printed circuit board or after exposing it to extensive mechanical stress. This value changes very little over temperature and time.

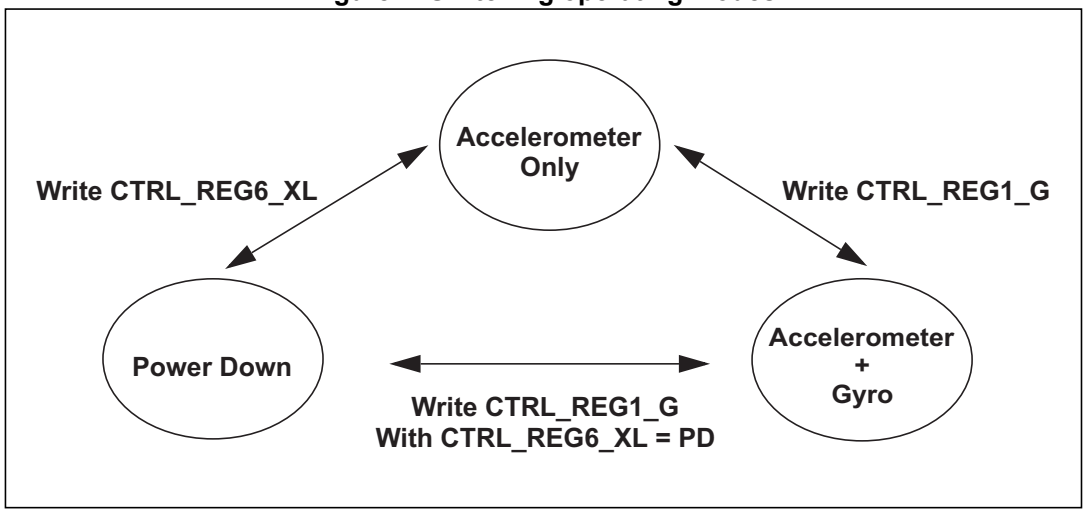
7 Device operating modes

7.1 Accelerometer and gyroscope operating modes

The LSM6DB0 has two operating modes available: only accelerometer active and gyroscope in power down or both accelerometer and gyroscope sensors active at the same ODR. Switching from one mode to the other requires one write operation: writing to *CTRL_REG6_XL (20h)* the accelerometer operates in normal mode and the gyroscope is powered down, writing to *CTRL_REG1_G (10h)* both the accelerometer and gyroscope are activated at the same ODR.

Figure 7 depicts both modes of operation from power down.

Figure 7. Switching operating modes



7.2 Gyroscope power modes

In the LSM6DB0, the gyroscope can be configured in three different operating modes: power-down, low-power and normal mode.

Low-power mode is available for lower ODR (14.9, 59.5, 119 Hz) while for greater ODR (238, 476, 952 Hz), the device is automatically in normal mode. *Table 9* summarizes the ODR configuration (ODR_G[2:0] bits set in *CTRL_REG1_G (10h)*) and corresponding power modes.

To enable low-power mode, the LP_mode bit in *CTRL_REG3_G (12h)* has to be set to ‘1’.

Low-power mode allows reaching low power consumption while maintaining the device always on, refer to *Table 10*.

The turn-on time to change from all operating modes for the gyroscope and accelerometer is indicated in *Table 11* and *Table 12*.

Table 9. Gyroscope operating mode

ODR_G [2:0]	ODR [Hz]	Power mode(1)
000	Power-down	Power-down
001	14.9	Low-power
010	59.5	Low-power
011	119	Low-power
100	238	Normal mode
101	476	Normal mode
110	952	Normal mode

1. Gyroscope low-power mode is available for G_FS = ±2000 dps.

Table 10. Operating mode current consumption

ODR [Hz]	Power mode	Current consumption(1) [mA]
14.9	Low-power	1.8
59.5	Low-power	2.3
119	Low-power	2.9
238	Normal mode	4.3
476	Normal mode	4.3
952	Normal mode	4.3

1. Gyroscope and accelerometer current consumption typical values based on characterization data.

Table 11. Gyroscope turn-on time

ODR [Hz]	LPF1 only(1)	LPF1 and LPF2(1)
14.9	2	LPF2 not available
59.5 or 119	3	13
238	4	14
476	5	15
952	8	18

1. The table contains the number of samples to be discarded after switching between low-power mode and normal mode.

Table 12. Accelerometer turn-on time

ODR [Hz]	BW = 400 Hz(1)	BW = 200 Hz(1)	BW = 100 Hz(1)	BW = 50 Hz(1)
14.9	0	0	0	0
59.5	0	0	0	0
119	1	1	1	2
238	1	1	2	4
476	1	2	4	7
952	2	4	7	14

1. The table contains the number of samples to be discarded after switching between power-down mode and normal mode.

7.3 Microprocessor operating modes

Several microprocessor operating modes are defined for the LSM6DB0:

- Reset mode
- Two low-power modes: low-power wait-for-interrupt (WFI) mode and high-power wait-for-interrupt (WFI) mode
- Active mode

In reset mode the LSM6DB0 is in ultra-low-power consumption: no voltage regulators, nor clocks are powered. The LSM6DB0 enters reset mode by asserting the external reset signal.

While in low-power WFI mode, the LSM6DB0 CPU is stopped and the high-frequency 80 MHz RC oscillator is powered down. All peripherals, apart from one timer, are disabled. The power consumption is about 800 µA with a 1 kHz clock.

In high-power WFI mode, the CPU is stopped and the high-frequency 80 MHz RC oscillator is powered up. This mode allows a faster response time for an interrupt to wake up the CPU. All peripherals are enabled and can wake up the CPU with an interrupt. The power consumption in this mode is around 2 mA with an 80 MHz clock.

In active mode the LSM6DB0 is fully operational: all interfaces, including SPI, I^2C, JTAG and UART, are active as well as all internal power supplies together with the high-speed frequency oscillator. The MCU core is also running.

Table 13 summarizes the modes of operation and transition times.

Table 13. LSM6DB0 operating modes

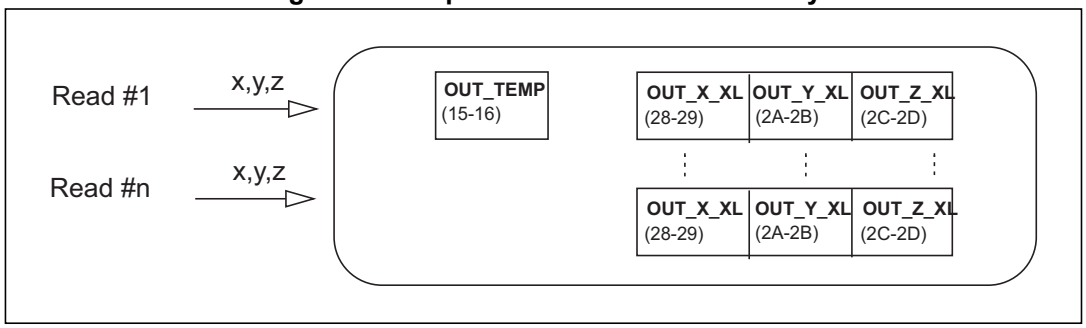
IP	Active mode	High-power WFI mode	Low-power WFI mode
CPU	Yes	Yes	Yes
Flash			
SRAM			
BOR			Yes
POR			
High-speed internal osc.			No
Low-speed internal osc.			Yes
Timer			Yes
SPI			No
I²C			
UART			
WDG			Yes
GPIOs			Yes
Wake-up time to active mode	0 µs	50 ns	300 µs
Consumption (typ)	10 mA	3 mA	800 µA

8 Accelerometer and gyroscope functionality

8.1 Multiple reads (burst)

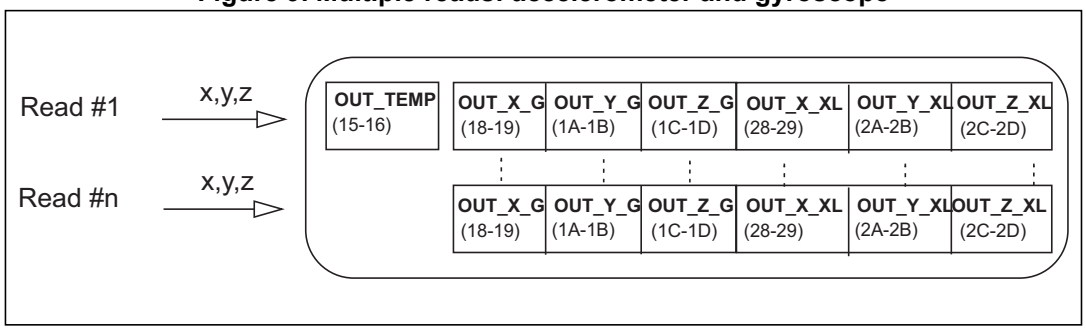
When only the accelerometer is activated and the gyroscope is in power down, starting from *OUT_X_XL (28h - 29h)* multiple reads can be performed. Once *OUT_Z_XL (2Ch - 2Dh)* is read, the system automatically restarts from *OUT_X_XL (28h - 29h)* (see *Figure 8*).

Figure 8. Multiple reads: accelerometer only



When both accelerometer and gyroscope sensors are activated at the same ODR, starting from *OUT_X_G (18h - 19h)* multiple reads can be performed. Once *OUT_Z_XL (2Ch - 2Dh)* is read, the system automatically restarts from *OUT_X_G (18h - 19h)* (see *Figure 9*).

Figure 9. Multiple reads: accelerometer and gyroscope



8.2 FIFO

The LSM6DB0 embeds a 32 slots of 16-bit data FIFO for each of the gyroscope's three output channels, yaw, pitch and roll, and 16-bit data FIFO for each of the accelerometer's three output channels, X, Y and Z. This allows consistent power saving for the system, since the host processor does not need to continuously poll data from the sensor, but it can wake up only when needed and burst the significant data out from the FIFO. This buffer can work accordingly to five different modes: Bypass mode, FIFO-mode, Continuous mode, Continuous-to-FIFO mode and Bypass-to-Continuous. Each mode is selected by the FMODE [2:0] bits in the *FIFO_CTRL (2Eh)* register. Programmable FIFO threshold status, FIFO overrun events and the number of unread samples stored are available in the *FIFO_SRC (2Fh)* register and can be set to generate dedicated interrupts on the INT1 pin using the *INT1_CTRL (0Ch)* register.

FIFO_SRC (2Fh) (FTH) goes to '1' when the number of unread samples (*FIFO_SRC (2Fh)* (FSS5:0)) is greater than or equal to FTH [4:0] in *FIFO_CTRL (2Eh)*. If *FIFO_CTRL (2Eh)* (FTH[4:0]) is equal to 0, *FIFO_SRC (2Fh)* (FTH) goes to '0'.

FIFO_SRC (2Fh) (OVRN) is equal to '1' if a FIFO slot is overwritten.

FIFO_SRC (2Fh) (FSS [5:0]) contains stored data levels of unread samples. When FSS [5:0] is equal to '000000', FIFO is empty, when FSS [5:0] is equal to '100000', FIFO is full and the unread samples are 32.

The FIFO feature is enabled by writing '1' in *CTRL_REG9 (23h)* (FIFO_EN).

To guarantee the correct acquisition of data during the switching into and out of FIFO mode, the first sample acquired must be discarded.

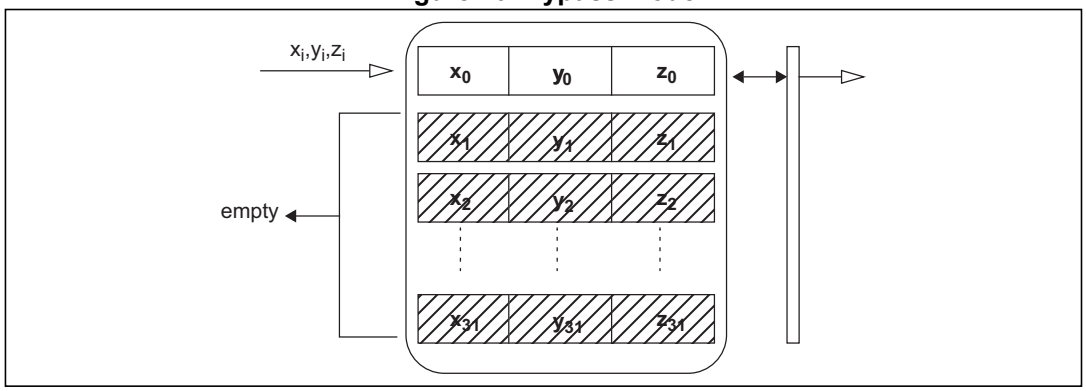
8.2.1 Bypass mode

In Bypass mode (*FIFO_CTRL (2Eh)*(FMODE [2:0]= 000), the FIFO is not operational and it remains empty.

Bypass mode is also used to reset the FIFO when in FIFO mode.

As described in *Figure 10*, for each channel only the first address is used. When a new data is available the old data is overwritten.

Figure 10. Bypass mode



8.2.2 FIFO mode

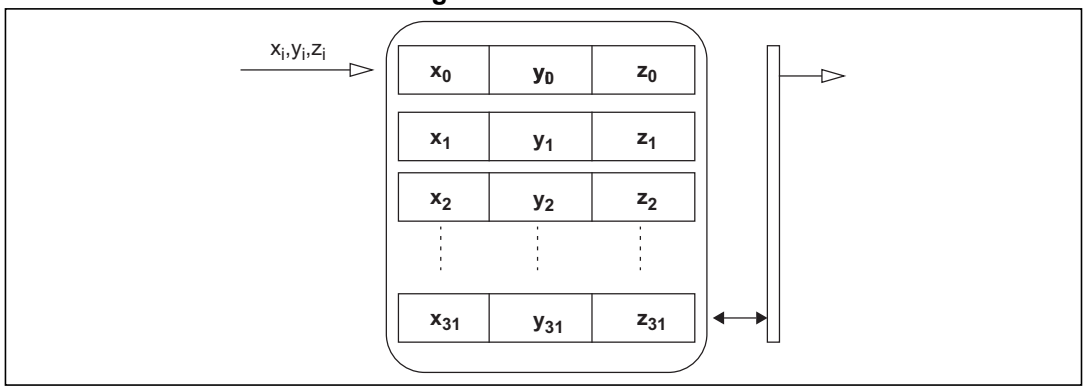
In FIFO mode (*FIFO_CTRL (2Eh)* (FMODE [2:0] = 001) data from the output channels are stored in the FIFO until it is overwritten.

To reset FIFO content, Bypass mode should be selected by writing *FIFO_CTRL (2Eh)* (FMODE [2:0]) to '000'. After this reset command, it is possible to restart FIFO mode, writing *FIFO_CTRL (2Eh)* (FMODE [2:0]) to '001'.

The FIFO buffer memorizes 32 levels of data but the depth of the FIFO can be resized by setting the STOP_ON_FTH bit in *CTRL_REG9 (23h)*. If the STOP_ON_FTH bit is set to '1', FIFO depth is limited to *FIFO_CTRL (2Eh)*(FTH [4:0]) + 1 data.

A FIFO threshold interrupt can be enabled (INT_OVR bit in *INT1_CTRL (0Ch)*) in order to be raised when the FIFO is filled to the level specified by the FTH[4:0] bits of *FIFO_CTRL (2Eh)*. When a FIFO threshold interrupt occurs, the first data has been overwritten and the FIFO stops collecting data from the input channels.

Figure 11. FIFO mode



8.2.3 Continuous mode

Continuous mode (*FIFO_CTRL (2Eh)*(FMODE[2:0] = 110) provides a continuous FIFO update: as new data arrives, the older is discarded.

A FIFO threshold flag *FIFO_SRC (2Fh)*(FTH) is asserted when the number of unread samples in FIFO is greater than or equal to *FIFO_CTRL (2Eh)*(FTH4:0).

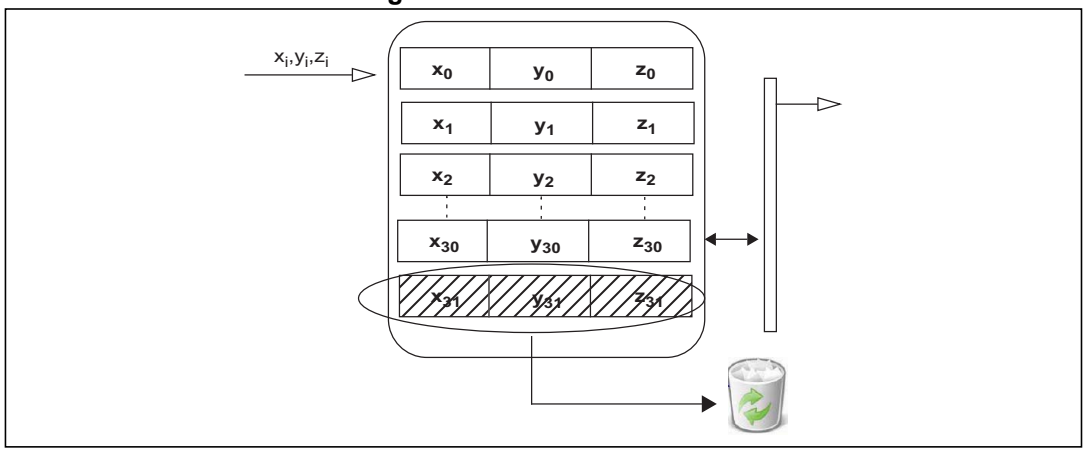
It is possible to route *FIFO_SRC (2Fh)*(FTH) to the INT1 pin by writing the INT_FTH bit to '1' in register *INT1_CTRL (0Ch)*.

A full-flag interrupt can be enabled, *INT1_CTRL (0Ch)* (INT_ FSS5)= '1', when the FIFO becomes saturated and in order to read the contents all at once.

If an overrun occurs, the oldest sample in FIFO is overwritten and the OVRN flag in *FIFO_SRC (2Fh)* is asserted.

In order to empty the FIFO before it is full, it is also possible to pull from FIFO the number of unread samples available in *FIFO_SRC (2Fh)* (FSS[5:0]).

Figure 12. Continuous mode



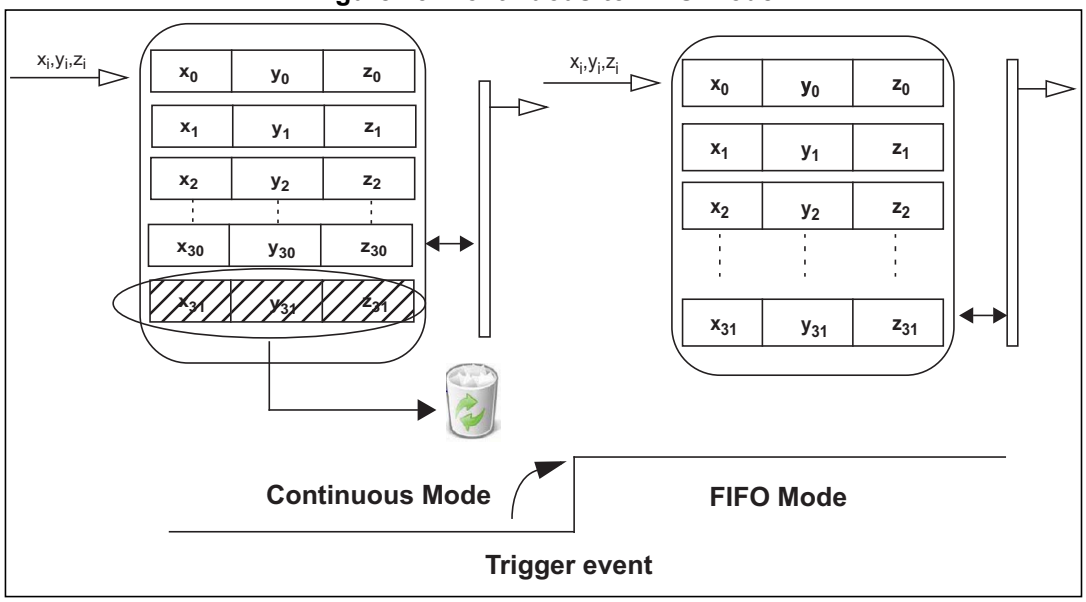
8.2.4 Continuous-to-FIFO mode

In Continuous-to-FIFO mode (*FIFO_CTRL (2Eh)*(FMODE [2:0] = 011), FIFO behavior changes according to the *INT1_GEN_SRC_XL (26h)*(IA1_XL) bit. When *INT1_GEN_SRC_XL (26h)*(IA1_XL) bit is equal to '1' FIFO operates in FIFO mode, when *INT1_GEN_SRC_XL (26h)*(IA1_XL) bit is equal to '0' FIFO operates in Continuous mode.

The interrupt generator should be set to the desired configuration by means of *INT_GEN_CFG1_XL (06h)*, *INT_GEN_THS1_X_XL (07h)*, *INT_GEN_THS1_Y_XL (08h)*and *INT_GEN_THS1_Z_XL (09h)*.

The *CTRL_REG4 (1Eh)*(LIR_XL) bit should be set to '1' in order to have latched interrupt.

Figure 13. Continuous-to-FIFO mode



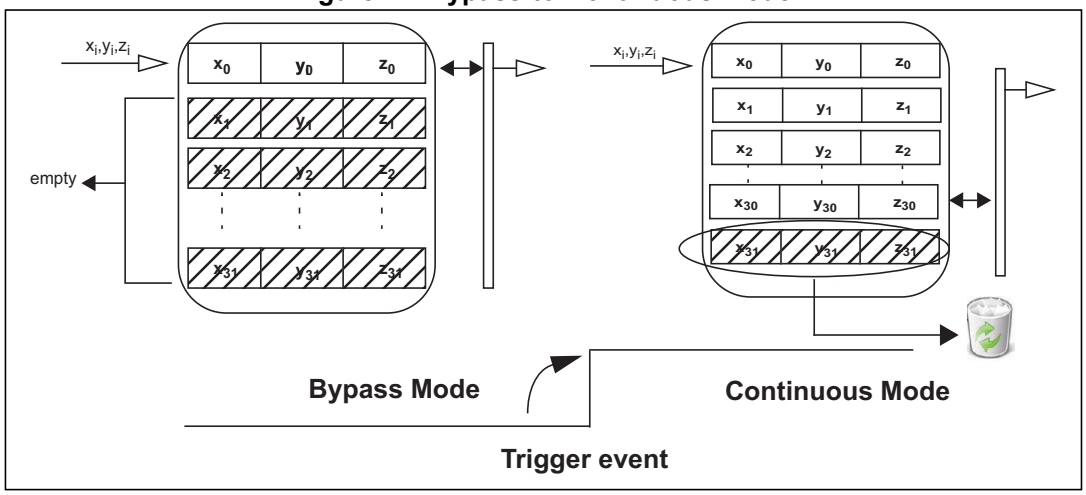
8.2.5 Bypass-to-Continuous mode

In Bypass-to-Continuous mode (*FIFO_CTRL (2Eh)*(FMODE[2:0] = '100'), data measurement storage inside FIFO operates in Continuous mode when *INT1_GEN_SRC_XL (26h)*(IA1_XL) is equal to '1', otherwise FIFO content is reset (Bypass mode).

The interrupt generator should be set to the desired configuration by means of *INT_GEN_CFG1_XL (06h)*, *INT_GEN_THS1_X_XL (07h)*, *INT_GEN_THS1_Y_XL (08h)* and *INT_GEN_THS1_Z_XL (09h)*.

The *CTRL_REG4 (1Eh)*(LIR_XL) bit should be set to '1' in order to have latched interrupt.

Figure 14. Bypass-to-Continuous mode



8.3 Digital interface

The sensors embedded inside the LSM6DB0 can be accessed by the microcontroller through the I^2C serial interface. The serial interfaces are mapped to the same pins.

Table 14. Serial interface pin description

Pin name	Pin description
Master SCL (I2C1_SCL)	I2C serial clock (SCL_X/G)
Master SDA (I2C1_SDA)	I2C serial data (SDA_X/G)

8.3.1 I^2C serial interface

The LSM6DB0 I^2C is a bus slave. The I^2C is employed to write data into registers whose content can also be read back.

The relevant I^2C terminology is given in the following table.

Table 15. Serial interface pin description

Term	Description
Transmitter	The device which sends data to the bus
Receiver	The device which receives data from the bus
Master	The device which initiates a transfer, generates clock signals and terminates a transfer
Slave	The device addressed by the master

There are two signals associated with the I^2C bus: the serial clock line (SCL_X/G) and the serial data line (SDA_X/G). The latter is a bi-directional line used for sending and receiving the data to/from the interface. Both lines must be connected to VDDA through an external pull-up resistor. When the bus is free, both lines are high.

The I^2C interface is compliant with fast mode (400 kHz) I^2C standards as well as with normal mode.

In order to disable the I^2C block, the I2C_disable bit must be written to '1' in *CTRL_REG9 (23h)*

8.3.2 I^2C operation

The transaction on the bus is started through a start (ST) signal. A start condition is defined as a high-to-low transition on the data line while the SCL_X/G line is held high. After this has been transmitted by the master, the bus is considered busy. The next byte of data transmitted after the start condition contains the address of the slave in the first 7 bits and the eighth bit tells whether the master is receiving data from the slave or transmitting data to the slave. When an address is sent, each device in the system compares the first seven bits after a start condition with its address. If they match, the device considers itself addressed by the master.

The slave address (SAD) associated to the LSM6DB0 accelerometer is 1101011b.

Data transfer with acknowledge is mandatory. The transmitter must release the SDA_X/G line during the acknowledge pulse. The receiver must then pull the data line low so that it remains stable low during the high period of the acknowledge clock pulse. A receiver which has been addressed is obliged to generate an acknowledge after each byte of data received.

The I^2C embedded inside the LSM6DB0 behaves like a slave device and the following protocol must be adhered to. After the start condition (ST) a slave address is sent, once a slave acknowledge (SAK) has been returned, an 8-bit sub-address (SUB) is transmitted. Incrementing the address is configured by *CTRL_REG8 (22h)* (IF_ADD_INC).

The slave address is completed with a Read/Write bit. If the bit was '1' (Read), a repeated START (SR) condition must be issued after the two sub-address bytes. If the bit is '0' (Write) the master will transmit to the slave with direction unchanged. *Table 16* explains how the SAD+Read/Write bit pattern is composed, listing all the possible configurations.

Table 16. SAD+Read/Write patterns

Command	SAD[6:1]	SAD[0] = SA0	R/W	SAD+R/W
Read	110101	1	1	11010111 (D7h)
Write	110101	1	0	11010110 (D6h)

Table 17. Transfer when master is writing one byte to slave

Master	ST	SAD + W		SUB		DATA		SP
Slave			SAK		SAK		SAK	

Table 18. Transfer when master is writing multiple bytes to slave

Master	ST	SAD + W		SUB		DATA		DATA		SP
Slave			SAK		SAK		SAK		SAK	

Table 19. Transfer when master is receiving (reading) one byte of data from slave

Master	ST	SAD + W		SUB		SR	SAD + R			NMAK	SP
Slave			SAK		SAK			SAK	DATA		

Table 20. Transfer when master is receiving (reading) multiple bytes of data from slave

Master	ST	SAD+W		SUB		SR	SAD+R			MAK		MAK		NMAK	SP
Slave			SAK		SAK			SAK	DATA		DAT A		DATA		

Data are transmitted in byte format (DATA). Each data transfer contains 8 bits. The number of bytes transferred per transfer is unlimited. Data is transferred with the Most Significant bit (MSb) first. If a receiver can't receive another complete byte of data until it has performed some other function, it can hold the clock line, SCL low, to force the transmitter into a wait state. Data transfer only continues when the receiver is ready for another byte and releases the data line. If a slave receiver doesn't acknowledge the slave address (i.e. it is not able to receive because it is performing some real-time function) the data line must be left high by the slave. The master can then abort the transfer. A low-to-high transition on the SDA_X/G line while the SCL_X/G line is high is defined as a STOP condition. Each data transfer must be terminated by the generation of a STOP (SP) condition.

In the presented communication format, MAK is Master acknowledge and NMAK is No Master Acknowledge.

9 Microprocessor functionality

9.1 ARM Cortex-M0 core

The ARM Cortex-M0 processor is a very low gate count, energy-efficient processor. It has been developed to provide an energy-efficient processor for microcontrollers and embedded applications requiring an area-optimized processor. The ARM Cortex-M0 32-bit RISC processor uses Thumb-2® technology, providing a blend of 16/32-bit instructions delivering a smaller code size to 8-bit and 16-bit architectures.

Owing to its embedded ARM core, the LSM6DB0 is compatible with all ARM tools and software.

9.1.1 Nested vectored interrupt controller (NVIC)

The ARM Cortex-M0 processor supports up to 32 interrupt requests (IRQ), a non-maskable interrupt (NMI), and various system exceptions. The NVIC and the ARM Cortex-M0 processor core are closely coupled and provide:

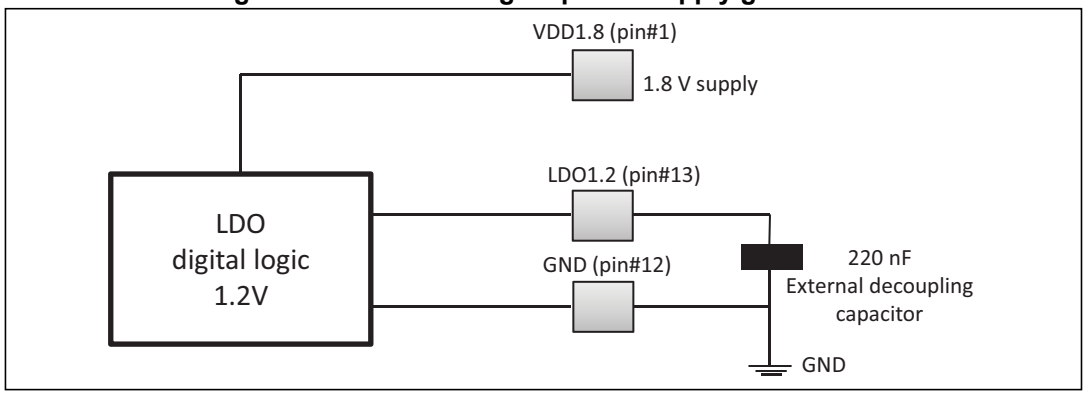
- Low-latency interrupt processing
- Four interrupt priority levels
- Efficient processing of late-arriving interrupts and higher priority interrupts
- Support for tail-chaining

9.2 Power supply scheme

- VDD[(c)] = 1.8 V to 3.3 V: external power supply for master serial port (DIO6 to DIO10). Provided through VDD pin.
- VDD1.8[(c)] = 1.8 V: external power supply for internal regulator. Provided through VDD1.8 pin.

The LSM6DB0 integrates an LDO regulator which is used to generate the power supply for the internal digital circuitry. The LDO supplies 1.2 V for the digital blocks and requires a decoupling capacitor for stable operation.

Figure 15. LSM6DB0 digital power supply generation



c. For minimum and maximum operating conditions of VDD and VDD1.8 refer to *Table 6*.

9.3 Reset management

The device has an integrated brownout reset (BOR) circuit and an integrated power-on reset (POR).

In the LSM6DB0, the BOR threshold is 1.5 V. When V_{DD} is below this threshold, the device is in reset. The BOR is always active in the LSM6DB0 at power-on.

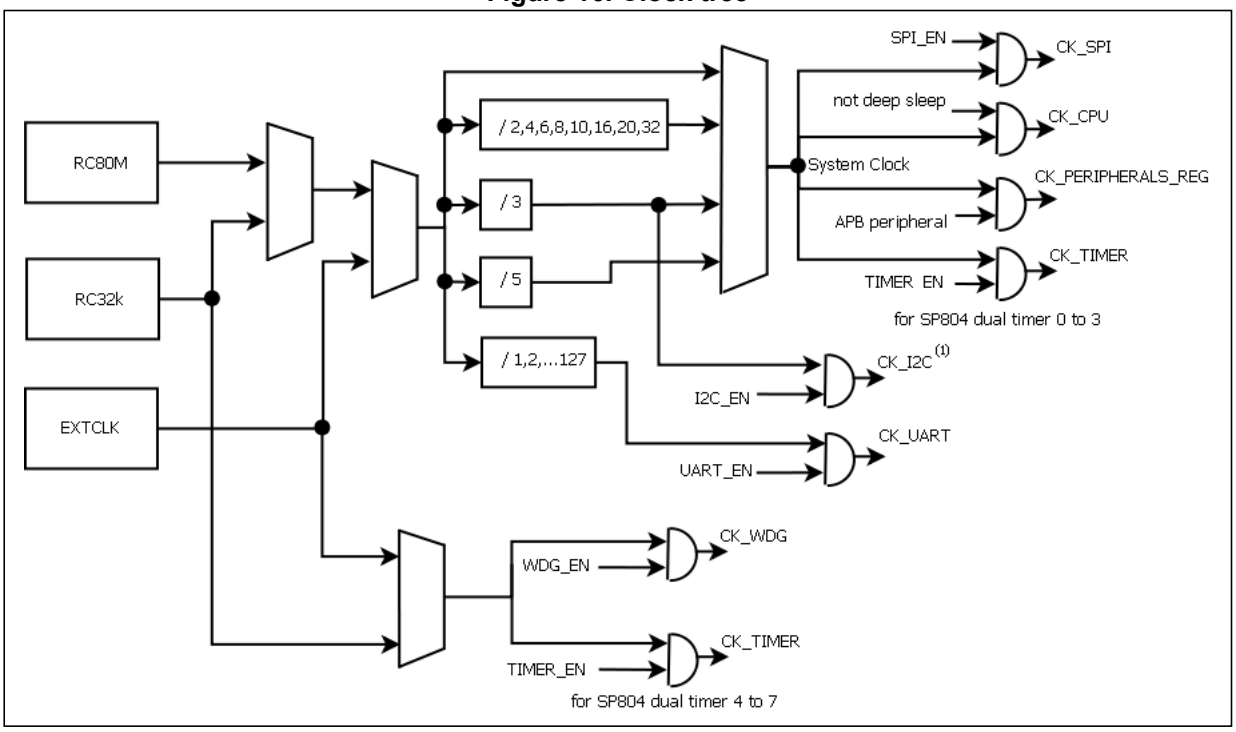
The POR circuit is activated when the LDO has stabilized. The startup time of the LSM6DB0 at power-on is typically 1 ms with the BOR active.

9.4 Boot mode

At startup, the LSM6DB0 boots from a reserved section of the Flash memory programmed by ST during production. It is used to adjust accurately the oscillator frequencies and contains manufacturing information. Any interference with this initialization sequence can degrade the performance of the device. At the end of this sequence, the system boots from the main Flash which contains the user's program.

9.5 Clock management

Figure 16. Clock tree



1. Same clock supply for both I^2C

The clock management block distributes clocks from various clock sources to the CPU and peripherals. The clock management block is comprised of the following circuitry and switches:

- Clock divider: the system contains various clock dividers which allow the frequency of the peripherals and CPU clock sources to be changed.
- Glitch-free clock switching: the clock sources can be changed dynamically and securely in active mode.
- Clock gating: the peripherals can have their clocks gated off to reduce their power consumption.
- Three system clock sources:
  - RC80M 80 MHz internal RC oscillator which is trimmed at 1% accuracy with factory settings
  - RC32K 32 kHz internal RC oscillator which is trimmed at 1% accuracy with factory settings
  - EXTCLK external clock up to 80 MHz
- Watchdog clock sources: the RC32k or EXTCLK.
- I^2C clock source: system clock divided by 3.
- UART clock source: system clock divided by a programmable division factor between 1 and 127.
- SPI clock source: clock synchronous to the processor.
- Dual timers: four timers clocked by 32 kHz clock pulses synchronous to the system clock sources and four timers clocked on a clock synchronous to the processor clock.
- Clock-out capability: either the 32 kHz clock or the output of the divide-by-5 clock can be output on a GPIO for external use.

9.6 General-purpose inputs/outputs (GPIOs)

The LSM6DB0 contains up to 11 GPIO pins each of which can be configured by software as output, as input (either pull-up or pull-down), or as an alternate function in serial mode 0 or serial mode1 (see *Table 21*). Each of the GPIOs can also be used as an external interrupt source.

Table 21. Alternate function input/output

Pin name	Serial mode 0		Serial mode 1		GPIO mode	
	Direction	Function	Direction	Function	Direction	Function
IO0	Input/Output	JTAG TMS / SW_TDIO	Input	UART CTS	Input/Output	GPIO
IO1	Input	JTAG TCK / SW_TCK	Output	UART RTS		
IO2	Input/Output	I^2C2_SCL		UART TXD		
IO3		I^2C2_SDA	Input	UART RXD		
IO4	Output	JTAG TDO		None		
IO5	Input	JTAG TDI		Clock input		
IO6	Output	16 MHz clock	Output	32 kHz clock		
IO7	Input/Output	I^2C1_SCL	Input/Output	SPI SCLK		
IO8		I^2C1_SDA	Output	SPI output		
IO9	Input	IRQ input	Input	SPI CS		
IO10				SPI input		

9.7 Memories

The LSM6DB0 has the following memory features:

- Flash memory with 0 wait states at 26.66 MHz and 2 wait states at 80 MHz
- SRAM with ECC for data and program access (read/write) referred to as RAM bank0
- SRAM for data and program access (read/write) referred to as RAM bank1
- Memory protection: the Flash and RAM memory banks cannot be read from or written to by the JTAG link if the debug features are connected.

9.8 Timers and watchdogs

The LSM6DB0 includes eight dual timers, one WDG timer, and a SysTick timer.

9.8.1 Dual timer

The dual-timer features are listed below. They consist of two identical programmable free-running counters (FRCs) that can be configured for 32-bit or 16-bit operations. The FRCs operate from a common timer clock which must be synchronous to the CPU clock.

- 16/32-bit down counter
- Interrupt generation when the counter reaches zero
- Free-running mode: the counter operates continuously and wraps around to its maximum value each time it reaches zero.
- Periodic mode: the counter operates continuously by reloading the programmed value each time it reaches zero.
- One-shot mode: the counter decrements to zero and then halts until it is reprogrammed
- The timer clock prescaler factors are 1, 16, or 256

9.8.2 Watchdog (WDG) timer

The WDG timer is a 32-bit down counter which operates on either the RC32k clock or the EXTCLK clock. It can generate an interrupt and/or a reset when the counter reaches zero.

9.8.3 System tick (SysTick) timer

The SysTick timer provides a 24-bit clear-on-write, decrementing counter which wraps around when it reaches zero. It operates on the CPU clock.

9.9 Communication interfaces

9.10 I²C bus

The LSM6DB0 provides two I²C interfaces which can operate in master and slave modes. They can support standard mode and fast mode.

9.11 Universal asynchronous receiver transmitter (UART)

The UART interface (IO0, IO1, IO2, IO3 pins) of the LSM6DB0 supports the following maximum baud rates:

- 921600 bps in UART mode
- 460800 bps in Infrared data association (IrDA) mode
- 115200 bps in low-power IrDA mode

The interface supports the IrDA serial infrared (SIR) ENDEC and also provides flow control capabilities through the hardware management of the clear-to-send (CTS) and request-to-send (RTS) signals.

For more details, refer to the ARM document “DDIO83G_uart_pl011_trm.pdf”.

9.12 Serial peripheral interface (SPI)

The SPI interface operates as a master or slave interface. This interface supports 6 MHz bit rate max in slave mode and 16 MHz bit rate max in master mode due to the limitation of the IOs. A programmable clock prescaler inside the SPI allows the input clock to be divided by a factor of 2 to 254 in steps of two to provide the serial output clock. The SPI interface provides data frames between 4 and 16 bits long.

For more details, refer to the ARM document “DDIO94C_ssp_PL022_trm.pdf”.

9.13 JTAG and SW debug support

The ARM JTAG debug port is embedded which enables debug using a standard JTAG connection. The ARM SWD (serial wire debug) port is also embedded which enables serial wire debug to be connected to the CPU. The JTAG TMS and TCK pins are shared with the SW_TDIO and SW_TCK respectively.

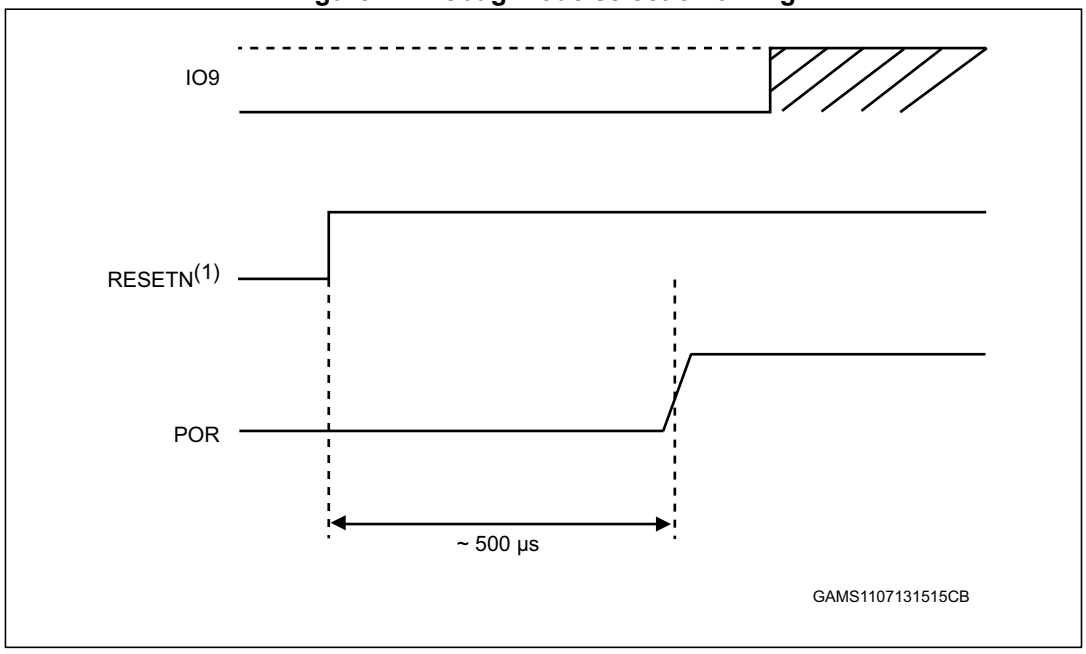
The two debug mode mechanisms can be selected by driving the IO9 pin during reset: JTAG debug mode is selected by setting the IO9 pin to zero, while SWD mode is selected by setting the IO9 pin to 1.

Table 22. Debug mode selection

POR	IO9	Debug mode
0	0	JTAG: SOC(1) + CPU TAP(2) selected
0	1	SW: CPU TAP(2) selected
1	X(3)	JTAG or SW available

1. SOC = chip and processor
2. TAP = test access port
3. X = don't care

Figure 17. Debug mode selection timing



1. RESETN needs an external pull-up if not driven
1. Default option depending on software configuration

10 Absolute maximum ratings

10.1 Accelerometer and gyroscope

Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 23. Absolute maximum ratings

Symbol	Ratings	Maximum value	Unit
VDD	Supply voltage	-0.3 to 4.8	V
T_{STG}	Storage temperature range	-40 to +125	°C
Sg	Acceleration *g* for 0.1 ms	10,000	*g*
ESD	Electrostatic discharge protection (HBM)	2	kV
Vin	Input voltage on any control pin (including CS, SCL/SPC, SDA/SDI/SDO, SDO/SA0)	0.3 to Vdd_IO +0.3	V

Note: Supply voltage on any pin should never exceed 4.8 V

This device is sensitive to mechanical shock, improper handling can cause permanent damage to the part.

This device is sensitive to electrostatic discharge (ESD), improper handling can cause permanent damage to the part.

10.2 Microprocessor

Absolute maximum ratings are those values above which damage to the device may occur. Functional operation under these conditions is not implied. All voltages are in reference to GND.

Table 24. Absolute maximum ratings for microprocessor

Pin	Parameter	Value (min to max)	Unit
13	DC voltage on linear voltage regulator	-0.3 to +1.8	V
9, 10, 11, 15, 16	DC voltage on digital output pins	-0.3 to +3.6	
2, 3, 4, 6, 7, 8		-0.3 to +1.8	
5	DC voltage on analog pins	-0.3 to +1.8	
7, 8	DC voltage on RF/XTAL pins	-0.3 to +1.8	
T_{STG}	Storage temperature range	-40 to +125	°C
$V_{ESD-HBM}$	Electrostatic discharge voltage	±2.0	kV

11 Register mapping

The table given below provides a list of the 8/16 bit registers of the motion sensors and the corresponding addresses.

Table 25. Motion sensor registers

Name	Type	Register address		Default	Note
		Hex	Binary		
Reserved		00	00000000	--	Reserved
INT_GEN_CFG2_XL	r/w	01	00000001	00000000	
INT_GEN_THS2_XL	r/w	02	00000010	00000000	
INT_GEN_DUR2_XL	r/w	03	00000011	00000000	
ACT_THS	r/w	04	00000100	00000000	
ACT_DUR	r/w	05	00000101	00000000	
INT_GEN_CFG1_XL	r/w	06	00000110	00000000	
INT_GEN_THS1_X_XL	r/w	07	00000111	00000000	
INT_GEN_THS1_Y_XL	r/w	08	00001000	00000000	
INT_GEN_THS1_Z_XL	r/w	09	00001001	00000000	
INT_GEN_DUR1_XL	r/w	0A	00001010	00000000	
REFERENCE_G	r/w	0B	00001011	00000000	
INT1_CTRL	r/w	0C	00001100	00000000	
INT2_CTRL	r/w	0D	00001101	00000000	
Reserved	--	0E	--	--	Reserved
WHO_AM_I	r	0F	00001111	01101000	
CTRL_REG1_G	r/w	10	00010000	00000000	
CTRL_REG2_G	r/w	11	00010001	00000000	
CTRL_REG3_G	r/w	12	00010010	00000000	
ORIENT_CFG_G	r/w	13	00010011	00000000	
INT_GEN_SRC_G	r	14	00010100	output	
OUT_TEMP_L	r	15	00010101	output	
OUT_TEMP_H	r	16	00010110	output	
STATUS_REG	r	17	00010111	output	
OUT_X_L_G	r	18	00011000	output	
OUT_X_H_G	r	19	00011001	output	
OUT_Y_L_G	r	1A	00011010	output	
OUT_Y_H_G	r	1B	00011011	output	
OUT_Z_L_G	r	1C	00011100	output	
OUT_Z_H_G	r	1D	00011101	output	

Table 25. Motion sensor registers (continued)

Name	Type	Register address		Default	Note
		Hex	Binary		
CTRL_REG4	r/w	1E	00011110	00111000	
CTRL_REG5_XL	r/w	1F	00011111	00111000	
CTRL_REG6_XL	r/w	20	00100000	00000000	
CTRL_REG7_XL	r/w	21	00100001	00000000	
CTRL_REG8	r/w	22	00100010	00000100	
CTRL_REG9	r/w	23	00100011	00000000	
CTRL_REG10	r/w	24	00100100	00000000	
INT2_GEN_SRC_XL	r	25	00100101	output	
INT1_GEN_SRC_XL	r	26	00100110	output	
STATUS_REG	r	27	00100111	output	
OUT_X_L_XL	r	28	00101000	output	
OUT_X_H_XL	r	29	00101001	output	
OUT_Y_L_XL	r	2A	00101010	output	
OUT_Y_H_XL	r	2B	00101011	output	
OUT_Z_L_XL	r	2C	00101100	output	
OUT_Z_H_XL	r	2D	00101101	output	
FIFO_CTRL	r/w	2E	00101110	00000000	
FIFO_SRC	r	2F	00101111	output	
INT_GEN_CFG_G	r/w	30	00110000	00000000	
INT_GEN_THS_XH_G	r/w	31	00110001	00000000	
INT_GEN_THS_XL_G	r/w	32	00110010	00000000	
INT_GEN_THS_YH_G	r/w	33	00110011	00000000	
INT_GEN_THS_YL_G	r/w	34	00110100	00000000	
INT_GEN_THS_ZH_G	r/w	35	00110101	00000000	
INT_GEN_THS_ZL_G	r/w	36	00110110	00000000	
INT_GEN_DUR_G	r/w	37	00110111	00000000	
Reserved	r	38-7F	--	--	Reserved

Registers marked as *Reserved* must not be changed. Writing to those registers may cause permanent damage to the device.

To guarantee proper behavior of the device, all registers addresses not listed in the above table must not be accessed and the content stored on those registers must not be changed.

The content of the registers that are loaded at boot should not be changed. They contain the factory calibration values. Their content is automatically restored when the device is powered up.

12 Register description

The device contains a set of registers which are used to control its behavior and to retrieve linear acceleration, angular rate and temperature data. The register addresses, made up of 7 bits, are used to identify them and to write the data through the serial interface.

12.1 INT_GEN_CFG2_XL (01h)

Linear acceleration sensor interrupt generator 2 configuration register (r/w).

Table 26. INT_GEN_CFG2_XL register

AOI2_XL	6D2	ZHIE2_XL	ZLIE2_XL	YHIE2_XL	YLIE2_XL	XHIE2_XL	XLIE2_XL

Table 27. INT_GEN_CFG2_XL register description

AOI2_XL	And/Or combination of accelerometer's interrupt 2 events. Default value: 0. (0: OR combination; 1: AND combination)
6D2	6 direction detection function for interrupt 2. Default value: 0. (0: disabled; 1: enabled)
ZHIE2_XL	Enable interrupt 2 generation on accelerometer's Z-axis high event or on direction recognition. Default value: 0. (0: disable interrupt request; 1: enable interrupt request)
ZLIE2_XL	Enable interrupt 2 generation on accelerometer's Z-axis low event or on direction recognition. Default value: 0. (0: disable interrupt request; 1: enable interrupt request)
YHIE2_XL	Enable interrupt 2 generation on accelerometer's Y-axis high event or on direction recognition. Default value: 0. (0: disable interrupt request; 1: enable interrupt request)
YLIE2_XL	Enable interrupt 2 generation on accelerometer's Y-axis low event or on direction recognition. Default value: 0. (0: disable interrupt request; 1: enable interrupt request)
XHIE2_XL	Enable interrupt 2 generation on accelerometer's X-axis high event or on direction recognition. Default value: 0. (0: disable interrupt request; 1: enable interrupt request)
XLIE2_XL	Enable interrupt 2 generation on accelerometer's X-axis low event or on direction recognition. Default value: 0. (0: disable interrupt request; 1: enable interrupt request)

12.2 INT_GEN_THS2_XL (02h)

Linear acceleration sensor interrupt 2 threshold register (r/w).

Table 28. INT_GEN_THS2_XL register

THS2_XL7	THS2_XL6	THS2_XL5	THS2_XL4	THS2_XL3	THS2_XL2	THS2_XL1	THS2_XL0

Table 29. INT_GEN_THS2_XL register description

THS2_XL [7:0]	Interrupt 2 thresholds. Default value: 0000 0000

12.3 INT_GEN_DUR2_XL (03h)

Linear acceleration sensor interrupt 2 duration register (r/w).

Table 30. INT_GEN_DUR2_XL register

WAIT2_XL	DUR2_XL6	DUR2_XL5	DUR2_XL4	DUR2_XL3	DUR2_XL2	DUR2_XL1	DUR2_XL0

Table 31. INT_GEN_DUR2_XL register description

WAIT2_XL	Wait function enable on duration counter. Default value: 0. (0: wait function off; 1: wait for DUR2_XL [6:0] samples before exiting interrupt 2)
DUR2_XL [6:0]	Enter/exit interrupt 2 duration value. Default value: 000 0000

12.4 ACT_THS (04h)

Activity threshold register.

Table 32. ACT_THS register

SLEEP_ON_INACT_EN	ACT_THS6	ACT_THS5	ACT_THS4	ACT_THS3	ACT_THS2	ACT_THS1	ACT_THS0

Table 33. ACT_THS register description

SLEEP_ON_INACT_EN	Gyroscope operating mode during inactivity. Default value: 0 (0: Gyroscope in power-down; 1: Gyroscope in sleep mode)
ACT_THS [6:0]	Inactivity threshold. Default value: 000 0000.

12.5 ACT_DUR (05h)

Inactivity duration register.

Table 34. ACT_DUR register

ACT_DUR7	ACT_DUR6	ACT_DUR5	ACT_DUR4	ACT_DUR3	ACT_DUR2	ACT_DUR1	ACT_DUR0

Table 35. ACT_DUR register description

ACT_DUR [7:0]	Inactivity duration. Default value: 0000 0000

12.6 INT_GEN_CFG1_XL (06h)

Linear acceleration sensor interrupt 1 generator configuration register.

Table 36. INT_GEN_CFG1_XL register

AOI_XL	6D	ZHIE_XL	ZLIE_XL	YHIE_XL	YLIE_XL	XHIE_XL	XLIE_XL

Table 37. INT_GEN_CFG1_XL register description

AOI_XL	AND/OR combination of accelerometer's interrupt 1 events. Default value: 0 (0: OR combination; 1: AND combination)
6D	6-direction detection function for interrupt 1. Default value: 0 (0: disabled; 1: enabled)
ZHIE_XL	Enable interrupt 1 generation on accelerometer's Z-axis high event. Default value: 0 (0: disable interrupt request; 1: interrupt request on measured acceleration value higher than preset threshold)
ZLIE_XL	Enable interrupt 1 generation on accelerometer's Z-axis low event. Default value: 0 (0: disable interrupt request; 1: interrupt request on measured acceleration value lower than preset threshold)
YHIE_XL	Enable interrupt 1 generation on accelerometer's Y-axis high event. Default value: 0 (0: disable interrupt request; 1: interrupt request on measured acceleration value higher than preset threshold)
YLIE_XL	Enable interrupt 1 generation on accelerometer's Y-axis low event. Default value: 0 (0: disable interrupt request; 1: interrupt request on measured acceleration value lower than preset threshold)
XHIE_XL	Enable interrupt 1 generation on accelerometer's X-axis high event. Default value: 0 (0: disable interrupt request; 1: interrupt request on measured acceleration value higher than preset threshold)
XLIE_XL	Enable interrupt 1 generation on accelerometer's X-axis low event. Default value: 0 (0: disable interrupt request; 1: interrupt request on measured acceleration value lower than preset threshold)

12.7 INT_GEN_THS1_X_XL (07h)

Linear acceleration sensor interrupt 1 threshold register.

Table 38. INT_GEN_THS1_X_XL register

THS1_XL_X7	THS1_XL_X6	THS1_XL_X5	THS1_XL_X4	THS1_XL_X3	THS1_XL_X2	THS1_XL_X1	THS1_XL_X0

Table 39. INT_GEN_THS1_X_XL register description

THS1_XL_X [7:0]	X-axis interrupt threshold. Default value: 0000 0000

12.8 INT_GEN_THS1_Y_XL (08h)

Linear acceleration sensor interrupt 1 threshold register.

Table 40. INT_GEN_THS1_Y_XL register

THS1_XL_Y 7	THS1_XL_Y 6	THS1_XL_Y 5	THS1_XL_Y 4	THS1_XL_Y 3	THS1_XL_Y 2	THS1_XL_Y 1	THS1_XL_Y 0

Table 41. INT_GEN_THS1_Y_XL register description

THS1_XL_Y [7:0]	Y-axis interrupt threshold. Default value: 0000 0000

12.9 INT_GEN_THS1_Z_XL (09h)

Linear acceleration sensor interrupt 1 threshold register.

Table 42. INT_GEN_THS1_Z_XL register

THS1_XL_Z 7	THS1_XL_Z 6	THS1_XL_Z 5	THS1_XL_Z 4	THS1_XL_Z 3	THS1_XL_Z 2	THS1_XL_Z 1	THS1_XL_Z 0

Table 43. INT_GEN_THS_Z_XL register description

THS1_XL_Z [7:0]	Z-axis interrupt threshold. Default value: 0000 0000

12.10 INT_GEN_DUR1_XL (0Ah)

Linear acceleration sensor interrupt 1 duration register.

Table 44. INT_GEN_DUR1_XL register

WAIT_XL	DUR1_XL6	DUR1_XL5	DUR1_XL4	DUR1_XL3	DUR1_XL2	DUR1_XL1	DUR1_XL0

Table 45. INT_GEN_DUR1_XL register description

WAIT_XL	Wait function enabled on duration counter. Default value: 0 (0: wait function off; 1: wait for DUR_XL [6:0] samples before exiting interrupt)
DUR1_XL [6:0]	Enter/exit interrupt duration value. Default value: 000 0000

12.11 REFERENCE_G (0Bh)

Angular rate sensor reference value register for digital high-pass filter (r/w)

Table 46. REFERENCE_G register

REF7_G	REF6_G	REF5_G	REF4_G	REF3_G	REF2_G	REF1_G	REF0_G

Table 47. REFERENCE_G register description

REF_G [7:0]	Reference value for gyroscope's digital high-pass filter (r/w). Default value: 0000 0000

12.12 INT1_CTRL (0Ch)

INT1 pin control register.

Table 48. INT1_CTRL register

INT1_IG_G	INT1_IG_XL	INT1_FSS5	INT1_OVR	INT1_FTH	INT1_ Boot	INT1_DRDY_G	INT1_DRDY_XL

Table 49. INT1_CTRL register description

INT1_IG_G	Gyroscope interrupt enable on INT1 pin. Default value: 0 (0: disabled; 1: enabled)
INT_ IG_XL	Accelerometer interrupt generator on INT1 pin. Default value: 0 (0: disabled; 1: enabled)
INT_ FSS5	FSS5 interrupt enable on INT1 pin. Default value: 0 (0: disabled; 1: enabled)
INT_OVR	Overrun interrupt on INT1 pin. Default value: 0 (0: disabled; 1: enabled)
INT_FTH	FIFO threshold interrupt on INT1 pin. Default value: 0 (0: disabled; 1: enabled)
INT_ Boot	Boot status available on INT1 pin. Default value: 0 (0: disabled; 1: enabled)
INT_DRDY_G	Gyroscope data ready on INT1 pin. Default value: 0 (0: disabled; 1: enabled)
INT_DRDY_XL	Accelerometer data ready on INT1 pin. Default value: 0 (0: disabled; 1: enabled)

12.13 INT2_CTRL (0Dh)

INT2 pin control register.

Table 50. INT2_CTRL register

INT2_INACT	INT2_IG2_XL	INT2_FSS5	INT2_OVR	INT2_FTH	INT2_DRDY_TEMP	INT2_DRDY_G	INT2_DRDY_XL

Table 51. INT2_CTRL register description

INT2_INACT	Gyroscope interrupt enable on INT2 pin. Default value: 0 (0: disabled; 1: enabled)
INT2_ IG2_XL	Accelerometer Interrupt 2 generator on INT2 pin. Default value: 0 (0: disabled; 1: enabled)
INT2_ FSS5	FSS5 Interrupt Enable on INT2 pin. Default value: 0 (0: disabled; 1: enabled)
INT2_OVR	Overrun Interrupt on INT2 pin. Default value: 0 (0: disabled; 1: enabled)
INT2_FTH	FIFO threshold interrupt on INT2 pin. Default value: 0 (0: disabled; 1: enabled)
INT2_DRDY_TEMP	Temperature sensor data ready on INT2 pin. Default value: 0 (0: disabled; 1: enabled)
INT2_DRDY_G	Gyroscope data ready on INT2 pin. Default value: 0 (0: disabled; 1: enabled)
INT2_DRDY_XL	Accelerometer data ready on INT2 pin. Default value: 0 (0: disabled; 1: enabled)

12.14 WHO_AM_I (0Fh)

Who_AM_I register.

Table 52. WHO_AM_I register

0	1	1	0	1	0	0	0

12.15 CTRL_REG1_G (10h)

Angular rate sensor control register 1.

Table 53. CTRL_REG1_G register

ODR_G2	ODR_G1	ODR_G0	FS_G1	FS_G0	0(1)	BW_G1	BW_G0

1. This bit must be set to ‘0’ for the correct operation of the device

Table 54. CTRL_REG1_G register description

ODR_G [2:0]	Gyroscope output data rate selection. Default value: 000 (Refer to *Table 55* and *Table 56*)
FS_G [1:0]	Gyroscope full-scale selection. Default value: 00 (00: 245 dps; 01: 500 dps; 10: Not Available; 11: 2000 dps)
BW_G [1:0]	Gyroscope bandwidth selection. Default value: 00

ODR_G [2:0] are used to set ODR selection when both the accelerometer and gyroscope are activated. BW_G [1:0] are used to set the bandwidth selection of the gyroscope bandwidth.

The following table summarizes all frequencies available for each combination of the ODR_G / BW_G bits after LPF1 (see *Table 55*) and LPF2 (see *Table 56*) when both the accelerometer and gyroscope are activated. For more details regarding signal processing please refer to *Figure 18*.

Table 55. ODR and BW configuration setting (after LPF1)

ODR_G2	ODR_G1	ODR_G0	ODR [Hz]	Cutoff [Hz](1)
0	0	0	Power-down	n.a.
0	0	1	14.9	5
0	1	0	59.5	19
0	1	1	119	38
1	0	0	238	76
1	0	1	476	100
1	1	0	952	100
1	1	1	n.a.	n.a.

1. Values in the table are indicative and can vary proportionally with the specific ODR value.

Table 56. ODR and BW configuration setting (after LPF2)

ODR_G [2:0]	BW_G [1:0]	ODR [Hz]	Cutoff [Hz](1)
000	00	Power-down	n.a.
000	01	Power-down	n.a.
000	10	Power-down	n.a.
000	11	Power-down	n.a.
001	00	14.9	n.a.
001	01	14.9	n.a.
001	10	14.9	n.a.
001	11	14.9	n.a.
010	00	59.5	16
010	01	59.5	16
010	10	59.5	16
010	11	59.5	16
011	00	119	14
011	01	119	31
011	10	119	31
011	11	119	31
100	00	238	14
100	01	238	29
100	10	238	63
100	11	238	78
101	00	476	21
101	01	476	28
101	10	476	57
101	11	476	100
110	00	952	33
110	01	952	40
110	10	952	58
110	11	952	100
111	00	n.a.	n.a.
111	01	n.a.	n.a.
111	10	n.a.	n.a.
111	11	n.a.	n.a.

1. Values in the table are indicative and can vary proportionally with the specific ODR value.

12.16 CTRL_REG2_G (11h)

Angular rate sensor control register 2.

Table 57. CTRL_REG2_G register

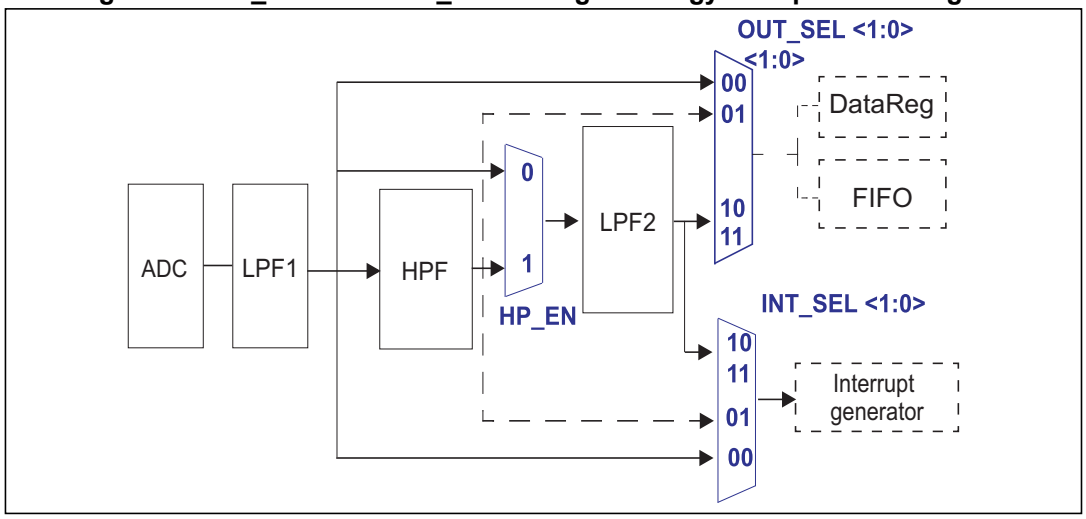
0(1)	0(1)	0(1)	0(1)	INT_SEL1	INT_SEL0	OUT_SEL1	OUT_SEL0

1. These bits must be set to '0' for the correct operation of the device

Table 58. CTRL_REG2_G register description

INT_SEL [1:0]	INT selection configuration. Default value: 00 (Refer to *Figure 18*)
OUT_SEL [1:0]	Out selection configuration. Default value: 00 (Refer to *Figure 18*)

Figure 18. INT_SEL and OUT_SEL configuration gyroscope block diagram



12.17 CTRL_REG3_G (12h)

Angular rate sensor control register 3.

Table 59. CTRL_REG3_G register

LP_mode	HP_EN	0(1)	0(1)	HPCF3_G	HPCF2_G	HPCF1_G	HPCF0_G

1. These bits must be set to '0' for the correct operation of the device

Table 60. CTRL_REG3_G register description

LP_mode	Low-power mode enable. Default value: 0 (0: Low-power disable; 1:Low-power enable)
HP_EN	High-pass filter enable. Default value: 0 (0: HPF disabled; 1: HPF enabled, refer to *Figure 18*)
HPCF_G [3:0]	Gyroscope high-pass filter cutoff frequency selection. Default value: 0000 Refer to *Table 61*.

Table 61. Gyroscope high-pass filter cutoff frequency configuration [Hz](1)

HPCF_G [3:0]	ODR= 14.9 Hz	ODR= 59.5 Hz	ODR= 119 Hz	ODR= 238 Hz	ODR= 476 Hz	ODR= 952 Hz
0000	1	4	8	15	30	57
0001	0.5	2	4	8	15	30
0010	0.2	1	2	4	8	15
0011	0.1	0.5	1	2	4	8
0100	0.05	0.2	0.5	1	2	4
0101	0.02	0.1	0.2	0.5	1	2
0110	0.01	0.05	0.1	0.2	0.5	1
0111	0.005	0.02	0.05	0.1	0.2	0.5
1000	0.002	0.01	0.02	0.05	0.1	0.2
1001	0.001	0.005	0.01	0.02	0.05	0.1

1. Values in the table are indicative and can vary proportionally with the specific ODR value.

12.18 ORIENT_CFG_G (13h)

Angular rate sensor sign and orientation register.

Table 62. ORIENT_CFG_G register

0(1)	0(1)	SignX_G	SignY_G	SignZ_G	Orient_2	Orient_1	Orient_0

1. These bits must be set to ‘0’ for the correct operation of the device

Table 63. ORIENT_CFG_G register description

SignX_G	Pitch axis (X) angular rate sign. Default value: 0 (0: positive sign; 1: negative sign)
SignY_G	Roll axis (Y) angular rate sign. Default value: 0 (0: positive sign; 1: negative sign)
SignZ_G	Yaw axis (Z) angular rate sign. Default value: 0 (0: positive sign; 1: negative sign)
Orient [2:0]	Directional user-orientation selection. Default value: 000

12.19 INT_GEN_SRC_G (14h)

Angular rate sensor interrupt source register.

Table 64. INT_GEN_SRC_G register

0	IA_G	ZH_G	ZL_G	YH_G	YL_G	XH_G	XL_G

Table 65. INT_GEN_SRC_G register description

IA_G	Interrupt active. Default value: 0 (0: no interrupt has been generated; 1: one or more interrupts have been generated)
ZH_G	Yaw (Z) high. Default value: 0 (0: no interrupt, 1: Z high event has occurred)
ZL_G	Yaw (Z) low. Default value: 0 (0: no interrupt; 1: Z low event has occurred)
YH_G	Roll (Y) high. Default value: 0 (0: no interrupt, 1: Y high event has occurred)
YL_G	Roll (Y) low. Default value: 0 (0: no interrupt, 1: Y low event has occurred)
XH_G	Pitch (X) high. Default value: 0 (0: no interrupt, 1: X high event has occurred)
XL_G	Pitch (X) low. Default value: 0 (0: no interrupt, 1: X low event has occurred)

12.20 OUT_TEMP_L (15h), OUT_TEMP_H (16h)

Temperature data output register. L and H registers together express a 16-bit word in two's complement right-justified.

Table 66. OUT_TEMP_L register

Temp7	Temp6	Temp5	Temp4	Temp3	Temp2	Temp1	Temp0

Table 67. OUT_TEMP_H register

Temp11	Temp11	Temp11	Temp11	Temp11	Temp10	Temp9	Temp8

Table 68. OUT_TEMP register description

Temp [11:0]	Temperature sensor output data. The value is expressed as two's complement sign extended on the MSB.

12.21 STATUS_REG (17h)

Status register.

Table 69. STATUS_REG register

0	IG_XL	IG_G	INACT	BOOT_ STATUS	TDA	GDA	XLDA

Table 70. STATUS_REG register description

IG_XL	Accelerometer interrupt output signal. Default value: 0 (0: no interrupt has been generated; 1: one or more interrupt events have been generated)
IG_G	Gyroscope interrupt output signal. Default value: 0 (0: no interrupt has been generated; 1: one or more interrupt events have been generated)
INACT	Inactivity interrupt output signal. Default value: 0 (0: no interrupt has been generated; 1: one or more interrupt events have been generated)
BOOT_ STATUS	Boot running flag signal. Default value: 0 (0: no boot running; 1: boot running)
TDA	Temperature sensor new data available. Default value: 0 (0:a new data is not yet available; 1: new data is available)
GDA	Gyroscope new data available. Default value: 0 (0: a new set of data is not yet available; 1: a new set of data is available)
XLDA	Accelerometer new data available. Default value: 0 (0: a new set of data is not yet available; 1: a new set of data is available)

12.22 OUT_X_G (18h - 19h)

Angular rate sensor pitch axis (X) angular rate output register. The value is expressed as a 16-bit word in two's complement.

12.23 OUT_Y_G (1Ah - 1Bh)

Angular rate sensor roll axis (Y) angular rate output register. The value is expressed as a 16-bit word in two's complement.

12.24 OUT_Z_G (1Ch - 1Dh)

Angular rate sensor yaw axis (Z) angular rate output register. The value is expressed as a 16-bit word in two's complement.

12.25 CTRL_REG4 (1Eh)

Control register 4.

Table 71. CTRL_REG4 register

0(1)	0(1)	Zen_G	Yen_G	Xen_G	0(1)	LIR_XL1	4D_XL1

1. These bits must be set to '0' for the correct operation of the device

Table 72. CTRL_REG4 register description

Zen_G	Gyroscope's yaw axis (Z) output enable. Default value: 1 (0: Z-axis output disabled; 1: Z-axis output enabled)
Yen_G	Gyroscope's roll axis (Y) output enable. Default value: 1 (0: Y-axis output disabled; 1: Y axis output enabled)
Xen_G	Gyroscope's pitch axis (X) output enable. Default value: 1 (0: X-axis output disabled; 1: X-axis output enabled)
LIR_XL1	Latched interrupt. Default value: 0 (0: interrupt request not latched; 1: interrupt request latched)
4D_XL1	4D option enabled on interrupt. Default value: 0 (0: interrupt generator uses 6D for position recognition; 1: interrupt generator uses 4D for position recognition)

12.26 CTRL_REG5_XL (1Fh)

Linear acceleration sensor control register 5.

Table 73. CTRL_REG5_XL register

DEC_1	DEC_0	Zen_XL	Yen_XL	Xen_XL	0(1)	0(1)	0(1)

1. These bits must be set to '0' for the correct operation of the device

Table 74. CTRL_REG5_XL register description

DEC_ [0:1]	Decimation of acceleration data on OUT REG and FIFO. Default value: 00 (00: no decimation; 01: update every 2 samples; 10: update every 4 samples; 11: update every 8 samples)
Zen_XL	Accelerometer's Z-axis output enable. Default value: 1 (0: Z-axis output disabled; 1: Z-axis output enabled)
Yen_XL	Accelerometer's Y-axis output enable. Default value: 1 (0: Y-axis output disabled; 1: Y-axis output enabled)
Xen_XL	Accelerometer's X-axis output enable. Default value: 1 (0: X-axis output disabled; 1: X-axis output enabled)

12.27 CTRL_REG6_XL (20h)

Linear acceleration sensor control register 6.

Table 75. CTRL_REG6_XL register

ODR_XL2	ODR_XL1	ODR_XL0	FS1_XL	FS0_XL	BW_SCAL_ODR	BW_XL1	BW_XL0

Table 76. CTRL_REG6_XL register description

ODR_XL [2:0]	Output data rate and power mode selection. Default value: 000 (see *Table 77*).
FS_XL [1:0]	Accelerometer full-scale selection. Default value: 00. (00: ±2g; 01: Not Available; 10: ±4g; 11: ±8g)
BW_SCAL_ ODR	Bandwidth selection. Default value: 0. (0: bandwidth determined by ODR selection: - BW = 408 Hz when ODR = 952 Hz, 50 Hz, 10 Hz; - BW = 211 Hz when ODR = 476 Hz; - BW = 105 Hz when ODR = 238 Hz; - BW = 50 Hz when ODR = 119 Hz; 1: bandwidth selected according to BW_XL [2:1] selection)
BW_XL [1:0]	Anti-aliasing filter bandwidth selection. Default value: 00. (00: 408 Hz; 01: 211 Hz; 10: 105 Hz; 11: 50 Hz)

ODR_XL [2:0] is used to set power mode and ODR selection. *Table 77* indicates all available frequencies when only the accelerometer is activated.

Table 77. ODR register setting (accelerometer only mode)

ODR_XL2	ODR_XL1	ODR_XL0	ODR selection [Hz]
0	0	0	Power-down
0	0	1	10 Hz
0	1	0	50 Hz
0	1	1	119 Hz
1	0	0	238 Hz
1	0	1	476 Hz
1	1	0	952 Hz
1	1	1	n.a.

12.28 CTRL_REG7_XL (21h)

Linear acceleration sensor control register 7.

Table 78. CTRL_REG7_XL register

HR	DCF1	DCF0	0(1)	0(1)	FDS	0(1)	HPIS1

1. These bits must be set to ‘0’ for the correct operation of the device

Table 79. CTRL_REG7_XL register description

HR	High resolution mode for accelerometer enable. Default value: 0 (0: disabled; 1: enabled). Refer to *Table 80*.
DCF[1:0]	Accelerometer digital filter (high-pass and low-pass) cutoff frequency selection: the bandwidth of the high-pass filter depends on the selected ODR. Refer to *Table 80*.
FDS	Filtered data selection. Default value: 0. (0: internal filter bypassed; 1: data from internal filter sent to output register and FIFO)
HPIS1	High Pass filter enabled for acceleration sensor interrupt function on Interrupt. Default value: 0. (0: filter bypassed; 1: filter enabled)

Table 80. Low-pass cutoff frequency in high resolution mode (HR = 1)

HR	CTRL_REG7 (DCF [1:0])	LP cutoff Freq. [Hz]
1	00	ODR/50
1	01	ODR/100
1	10	ODR/9
1	11	ODR/400

12.29 CTRL_REG8 (22h)

Control register 8.

Table 81. CTRL_REG8 register

BOOT	BDU	H_LACTIVE	0(1)	SIM	IF_ADD_INC	BLE	SW_RESET

1. This bit must be set to ‘0’ for the correct operation of the device.

Table 82. CTRL_REG8 register description

BOOT	Reboot memory content. Default value: 0 (0: normal mode; 1: reboot memory content(1))
BDU	Block Data Update. Default value: 0 (0: continuous update; 1: output registers not updated until MSB and LSB read)
H_LACTIVE	Interrupt activation level. Default value: 0 (0: interrupt output pins active high; 1: interrupt output pins active low)
SIM	SPI serial interface mode selection. Default value: 0 (0: 4-wire interface; 1: 3-wire interface)
IF_ADD_INC	Register address automatically incremented during a multiple byte access with a serial interface (I^2C or SPI). Default value: 1 (0: disabled; 1: enabled)
BLE	Big/Little Endian data selection. Default value 0. (0: data LSB @ lower address; 1: data MSB @ lower address)
SW_RESET	Software Reset. Default value: 0 (0: normal mode; 1: reset device) This bit is cleared by hardware after next flash boot.

1. Boot request is executed as soon as the internal oscillator is turned-on. It is possible to set the bit while in power-down mode, in this case it will be served at the next normal mode or sleep mode.

12.30 CTRL_REG9 (23h)

Control register 9.

Table 83. CTRL_REG9 register

0(1)	SLEEP_G	0(1)	FIFO_ TEMP_EN	DRDY_ mask_bit	I2C_disable	FIFO_EN	STOP_ON _FTH

1. These bits must be set to '0' for the correct operation of the device

Table 84. CTRL_REG9 register description

SLEEP_G	Gyroscope sleep mode enable. Default value: 0 (0: disabled; 1: enabled)
FIFO_TEMP_EN	Temperature data storage in FIFO enable. Default value: 0 (0: temperature data not stored in FIFO; 1: temperature data stored in FIFO)
DRDY_mask_bit	Data available enable bit. Default value: 0 (0: DA timer disabled; 1: DA timer enabled)
I2C_disable	Disable I^2C interface. Default value: 0 (0: both I^2C and SPI enabled; 1: I^2C disabled, SPI only)
FIFO_EN	FIFO memory enable. Default value: 0 (0: disabled; 1: enabled)
STOP_ON_FTH	Enable FIFO threshold level use. Default value: 0 (0: FIFO depth is not limited; 1: FIFO depth is limited to threshold level)

12.31 CTRL_REG10 (24h)

Control register 10.

Table 85. CTRL_REG10 register

0(1)	0(1)	0(1)	0(1)	0(1)	ST_G	0(1)	ST_XL

1. These bits must be set to '0' for the correct operation of the device

Table 86. CTRL_REG10 register description

ST_G	Angular rate sensor self-test enable. Default value: 0 (0: Self-test disabled; 1: Self-test enabled;)
ST_XL	Linear acceleration sensor self-test enable. Default value: 0 (0: Self-test disabled; 1: Self-test enabled;)

12.32 INT2_GEN_SRC_XL (25h)

Linear acceleration sensor interrupt 2 source register.

Table 87. INT2_GEN_SRC_XL register

0	IA2_XL	ZH2_XL	ZL2_XL	YH2_XL	YL2_XL	XH2_XL	XL2_XL

Table 88. INT2_GEN_SRC_XL register description

IA2_XL	Interrupt active. Default value: 0 (0: no interrupt has been generated; 1: one or more interrupts have been generated)
ZH2_XL	Accelerometer's Z high event. Default value: 0 (0: no interrupt, 1: Z high event has occurred)
ZL2_XL	Accelerometer's Z low event. Default value: 0 (0: no interrupt; 1: Z low event has occurred)
YH2_XL	Accelerometer's Y high event. Default value: 0 (0: no interrupt, 1: Y high event has occurred)
YL2_XL	Accelerometer's Y low event. Default value: 0 (0: no interrupt, 1: Y low event has occurred)
XH2_XL	Accelerometer's X high event. Default value: 0 (0: no interrupt, 1: X high event has occurred)
XL2_XL	Accelerometer's X low event. Default value: 0 (0: no interrupt, 1: X low event has occurred)

12.33 INT1_GEN_SRC_XL (26h)

Linear acceleration sensor interrupt 1 source register.

Table 89. INT1_GEN_SRC_XL register

0	IA1_XL	ZH1_XL	ZL1_XL	YH1_XL	YL1_XL	XH1_XL	XL1_XL

Table 90. INT1_GEN_SRC_XL register description

IA1_XL	Interrupt active. Default value: 0 (0: no interrupt has been generated; 1: one or more interrupts have been generated)
ZH1_XL	Accelerometer's Z high event. Default value: 0 (0: no interrupt, 1: Z high event has occurred)
ZL1_XL	Accelerometer's Z low event. Default value: 0 (0: no interrupt; 1: Z low event has occurred)
YH1_XL	Accelerometer's Y high event. Default value: 0 (0: no interrupt, 1: Y high event has occurred)
YL1_XL	Accelerometer's Y low event. Default value: 0 (0: no interrupt, 1: Y low event has occurred)
XH1_XL	Accelerometer's X high event. Default value: 0 (0: no interrupt, 1: X high event has occurred)
XL1_XL	Accelerometer's X low event. Default value: 0 (0: no interrupt, 1: X low event has occurred)

12.34 STATUS_REG (27h)

Status register.

Table 91. STATUS_REG register

0	IG_XL	IG_G	INACT	BOOT_ STATUS	TDA	GDA	XLDA

Table 92. STATUS_REG register description

IG_XL	Accelerometer interrupt output signal. Default value: 0 (0: no interrupt has been generated; 1: one or more interrupt events have been generated)
IG_G	Gyroscope interrupt output signal. Default value: 0 (0: no interrupt has been generated; 1: one or more interrupt events have been generated)
INACT	Inactivity interrupt output signal. Default value: 0 (0: no interrupt has been generated; 1: one or more interrupt events have been generated)
BOOT_ STATUS	Boot running flag signal. Default value: 0 (0: no boot running; 1: boot running)
TDA	Temperature sensor new data available. Default value: 0 (0: a new data is not yet available; 1: a new data is available)
GDA	Gyroscope new data available. Default value: 0 (0: a new set of data is not yet available; 1: a new set of data is available)
XLDA	Accelerometer new data available. Default value: 0 (0: a new set of data is not yet available; 1: a new set of data is available)

12.35 OUT_X_XL (28h - 29h)

Linear acceleration sensor X-axis output register. The value is expressed as a 16-bit word in two’s complement.

12.36 OUT_Y_XL (2Ah - 2Bh)

Linear acceleration sensor Y-axis output register. The value is expressed as a 16-bit word in two’s complement.

12.37 OUT_Z_XL (2Ch - 2Dh)

Linear acceleration sensor Z-axis output register. The value is expressed as a 16-bit word in two’s complement.

12.38 FIFO_CTRL (2Eh)

FIFO control register.

Table 93. FIFO_CTRL register

FMODE2	FMODE1	FMODE0	FTH4	FTH3	FTH2	FTH1	FTH0

Table 94. FIFO_CTRL register description

FMODE [2:0]	FIFO mode selection bits. Default value: 000 For further details refer to *Table 95*.
FTH [4:0]	FIFO threshold level setting. Default value: 0 0000

Table 95. FIFO mode selection

FMODE2	FMODE1	FMODE0	Mode
0	0	0	Bypass mode. FIFO turned off
0	0	1	FIFO mode. Stop collecting data when FIFO is full.
0	1	0	Reserved
0	1	1	Continuous mode until trigger is deasserted, then FIFO mode.
1	0	0	Bypass mode until trigger is deasserted, then Continuous mode.
1	1	0	Continuous mode. If the FIFO is full, the new sample over-writes the older one.

12.39 FIFO_SRC (2Fh)

FIFO status control register.

Table 96. FIFO_SRC register

FTH	OVRN	FSS5	FSS4	FSS3	FSS2	FSS1	FSS0

Table 97. FIFO_SRC register description

FTH	FIFO threshold status. (0: FIFO filling is lower than threshold level; 1: FIFO filling is equal or higher than threshold level
OVRN	FIFO overrun status. (0: FIFO is not completely filled; 1: FIFO is completely filled and at least one sample has been overwritten) For further details refer to *Table 98*.
FSS [5:0]	Number of unread samples stored into FIFO. (000000: FIFO empty; 100000: FIFO full, 32 unread samples) For further details refer to *Table 98*.

Table 98. FIFO_SRC example: OVR/FSS details

FTH	OVRN	FSS5	FSS4	FSS3	FSS2	FSS1	FSS0	Description
0	0	0	0	0	0	0	0	FIFO empty
--(1)	0	0	0	0	0	0	1	1 unread sample
...								
--(1)	0	1	0	0	0	0	0	32 unread samples
1	1	1	0	0	0	0	0	At least one sample has been overwritten

1. When the number of unread samples in FIFO is greater than the threshold level set in register *FIFO_CTRL (2Eh)*, FTH value is '1'.

12.40 INT_GEN_CFG_G (30h)

Angular rate sensor interrupt generator configuration register.

Table 99. INT_GEN_CFG_G register

AOI_G	LIR_G	ZHIE_G	ZLIE_G	YHIE_G	YLIE_G	XHIE_G	XLIE_G

Table 100. INT_GEN_CFG_G register description

AOI_G	AND/OR combination of gyroscope's interrupt events. Default value: 0 (0: OR combination; 1: AND combination)
LIR_G	Latch gyroscope interrupt request. Default value: 0 (0: interrupt request not latched; 1: interrupt request latched)
ZHIE_G	Enable interrupt generation on gyroscope's yaw (Z) axis high event. Default value: 0 (0: disable interrupt request; 1: interrupt request on measured angular rate value higher than preset threshold)
ZLIE_G	Enable interrupt generation on gyroscope's yaw (Z) axis low event. Default value: 0 (0: disable interrupt request; 1: interrupt request on measured angular rate value lower than preset threshold)
YHIE_G	Enable interrupt generation on gyroscope's roll (Y) axis high event. Default value: 0 (0: disable interrupt request; 1: interrupt request on measured angular rate value higher than preset threshold)
YLIE_G	Enable interrupt generation on gyroscope's roll (y) axis low event. Default value: 0 (0: disable interrupt request; 1: interrupt request on measured angular rate value lower than preset threshold)
XHIE_G	Enable interrupt generation on gyroscope's pitch (X) axis high event. Default value: 0 (0: disable interrupt request; 1: interrupt request on measured angular rate value higher than preset threshold)
XLIE_G	Enable interrupt generation on gyroscope's pitch (X) axis low event. Default value: 0 (0: disable interrupt request; 1: interrupt request on measured angular rate value lower than preset threshold)

12.41 INT_GEN_THS_X_G (31h - 32h)

Angular rate sensor interrupt generator threshold registers. The value is expressed as a 15-bit word in two's complement.

Table 101. INT_GEN_THS_XH_G register

DCRM_G	THS_G_ X14	THS_G_ X13	THS_G_ X12	THS_G_ X11	THS_G_ X10	THS_G_ X9	THS_G_ X8

Table 102. INT_GEN_THS_XL_G register

THS_G_ X7	THS_G_ X6	THS_G_ X5	THS_G_ X4	THS_G_ X3	THS_G_ X2	THS_G_ X1	THS_G_ X0

Table 103. INT_GEN_THS_X_G register description

DCRM_G	Decrement or reset counter mode selection. Default value: 0 (0: Reset; 1: Decrement, as per counter behavior in *Figure 19* and *Figure 20*)
THS_G_X [14:0]	Angular rate sensor interrupt threshold on pitch (X) axis. Default value: 0000000 00000000.

12.42 INT_GEN_THS_Y_G (33h - 34h)

Angular rate sensor interrupt generator threshold registers. The value is expressed as a 15-bit word in two's complement.

Table 104. INT_GEN_THS_YH_G register

0(1)	THS_G_ Y14	THS_G_ Y13	THS_G_ Y12	THS_G_ Y11	THS_G_ Y10	THS_G_ Y9	THS_G_ Y8

1. This bit must be set to '0' for the correct operation of the device

Table 105. INT_GEN_THS_YL_G register

THS_G_ Y7	THS_G_ Y6	THS_G_ Y5	THS_G_ Y4	THS_G_ Y3	THS_G_ Y2	THS_G_ Y1	THS_G_ Y0

Table 106. INT_GEN_THS_Y_G register description

THS_G_Y [14:0]	Angular rate sensor interrupt threshold on roll (Y) axis. Default value: 0000000 00000000.

12.43 INT_GEN_THS_Z_G (35h - 36h)

Angular rate sensor interrupt generator threshold registers. The value is expressed as a 15-bit word in two's complement.

Table 107. INT_GEN_THS_ZH_G register

0(1)	THS_G_ Z14	THS_G_ Z13	THS_G_ Z12	THS_G_ Z11	THS_G_ Z10	THS_G_ Z9	THS_G_ Z8

1. This bit must be set to '0' for the correct operation of the device

Table 108. INT_GEN_THS_ZL_G register

THS_G_ Z7	THS_G_ Z6	THS_G_ Z5	THS_G_ Z4	THS_G_ Z3	THS_G_ Z2	THS_G_ Z1	THS_G_ Z0

Table 109. INT_GEN_THS_Z_G register description

THS_G_Z [14:0]	Angular rate sensor interrupt thresholds on yaw (Z) axis. Default value: 0000000 00000000.

12.44 INT_GEN_DUR_G (37h)

Angular rate sensor interrupt generator duration register.

Table 110. INT_GEN_DUR_G register

WAIT_G	DUR_G6	DUR_G5	DUR_G4	DUR_G3	DUR_G2	DUR_G1	DUR_G0

Table 111. INT_GEN_DUR_G register description

WAIT_G	Exit from interrupt wait function enable. Default value: 0 (0: wait function off; 1: wait for DUR_G [6:0] samples before exiting interrupt)
DUR_G [6:0]	Enter/exit interrupt duration value. Default value: 000 0000

The **DUR_G [6:0]** bits set the minimum duration of the interrupt event to be recognized. Duration steps and maximum values depend on the ODR chosen.

The **WAIT_G** bit has the following meaning:

'0': the interrupt falls immediately if the signal crosses the selected threshold

'1': if the signal crosses the selected threshold, the interrupt falls after a number of samples equal to the value of the duration counter register.

For further details refer to *Figure 19* and *Figure 20*.

Figure 19. Wait bit disabled

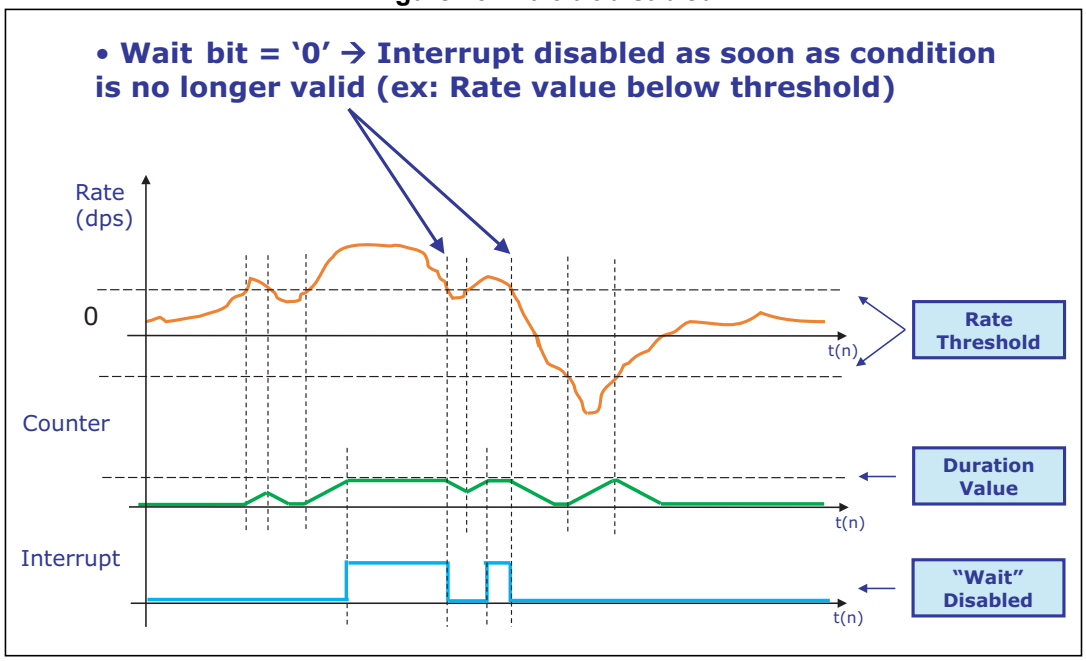
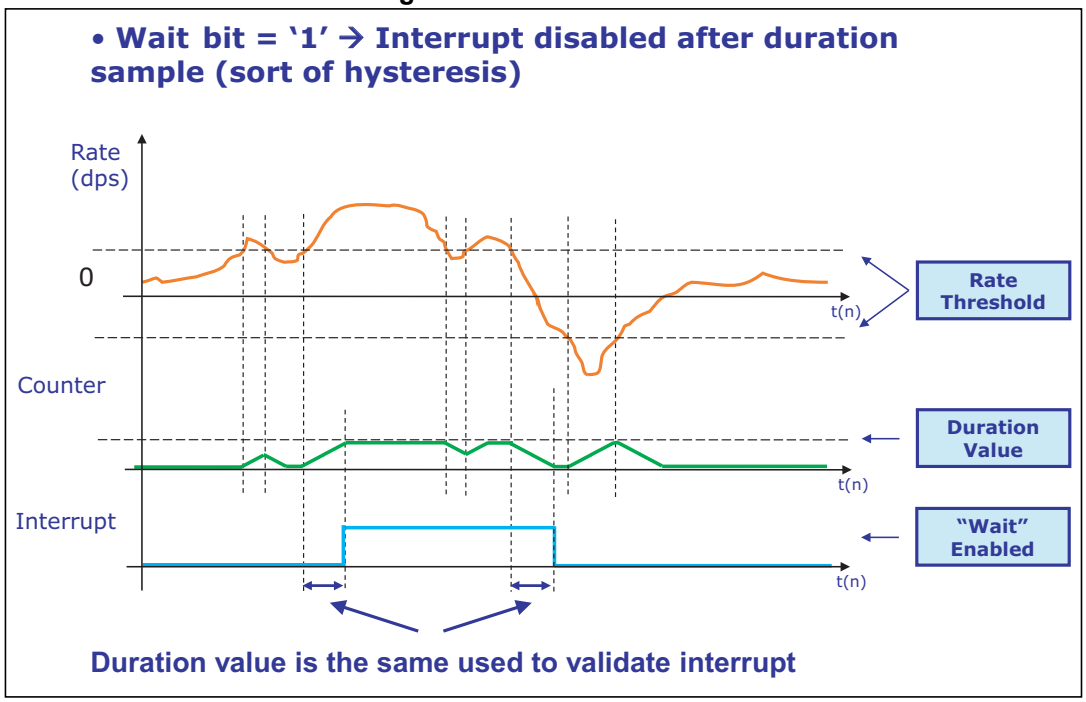


Figure 20. Wait bit enabled



13 Soldering information

The LGA package is compliant with the ECOPACK®, RoHS and “Green” standard.
It is qualified for soldering heat resistance according to JEDEC J-STD-020.

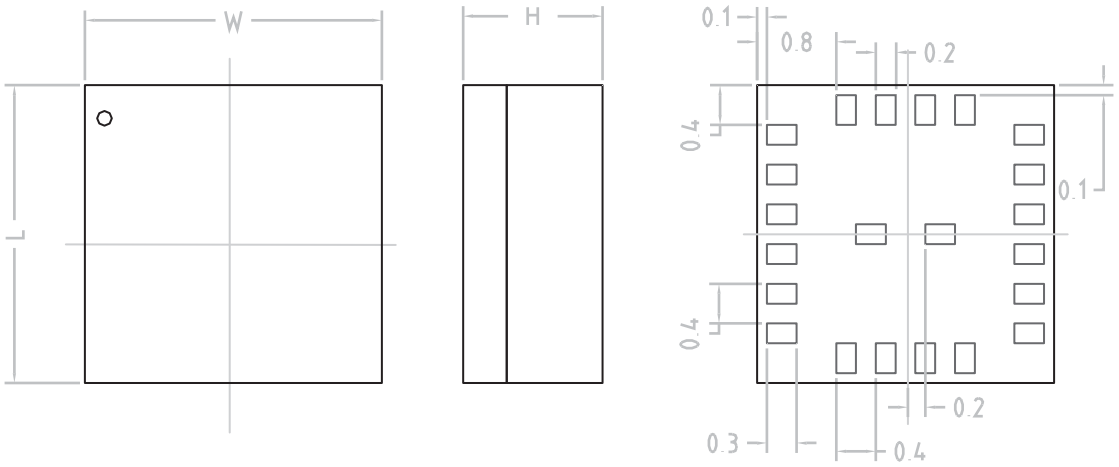
Leave “Pin 1 Indicator” unconnected during soldering.

Land pattern and soldering recommendations are available at www.st.com/mems.

14 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

Figure 21. LGA-22: mechanical data and package dimensions



Dimensions are in millimeter unless otherwise specified
General Tolerance is +/-0.1mm unless otherwise specified

OUTER DIMENSIONS

ITEM	DIMENSION [mm]	TOLERANCE [mm]
Length [L]	3.00	±0.1
Width [W]	3.00	±0.1
Height [H]	1.03	MAX

8514415_A

15 Revision history

Table 112. Document revision history

Date	Revision	Changes
28-Nov-2013	1	Initial release
25-Feb-2014	2	Updated *Figure 1*, *Figure 2*, *Figure 4*, *Table 2*, *Section 9.13: JTAG and SW debug support*, *Section 12.33: INT1_GEN_SRC_XL (26h)* and *Table 25: Motion sensor registers* Added *Section 2: LSM6DB0 application hints*, *Section 8.3: Digital interface* and *Section 12.32: INT2_GEN_SRC_XL (25h)*

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