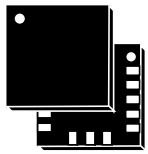
LSM6DS1

iNEMO inertial module: 3D accelerometer and 3D gyroscope

Datasheet - preliminary data



LGA-16L (3x3x0.86 mm)

Features

- Analog supply voltage: 1.71 V to 3.6 V
- Independent IOs supply (1.71 V)
- “Always on” eco power mode down to 1.8 mA
- 3 independent acceleration channels and 3 angular rate channels
- ±2/±4/±8 *g* full scale
- ±245/±500/±2000 dps full scale
- SPI/I^2C serial interface
- Embedded temperature sensor
- Embedded FIFO
- Embedded sensor hub
- ECOPACK®, RoHS and “Green” compliant

Applications

- GPS navigation systems
- Impact recognition and logging
- Gaming and virtual reality input devices
- Motion-activated functions
- Intelligent power saving for handheld devices
- Vibration monitoring and compensation
- Free-fall detection
- 6D orientation detection

Description

The LSM6DS1 is a system-in-package featuring a 3D digital accelerometer and a 3D digital gyroscope. ST’s family of MEMS sensor modules leverages the robust and mature manufacturing processes already used for the production of micromachined accelerometers and gyroscopes.

The various sensing elements are manufactured using specialized micromachining processes, while the IC interfaces are developed using CMOS technology that allows the design of a dedicated circuit which is trimmed to better match the sensing element characteristics.

The LSM6DS1 has a full-scale acceleration range of ±2/±4/±8 *g* and an angular rate range of ±245/±500/±2000 dps. The LSM6DS1 has two operating modes in that the accelerometer and gyroscope sensors can be either activated at the same ODR or the accelerometer can be enabled while the gyroscope is in power-down.

The LSM6DS1 is available in a plastic land grid array (LGA) package.

Table 1. Device summary

Part number	Temp. range [°C]	Package	Packing
LSM6DS1	-40 to +85	LGA-16L (3x3x0.86 mm)	Tray
LSM6DS1TR	-40 to +85		Tape and reel

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1 Pin description

Figure 1. Pin connections

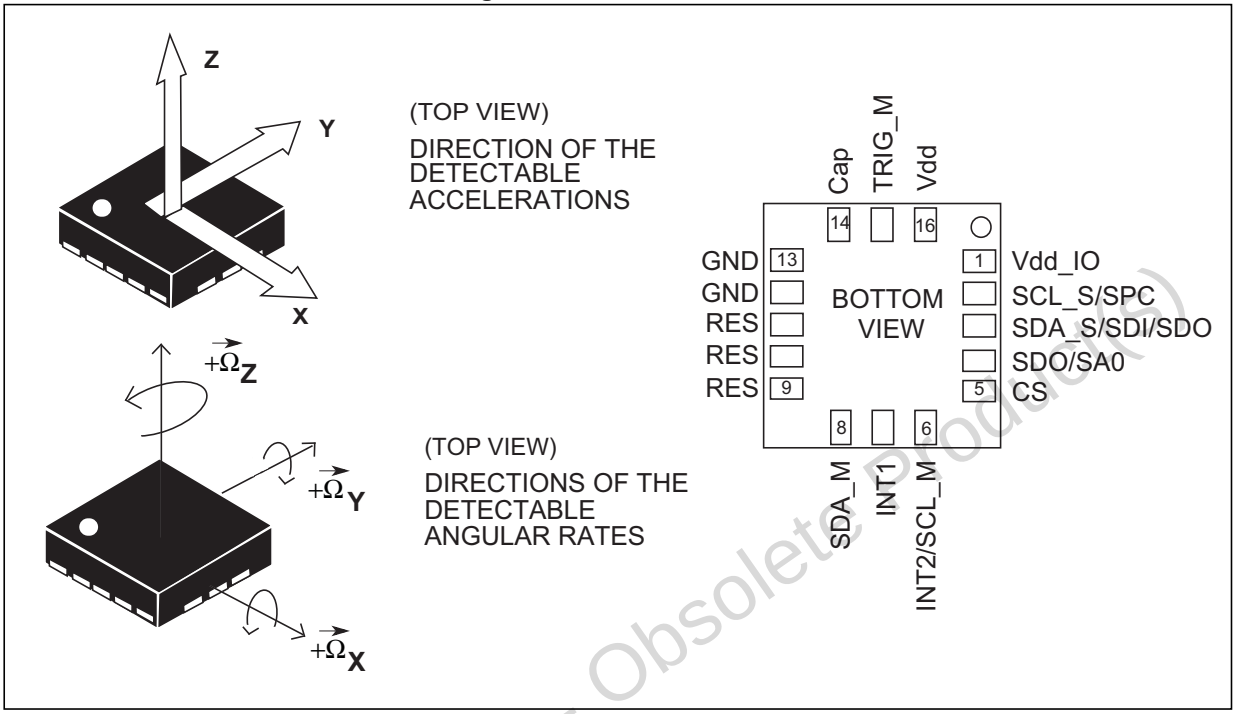


Table 2. Pin description

Pin#	Name	Function
1	Vdd_IO(1)	Power supply for I/O pins
2	SCL_S SPC	Slave I²C serial clock (SCL_S) SPI serial port clock (SPC)
3	SDA_S SDI SDO	Slave I²C serial data (SDA_S) SPI serial data input (SDI) 3-wire interface serial data output (SDO)
4	SDO SA0	SPI serial data output (SDO) I²C least significant bit of the device address (SA0)
5	CS	SPI enable I²C/SPI mode selection (1: SPI idle mode / I²C communication enabled; 0: SPI communication mode / I²C disabled)
6	INT2/SCL_M	Programmable interrupt (INT2)/ Master I²C serial clock (SCL_M)
7	INT1	Programmable interrupt
8	SDA_M	Master I²C serial data (SDA_M)
9	RES	Connect to GND
10	RES	Connect to GND
11	RES	Connect to Vdd or GND
12	GND	0 V supply
13	GND	0 V supply
14	Cap	Connect to GND with ceramic capacitor(2)
15	TRIG_M	External synchronization signal for master I²C
16	Vdd(3)	Power supply

1. Recommended 100 nF filter capacitor.
2. 10 nF (±10%), 16 V. 1 nF minimum value has to be guaranteed under 11 V bias condition.
3. Recommended 100 nF plus 10 µF capacitors.

2 Module specifications

2.1 Mechanical characteristics

@ Vdd = 2.2 V, T = 25 °C unless otherwise noted [a]

Table 3. Mechanical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.[1]	Max.	Unit
LA_FS	Linear acceleration measurement range			±2		*g*
				±4		
				±8		
G_FS	Angular rate measurement range			±245		dps
				±500		
				±2000		
LA_So	Linear acceleration sensitivity	FS = ±2 g		0.061		mg/LSb
		FS = ±4 g		0.122		
		FS = ±8 g		0.244		
G_So	Angular rate sensitivity	FS = ±245 dps		8.75		mdps/LSb
		FS = ±500 dps		17.50		
		FS = ±2000 dps		70		
LA_TyOff	Linear acceleration typical zero-*g* level offset accuracy[2]	FS = ±8 g		±90		m*g*
G_TyOff	Angular rate typical zero-rate level[3]	FS = ±2000 dps		±30		dps
LA_ODR	Linear acceleration output data rate	Gyro ON		952 476 238 119 59.5 14.9		Hz
		Gyro OFF		952 476 238 119 50 10		Hz

a. The product is factory calibrated at 2.2 V. The operational power supply range is from 1.71 V to 3.6 V.

Table 3. Mechanical characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.(1)	Max.	Unit
G_ODR	Angular digital output data rate			952 476 238 119 59.5 14.9		Hz
Top	Operating temperature range		-40		+85	°C

1. Typical specifications are not guaranteed.
2. Typical zero-g level offset value after soldering.
3. Typical zero-rate level offset value after MSL3 preconditioning.

2.2 Electrical characteristics

@ Vdd = 2.2 V, T = 25 °C unless otherwise noted

Table 4. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.(1)	Max.	Unit
Vdd	Supply voltage		1.71		3.6	V
Vdd_IO	Power supply for I/O		1.71		Vdd + 0.1	V
LA_Idd	Accelerometer current consumption in normal mode	ODR = 10 Hz		60		µA
		ODR = 50 Hz		160		
		ODR ≥ 119Hz		330		
G_Idd	Gyroscope current consumption in low-power mode			1.8		mA
Top	Operating temperature range		-40		+85	°C
Trise	Time for power supply rising(2)		0.01		100	ms
Twait	Time delay between Vdd_IO and Vdd(2)		0		10	ms

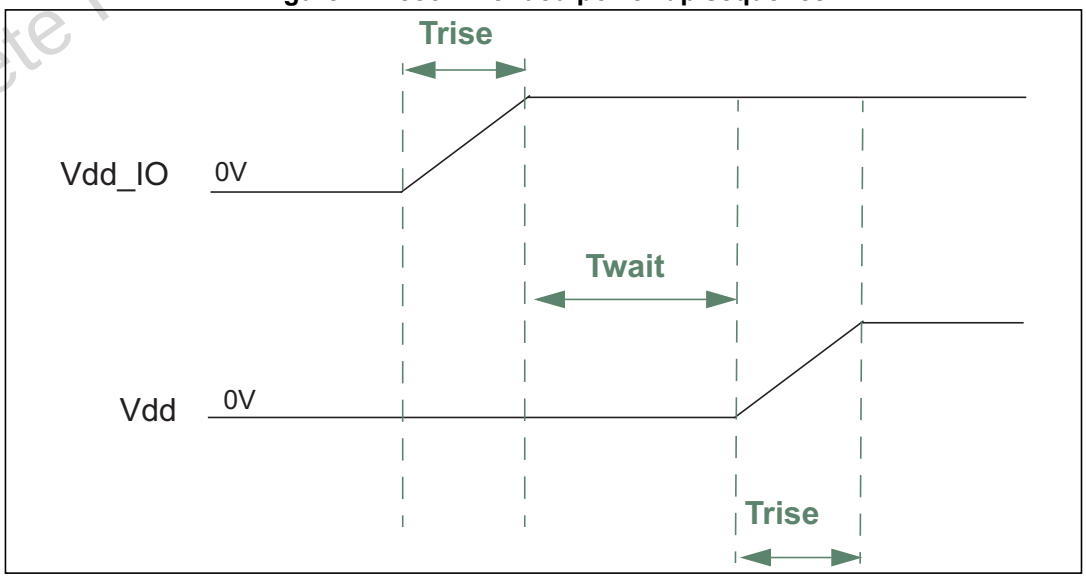
1. Typical specifications are not guaranteed.
2. Please refer to *Section 2.2.1: Recommended power-up sequence* for more details.

2.2.1 Recommended power-up sequence

For the power-up sequence please refer to the following figure, where:

- Trise is the time for the power supply to rise from 10% to 90% of its final value
- Twait is the time delay between the end of the Vdd_IO ramp (90% of its final value) and the start of the Vdd ramp

Figure 2. Recommended power-up sequence



2.3 Temperature sensor characteristics

@ Vdd = 2.2 V, T = 25 °C unless otherwise noted [b]

Table 5. Temperature sensor characteristics

Symbol	Parameter	Test condition	Min.	Typ.(1)	Max.	Unit
TODR	Temperature refresh rate	Gyro off(2)		50		Hz
		Gyro on		59.5		
TSen	Temperature Sensitivity(3)			16		LSB/°C
Top	Operating temperature range		-40		+85	°C

1. Typical specifications are not guaranteed.
2. When the accelerometer ODR is set to 10Hz and the gyroscope part is turned off, the TODR value is 10 Hz.
3. The output of the temperature sensor is 0 (typ.) at 25 °C

b. The product is factory calibrated at 2.2 V.

2.4 Communication interface characteristics

2.4.1 SPI - serial peripheral interface

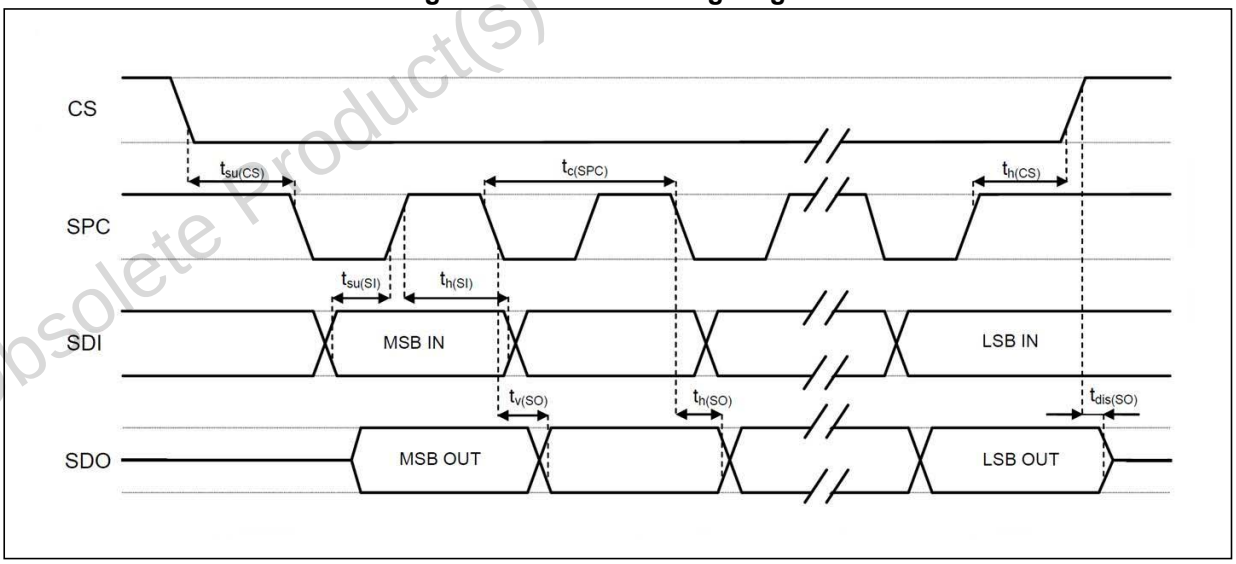
Subject to general operating conditions for Vdd and Top.

Table 6. SPI slave timing values

Symbol	Parameter	Value(1)		Unit
		Min	Max	
$t_{c(SPC)}$	SPI clock cycle	100		ns
$f_{c(SPC)}$	SPI clock frequency		10	MHz
$t_{su(CS)}$	CS setup time	5		ns
$t_{h(CS)}$	CS hold time	20		
$t_{su(SI)}$	SDI input setup time	5		
$t_{h(SI)}$	SDI input hold time	15		
$t_{v(SO)}$	SDO valid output time		50	
$t_{h(SO)}$	SDO output hold time	5		
$t_{dis(SO)}$	SDO output disable time		50	

1. Values are guaranteed at 10 MHz clock frequency for SPI with both 4 and 3 wires, based on characterization results, not tested in production

Figure 3. SPI slave timing diagram



Note: Measurement points are done at 0.2·Vdd_IO and 0.8·Vdd_IO, for both input and output ports.

2.4.2 I²C - inter-IC control interface

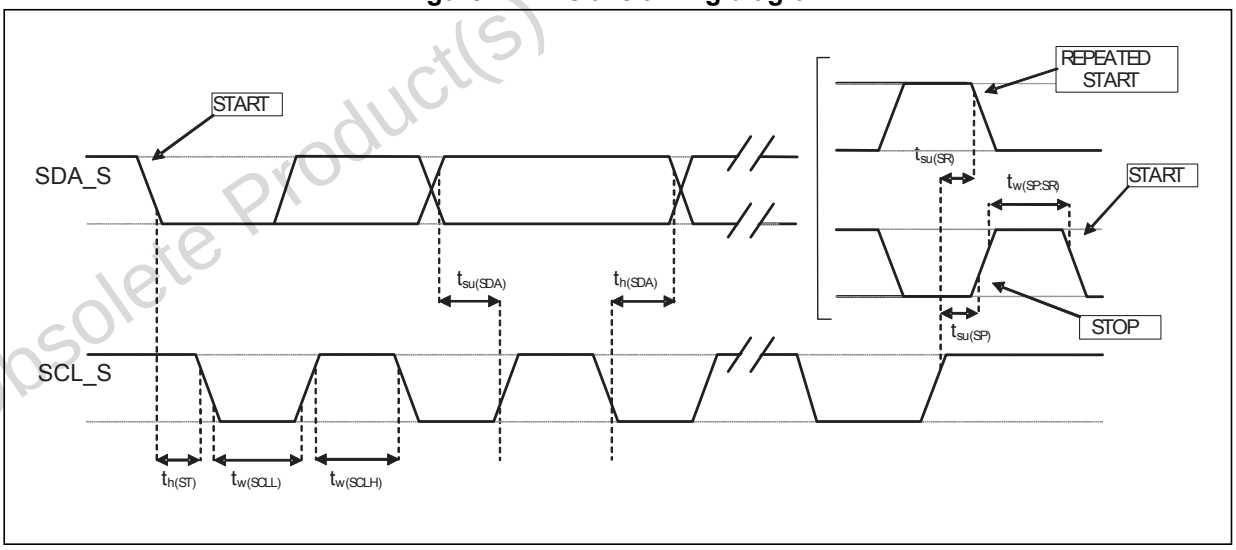
Subject to general operating conditions for Vdd and Top.

Table 7. I²C slave timing values

Symbol	Parameter	I²C standard mode(1)		I²C fast mode (1)		Unit
		Min	Max	Min	Max	
$f_{(SCL)}$	SCL clock frequency	0	100	0	400	kHz
$t_{w(SCLL)}$	SCL clock low time	4.7		1.3		µs
$t_{w(SCLH)}$	SCL clock high time	4.0		0.6		
$t_{su(SDA)}$	SDA setup time	250		100		ns
$t_{h(SDA)}$	SDA data hold time	0	3.45	0	0.9	µs
$t_{h(ST)}$	START condition hold time	4		0.6		µs
$t_{su(SR)}$	Repeated START condition setup time	4.7		0.6		
$t_{su(SP)}$	STOP condition setup time	4		0.6		
$t_{w(SP:SR)}$	Bus free time between STOP and START condition	4.7		1.3		

1. Data based on standard I²C protocol requirement, not tested in production.

Figure 4. I²C slave timing diagram



Note: Measurement points are done at 0.2·Vdd_IO and 0.8·Vdd_IO, for both ports.

2.5 Absolute maximum ratings

Stresses above those listed as “Absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 8. Absolute maximum ratings

Symbol	Ratings	Maximum value	Unit
Vdd	Supply voltage	-0.3 to 4.8	V
T_{STG}	Storage temperature range	-40 to +125	°C
Sg	Acceleration *g* for 0.1 ms	10,000	*g*
ESD	Electrostatic discharge protection (HBM)	2	kV
Vin	Input voltage on any control pin (including CS, SCL/SPC, SDA/SDI/SDO, SDO/SA0)	0.3 to Vdd_IO +0.3	V

Note: Supply voltage on any pin should never exceed 4.8 V.

This device is sensitive to mechanical shock, improper handling can cause permanent damage to the part.

This device is sensitive to electrostatic discharge (ESD), improper handling can cause permanent damage to the part.

2.6 Terminology

2.6.1 Sensitivity

Linear acceleration sensitivity can be determined for example by applying 1 *g* acceleration to the device. Because the sensor can measure DC accelerations, this can be done easily by pointing the selected axis towards the ground, noting the output value, rotating the sensor 180 degrees (pointing towards the sky) and noting the output value again. By doing so, ±1 *g* acceleration is applied to the sensor. Subtracting the larger output value from the smaller one, and dividing the result by 2, leads to the actual sensitivity of the sensor. This value changes very little over temperature and over time. The sensitivity tolerance describes the range of sensitivities of a large number of sensors.

An angular rate gyroscope is device that produces a positive-going digital output for counterclockwise rotation around the axis considered. Sensitivity describes the gain of the sensor and can be determined by applying a defined angular velocity to it. This value changes very little over temperature and time.

2.6.2 Zero-*g* and zero rate level

Linear acceleration zero-*g* level offset (TyOff) describes the deviation of an actual output signal from the ideal output signal if no acceleration is present. A sensor in a steady state on a horizontal surface will measure 0 *g* on both the X-axis and Y-axis, whereas the Z-axis will measure 1 *g*. Ideally, the output is in the middle of the dynamic range of the sensor (content of OUT registers 00h, data expressed as two's complement number). A deviation from the ideal value in this case is called zero-*g* offset.

Offset is to some extent a result of stress to the MEMS sensor and therefore the offset can slightly change after mounting the sensor onto a printed circuit board or exposing it to extensive mechanical stress. Offset changes little over temperature, see "Linear acceleration zero-*g* level change vs. temperature" in *Table 3*. The zero-*g* level tolerance (TyOff) describes the standard deviation of the range of zero-*g* levels of a group of sensors.

The zero-rate level describes the actual output signal if there is no angular rate present. The zero-rate level of precise MEMS sensors is, to some extent, a result of stress to the sensor and therefore zero-rate level can slightly change after mounting the sensor onto a printed circuit board or after exposing it to extensive mechanical stress. This value changes very little over temperature and time.

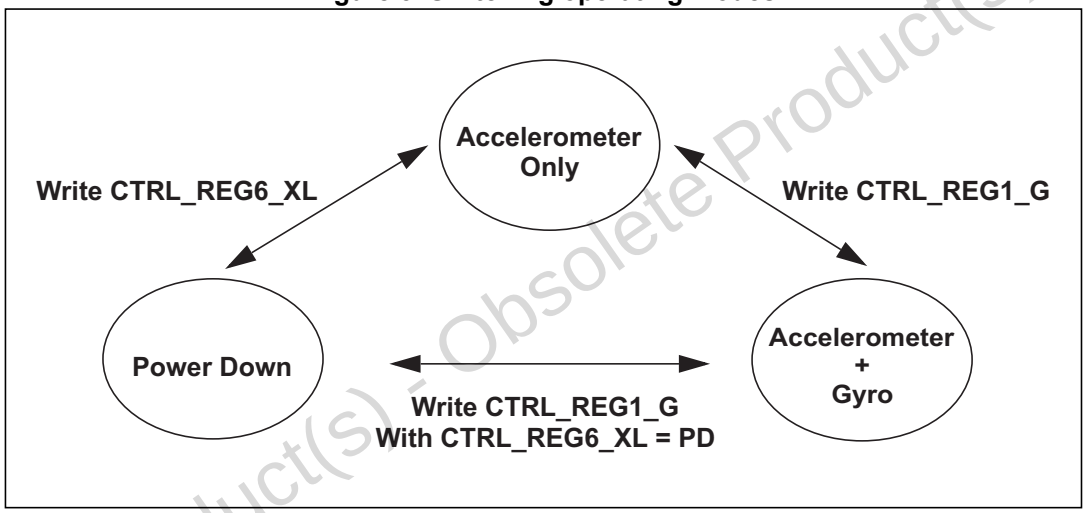
3 Functionality

3.1 Operating modes

The LSM6DS1 has two operating modes available: only accelerometer active and gyroscope in power-down or both accelerometer and gyroscope sensors active at the same ODR. Switching from one mode to the other requires one write operation: writing to *CTRL_REG6_XL (20h)*, the accelerometer operates in normal mode and the gyroscope is powered down, writing to *CTRL_REG1_G (10h)* both the accelerometer and gyroscope are activated at the same ODR.

Figure 5 depicts both modes of operation from power down.

Figure 5. Switching operating modes



3.2 Gyroscope power modes

In LSM6DS1, the gyroscope can be configured in three different operating modes: power-down, low-power and normal mode.

Low-power mode is available for lower ODR (14.9, 59.5, 119 Hz) while for greater ODR (238, 476, 952 Hz) the device is automatically in normal mode. In *Table 9* summarizes the ODR configuration (ODR_G[2:0] bits set in *CTRL_REG1_G (10h)*) and corresponding power modes.

To enable low-power mode, the LP_mode bit in *CTRL_REG3_G (12h)* has to be set to ‘1’.

Low-power mode allows reaching low power consumption while maintaining the device always on, refer to *Table 10*.

Table 9. Gyroscope operating mode

ODR_G [2:0]	ODR [Hz]	Power mode(1)
000	Power-down	Power-down
001	14.9	Low-power/Normal mode
010	59.5	Low-power/Normal mode
011	119	Low-power/Normal mode
100	238	Normal mode
101	476	Normal mode
110	952	Normal mode

1. Gyroscope low-power mode is available for G_FS=±2000 dps.

Table 10. Operating mode current consumption

ODR [Hz]	Power mode	Current consumption(1) [mA]
14.9	Low-power	1.8
59.5	Low-power	2.3
119	Low-power	2.9
238	Normal mode	4.3
476	Normal mode	4.3
952	Normal mode	4.3

1. Typical values of gyroscope and accelerometer current consumption based on characterization data.

Table 11. Accelerometer turn-on time

ODR [Hz]	BW = 400 Hz(1)	BW = 200 Hz(1)	BW = 100 Hz(1)	BW = 50 Hz(1)
14.9	0	0	0	0
59.5	0	0	0	0
119	1	1	1	2
238	1	1	2	4
476	1	2	4	7
952	2	4	7	14

1. The table contains the number of samples to be discarded after switching between power-down mode and normal mode.

Table 12. Gyroscope turn-on time

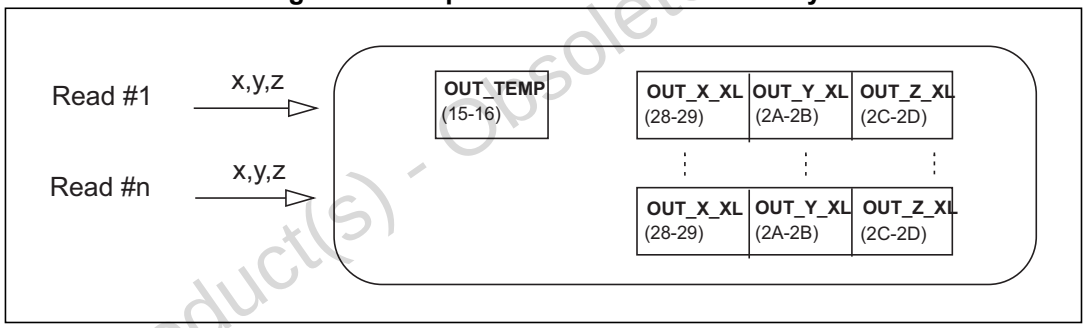
ODR [Hz]	LPF1 only(1)	LPF1 and LPF2(1)
14.9	2	LPF2 not available
59.5 or 119	3	13
238	4	14
476	5	15
952	8	18

1. The table contains the number of samples to be discarded after switching between low-power mode and normal mode.

3.3 Multiple reads (burst)

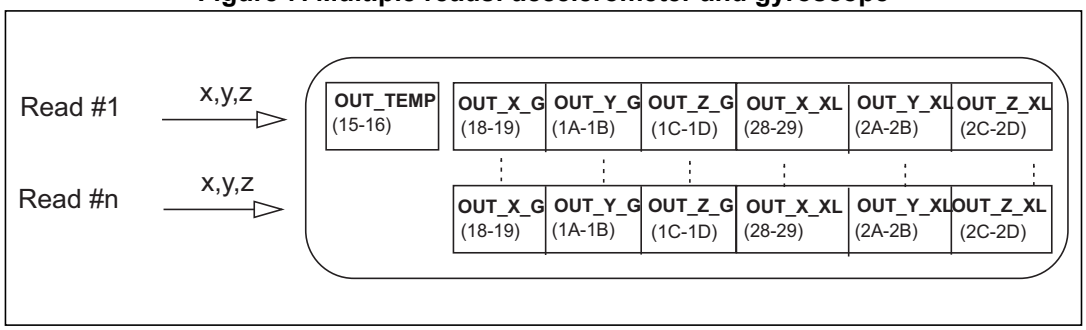
When only the accelerometer is activated and the gyroscope is in power down, starting from *OUT_X_XL (28h - 29h)* multiple reads can be performed. Once *OUT_Z_XL (2Ch - 2Dh)* is read, the system automatically restarts from *OUT_X_XL (28h - 29h)* (see *Figure 6*).

Figure 6. Multiple reads: accelerometer only



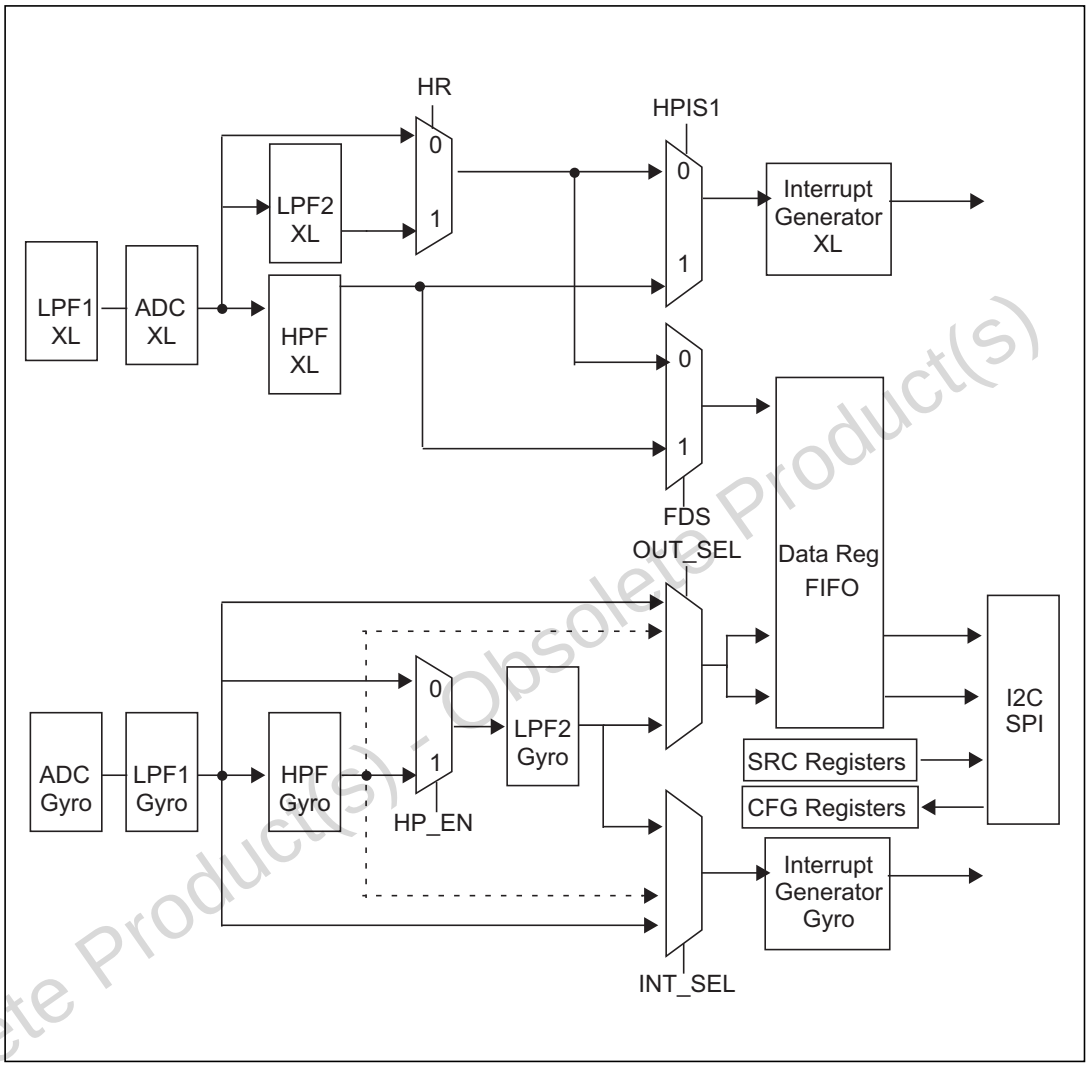
When both the accelerometer and gyroscope sensors are activated at the same ODR, starting from *OUT_X_G (18h - 19h)* multiple reads can be performed. Once *OUT_Z_XL (2Ch - 2Dh)* is read, the system automatically restarts from *OUT_X_G (18h - 19h)* (see *Figure 7*).

Figure 7. Multiple reads: accelerometer and gyroscope



3.4 Digital block diagram

Figure 8. Digital block diagram



3.5 FIFO

The LSM6DS1 embeds 32 slots of 16-bit data FIFO for each of the gyroscope's three output channels, yaw, pitch and roll, and 16-bit data FIFO for each of the accelerometer's three output channels, X, Y and Z. This allows consistent power saving for the system, since the host processor does not need to continuously poll data from the sensor, but it can wake up only when needed and burst the significant data out from the FIFO. This buffer can work accordingly to five different modes: Bypass mode, FIFO mode, Continuous mode, Continuous-to-FIFO mode and Bypass-to-Continuous. Each mode is selected by the FMODE [2:0] bits in the *FIFO_CTRL (2Eh)* register. Programmable FIFO threshold status, FIFO overrun events and the number of unread samples stored are available in the *FIFO_SRC (2Fh)* register and can be set to generate dedicated interrupts on the INT1 pin using the *INT1_CTRL (0Ch)* register.

FIFO_SRC (2Fh)(FTH) goes to '1' when the number of unread samples (*FIFO_SRC (2Fh)* (FSS5:0)) is greater than or equal to FTH [4:0] in *FIFO_CTRL (2Eh)*. If *FIFO_CTRL (2Eh)* (FTH[4:0]) is equal to 0, *FIFO_SRC (2Fh)*(FTH) goes to '0'.

FIFO_SRC (2Fh)(OVRN) is equal to '1' if a FIFO slot is overwritten.

FIFO_SRC (2Fh)(FSS [5:0]) contains stored data levels of unread samples. When FSS [5:0] is equal to '000000', FIFO is empty. When FSS [5:0] is equal to '100000', FIFO is full and the unread samples are 32.

The FIFO feature is enabled by writing '1' in *CTRL_REG9 (23h)* (FIFO_EN).

To guarantee the correct acquisition of data during the switching into and out of FIFO mode, the first sample acquired must be discarded.

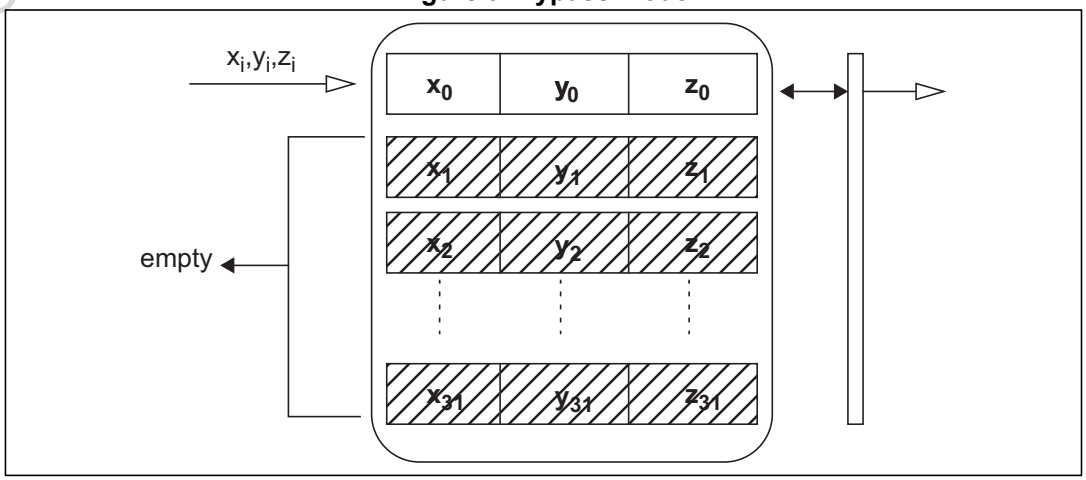
3.5.1 Bypass mode

In Bypass mode (*FIFO_CTRL (2Eh)*(FMODE [2:0]= 000), the FIFO is not operational and it remains empty.

Bypass mode is also used to reset the FIFO when in FIFO mode.

As described in *Figure 9*, for each channel only the first address is used. When a new data is available, the old data is overwritten.

Figure 9. Bypass mode



3.5.2 FIFO mode

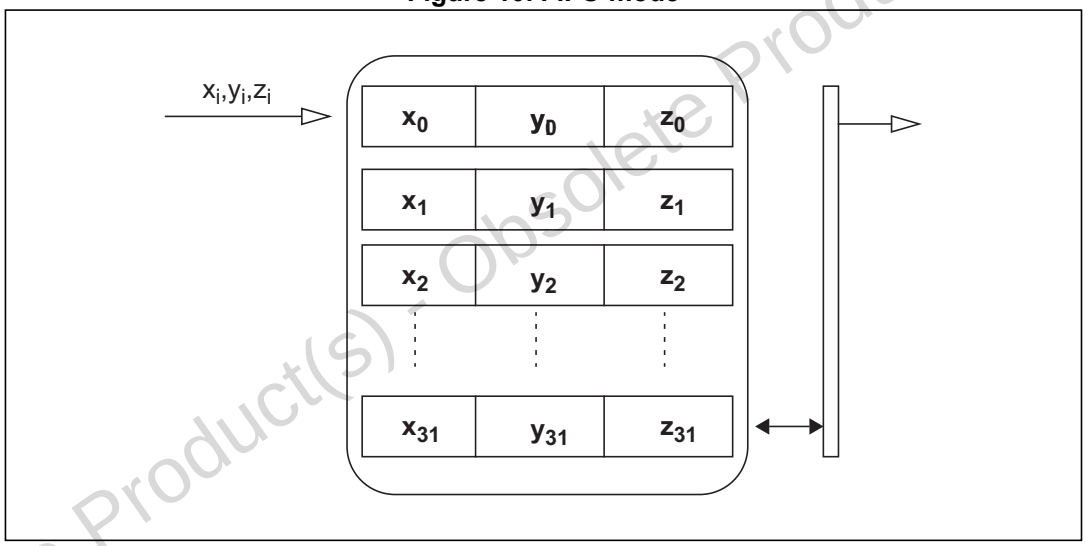
In FIFO mode (*FIFO_CTRL (2Eh)* (FMODE [2:0] = 001) data from the output channels are stored in the FIFO until it is overwritten.

To reset FIFO content, Bypass mode should be selected by writing *FIFO_CTRL (2Eh)* (FMODE [2:0]) to '000'. After this reset command, it is possible to restart FIFO mode writing, *FIFO_CTRL (2Eh)* (FMODE [2:0]) to '001'.

The FIFO buffer memorizes 32 levels of data, but the depth of the FIFO can be resized by setting the STOP_ON_FTH bit in *CTRL_REG9 (23h)*. If the STOP_ON_FTH bit is set to '1', FIFO depth is limited to *FIFO_CTRL (2Eh)*(FTH [4:0]) + 1 data.

A FIFO threshold interrupt can be enabled (INT_OVR bit in *INT1_CTRL (0Ch)*) in order to be raised when the FIFO is filled to the level specified by the FTH[4:0] bits of *FIFO_CTRL (2Eh)*. When a FIFO threshold interrupt occurs, the first data has been overwritten and the FIFO stops collecting data from the input channels.

Figure 10. FIFO mode



3.5.3 Continuous mode

Continuous mode (*FIFO_CTRL (2Eh)*(FMODE[2:0] = 110) provides a continuous FIFO update: as new data arrives the older is discarded.

A FIFO threshold flag *FIFO_SRC (2Fh)*(FTH) is asserted when the number of unread samples in FIFO is greater than or equal to *FIFO_CTRL (2Eh)*(FTH4:0).

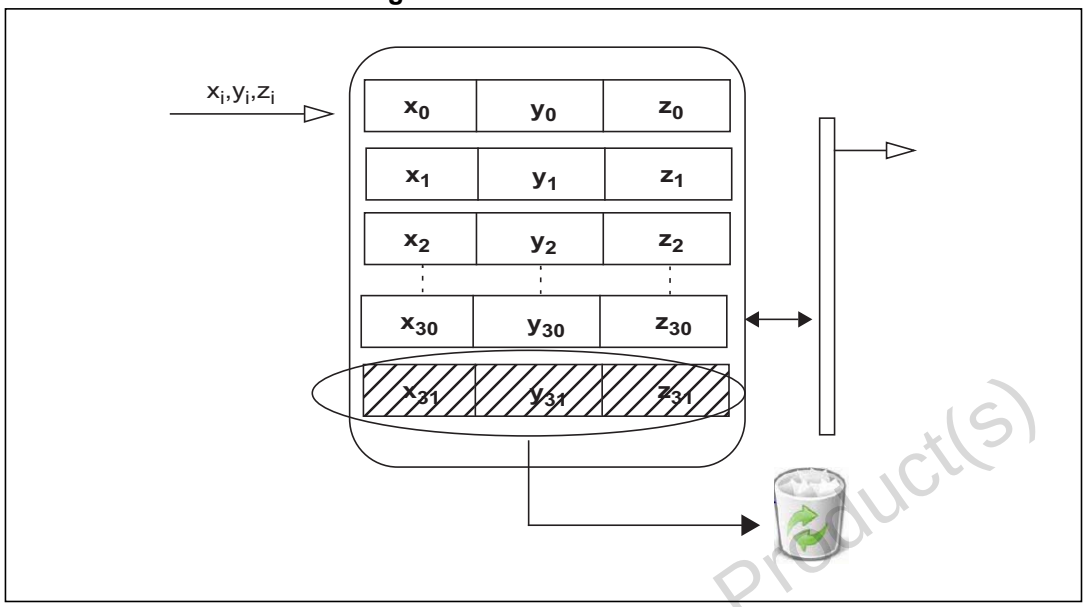
It is possible to route *FIFO_SRC (2Fh)*(FTH) to the INT1 pin by writing the INT_FTH bit to ‘1’in register *INT1_CTRL (0Ch)*.

A full-flag interrupt can be enabled, *INT1_CTRL (0Ch)* (INT_ FSS5) = '1' when FIFO becomes saturated and in order to read the contents all at once.

If an overrun occurs, the oldest sample in FIFO is overwritten and the OVRN flag in *FIFO_SRC (2Fh)* is asserted.

In order to empty the FIFO before it is full, it is also possible to pull from FIFO the number of unread samples available in *FIFO_SRC (2Fh)* (FSS[5:0]).

Figure 11. Continuous mode



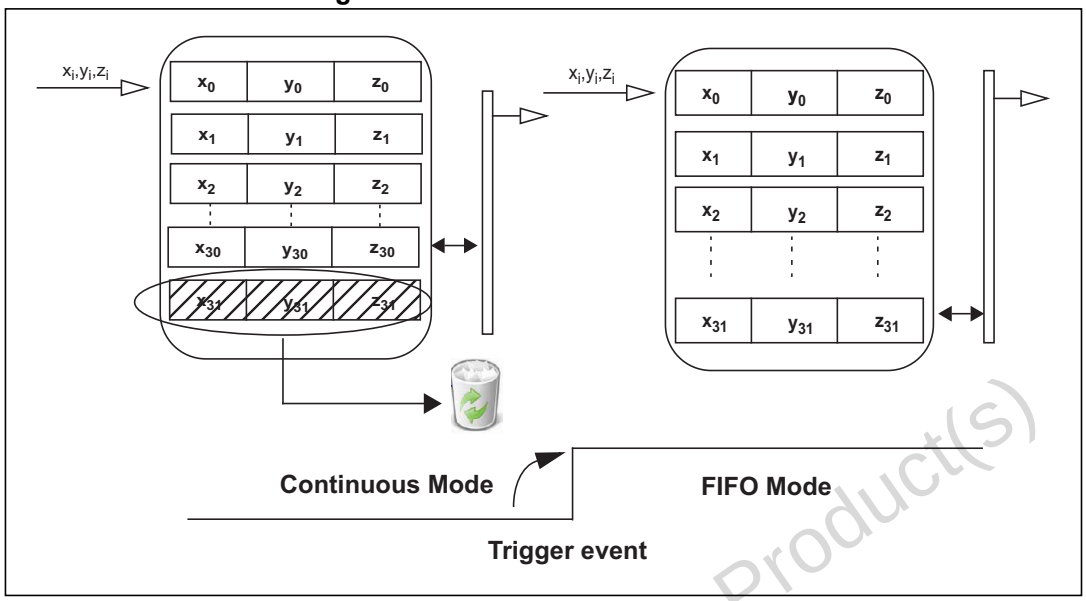
3.5.4 Continuous-to-FIFO mode

In Continuous-to-FIFO mode (*FIFO_CTRL (2Eh)*(FMODE [2:0] = 011), FIFO behavior changes according to the *INT1_GEN_SRC_XL (26h)* (IA1_XL) bit. When the *INT1_GEN_SRC_XL (26h)* (IA1_XL) bit is equal to '1', FIFO operates in FIFO mode. When the *INT1_GEN_SRC_XL (26h)* (IA1_XL) bit is equal to '0', FIFO operates in Continuous mode.

The interrupt generator should be set to the desired configuration by means of *INT_GEN_CFG1_XL (06h)*, *INT_GEN_THS1_X_XL (07h)*, *INT_GEN_THS1_Y_XL (08h)* and *INT_GEN_THS1_Z_XL (09h)*.

CTRL_REG4 (1Eh)(LIR_XL) bit should be set to '1' in order to have latched interrupt.

Figure 12. Continuous-to-FIFO mode



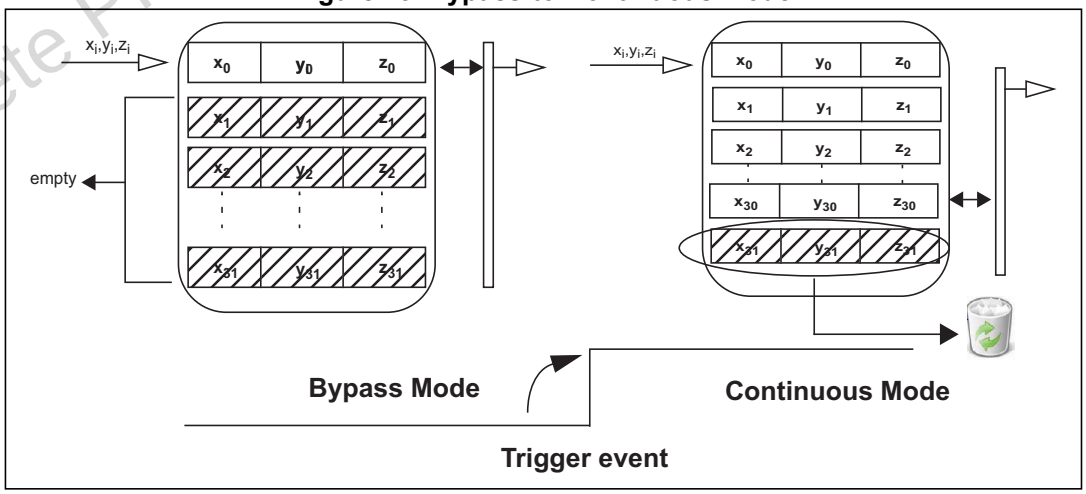
3.5.5 Bypass-to-Continuous mode

In Bypass-to-Continuous mode (*FIFO_CTRL (2Eh)*(FMODE[2:0] = '100'), data measurement storage inside FIFO operates in Continuous mode when *INT1_GEN_SRC_XL (26h)* (IA1_XL) is equal to '1', otherwise FIFO content is reset (Bypass mode).

The interrupt generator should be set to the desired configuration by means of *INT_GEN_CFG1_XL (06h)*, *INT_GEN_THS1_X_XL (07h)*, *INT_GEN_THS1_Y_XL (08h)* and *INT_GEN_THS1_Z_XL (09h)*.

The *CTRL_REG4 (1Eh)*(LIR_XL) bit should be set to '1' in order to have latched interrupt.

Figure 13. Bypass-to-Continuous mode



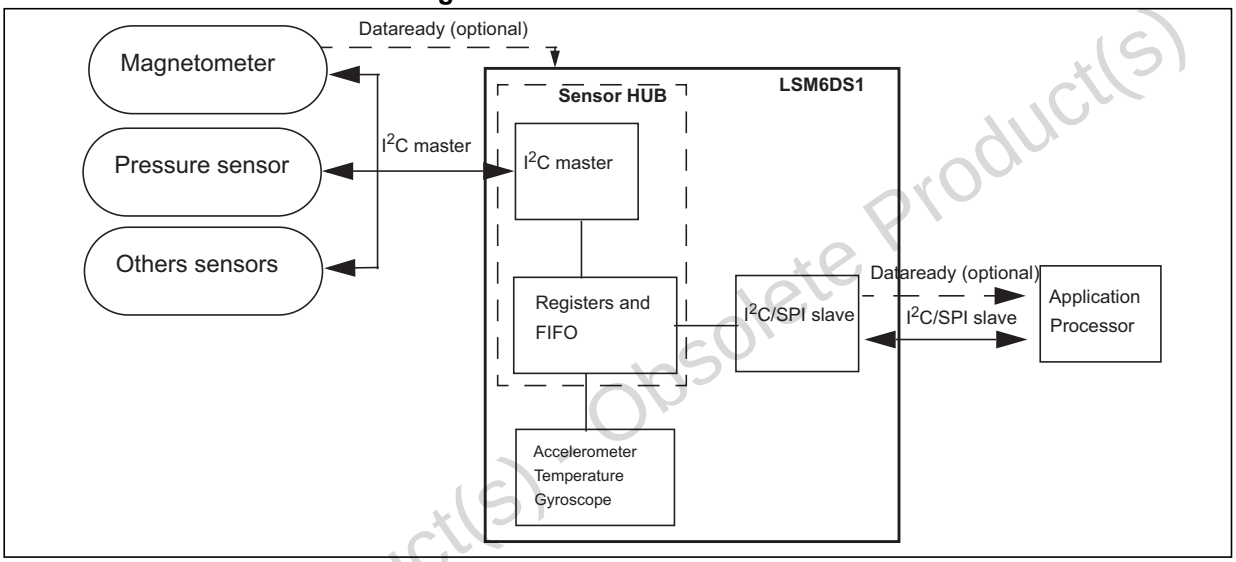
3.6 Sensor hub

3.6.1 Sensor hub description

In the LSM6DS1 the embedded sensor hub allows acquiring data from external sensors and collecting them in dedicated registers and FIFO using the I^2C master interface. These data can be read by the application processor accessing the LSM6DS1 registers through the SPI/ I^2C interfaces.

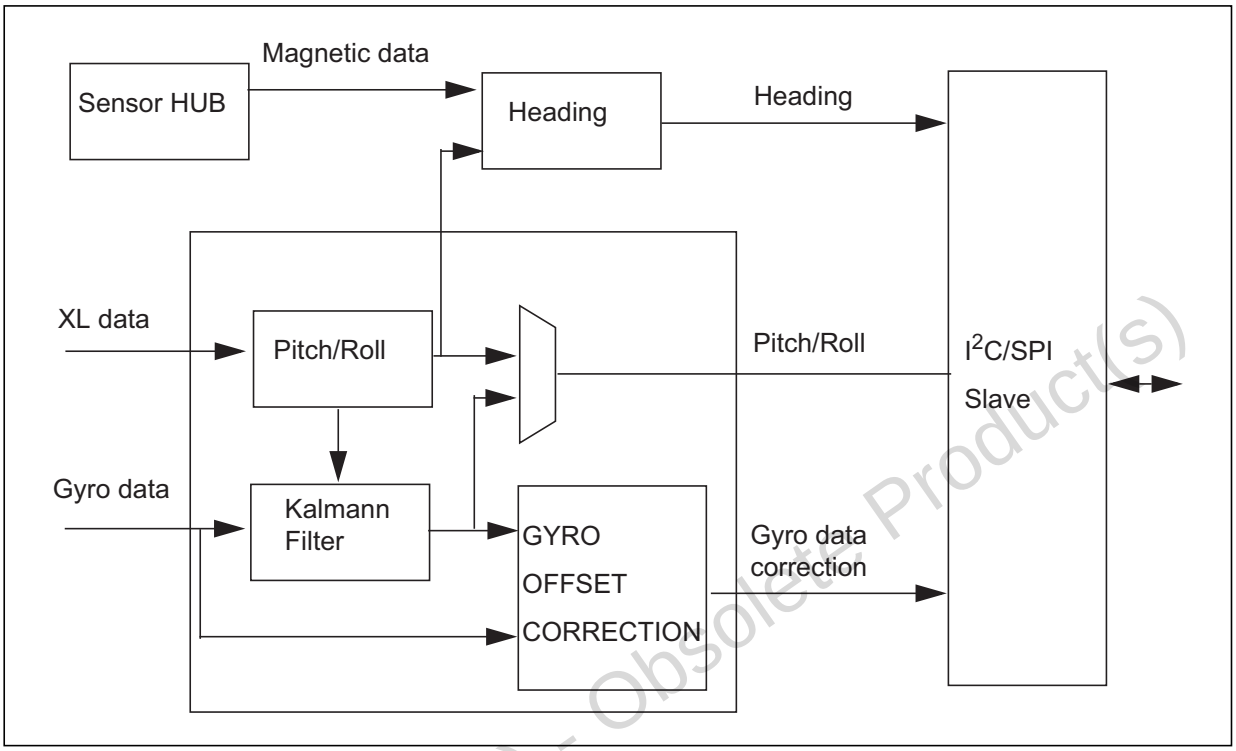
3.6.2 Sensor hub block diagram

Figure 14. LSM6DS1 sensor hub



3.7 Embedded functionalities

Figure 15. Embedded functionalities- block diagram



In the LSM6DS1 the embedded functionalities available are the following:

- Heading: it works if an external magnetometer is connected to the master; output data can be read in dedicated registers *HEADING_DATA_L/HEADING_DATA_H (D4h, D5h)*
- Pitch/Roll angular position: it is calculated from the accelerometer data or from the Kalmann filter; output data can be read in dedicated registers *PITCH_ANGLE_L/PITCH_ANGLE_H (CCh, CDh)* and *ROLL_ANGLE_L/ROLL_ANGLE_H (CEh, CFh)*.
- Gyroscope data correction: gyroscope output is stabilized using information coming from the accelerometer. The offset used to correct the output data can be read in dedicated registers *GYRO_OFS_PITCH_DATA_L/GYRO_OFS_PITCH_DATA_H (D0h, D1h)* and *GYRO_OFS_ROLL_DATA_L/GYRO_OFS_ROLL_DATA_H (D2h, D3h)*.

4 Digital interfaces

The registers embedded inside the LSM6DS1 may be accessed through both the I^2C slave and SPI serial interfaces. The latter may be SW configured to operate either in 3-wire or 4-wire interface mode.

The serial interfaces are mapped onto the same pins. To select/exploit the I^2C slave interface, the CS line must be tied high (i.e connected to Vdd_IO).

Table 13. Serial interface pin description

Pin name	Pin description
CS	SPI enable I^2C/SPI mode selection (1: SPI idle mode / I2C slave communication enabled; 0: SPI communication mode / I2C slave disabled)
SCL_S/SPC	I^2C slave Serial Clock (SCL_S) SPI Serial Port Clock (SPC)
SDA_S/SDI/SDO	I^2C slave Serial Data (SDA_S) SPI Serial Data Input (SDI) 3-wire Interface Serial Data Output (SDO)
SDO/SA0	SPI Serial Data Output (SDO) I^2C slave less significant bit of the device address

4.1 I^2C serial interface

The LSM6DS1 I^2C slave is a bus slave. The I^2C slave is employed to write the data to the registers, whose content can also be read back.

The relevant I^2C terminology is provided in the table below.

Table 14. I^2C terminology

Term	Description
Transmitter	The device which sends data to the bus
Receiver	The device which receives data from the bus
Master	The device which initiates a transfer, generates clock signals and terminates a transfer
Slave	The device addressed by the master

There are two signals associated with the I^2C slave bus: the serial clock line (SCL_S) and the Serial DAta line (SDA_S). The latter is a bidirectional line used for sending and receiving the data to/from the interface. Both the lines must be connected to Vdd_IO through an external pull-up resistor. When the bus is free, both the lines are high.

The I^2C slave interface is implemeted with fast mode (400 kHz) I^2C standards as well as with the standard mode.

In order to disable the I^2C block, the I2C_disable bit must be written to ‘1’ in *CTRL_REG9 (23h)*.

4.1.1 I²C operation

The transaction on the bus is started through a START (ST) signal. A START condition is defined as a high-to-low transition on the data line while the SCL_S line is held high. After this has been transmitted by the master, the bus is considered busy. The next byte of data transmitted after the start condition contains the address of the slave in the first 7 bits and the eighth bit tells whether the master is receiving data from the slave or transmitting data to the slave. When an address is sent, each device in the system compares the first seven bits after a start condition with its address. If they match, the device considers itself addressed by the master.

The Slave ADdress (SAD) associated to the LSM6DS1 is 110101xb. The SDO/SA0 pin can be used to modify the less significant bit of the device address. If the SDO/SA0 pin is connected to the voltage supply LSb is '1' (address 1101011b), else if the SDO/SA0 pin is connected to ground, the LSb value is '0' (address 1101010b). This solution permits to connect and address two different inertial modules to the same I²C bus.

Data transfer with acknowledge is mandatory. The transmitter must release the SDA line during the acknowledge pulse. The receiver must then pull the data line low so that it remains stable low during the high period of the acknowledge clock pulse. A receiver which has been addressed is obliged to generate an acknowledge after each byte of data received.

The I²C embedded inside the LSM6DS1 behaves like a slave device and the following protocol must be adhered to. After the start condition (ST) a slave address is sent, once a slave acknowledge (SAK) has been returned, an 8-bit sub-address (SUB) is transmitted. The increment of the address is configured by the *CTRL_REG8 (22h)* (IF_ADD_INC).

The slave address is completed with a Read/Write bit. If the bit was '1' (Read), a repeated START (SR) condition must be issued after the two sub-address bytes. If the bit is '0' (Write) the master will transmit to the slave with direction unchanged. *Table 15* explains how the SAD+Read/Write bit pattern is composed, listing all the possible configurations.

Table 15. SAD+Read/Write patterns

Command	SAD[6:1]	SAD[0] = SA0	R/W	SAD+R/W
Read	110101	0	1	11010101 (D5h)
Write	110101	0	0	11010100 (D4h)
Read	110101	1	1	11010111 (D7h)
Write	110101	1	0	11010110 (D6h)

Table 16. Transfer when master is writing one byte to slave

Master	ST	SAD + W		SUB		DATA		SP
Slave			SAK		SAK		SAK	

Table 17. Transfer when master is writing multiple bytes to slave

Master	ST	SAD + W		SUB		DATA		DATA		SP
Slave			SAK		SAK		SAK		SAK	

Table 18. Transfer when master is receiving (reading) one byte of data from slave

Master	ST	SAD + W		SUB		SR	SAD + R			NMAK	SP
Slave			SAK		SAK			SAK	DATA		

Table 19. Transfer when master is receiving (reading) multiple bytes of data from slave

Master	ST	SAD+W		SUB		SR	SAD+R			MAK		MAK		NMAK	SP
Slave			SAK		SAK			SAK	DATA		DATA		DATA		

Data are transmitted in byte format (DATA). Each data transfer contains 8 bits. The number of bytes transferred per transfer is unlimited. Data is transferred with the Most Significant bit (MSb) first. If a receiver can't receive another complete byte of data until it has performed some other function, it can hold the clock line, SCL_S low to force the transmitter into a wait state. Data transfer only continues when the receiver is ready for another byte and releases the data line. If a slave receiver doesn't acknowledge the slave address (i.e. it is not able to receive because it is performing some real-time function) the data line must be left high by the slave. The master can then abort the transfer. A low-to-high transition on the SDA_S line while the SCL_S line is high is defined as a STOP condition. Each data transfer must be terminated by the generation of a STOP (SP) condition.

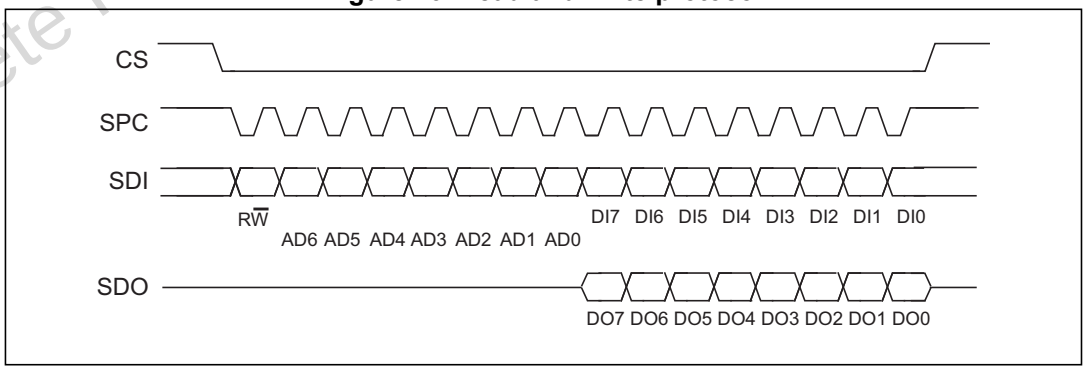
In the presented communication format MAK is Master acknowledge and NMAK is No Master Acknowledge.

4.2 SPI bus interface

The LSM6DS1 SPI is a bus slave. The SPI allows to write and read the registers of the device.

The serial interface connects to applications using 4 wires: **CS**, **SPC**, **SDI** and **SDO**.

Figure 16. Read and write protocol



CS is the serial port enable and it is controlled by the SPI master. It goes low at the start of the transmission and goes back high at the end. **SPC** is the serial port clock and it is controlled by the SPI master. It is stopped high when **CS** is high (no transmission). **SDI** and **SDO** are respectively the serial port data input and output. Those lines are driven at the falling edge of **SPC** and should be captured at the rising edge of **SPC**.

Both the read register and write register commands are completed in 16 clock pulses or in multiples of 8 in case of multiple read/write bytes. Bit duration is the time between two falling edges of **SPC**. The first bit (bit 0) starts at the first falling edge of **SPC** after the falling edge of **CS** while the last bit (bit 15, bit 23, ...) starts at the last falling edge of SPC just before the rising edge of **CS**.

bit 0: R$\overline{W}$ bit. When 0, the data DI(7:0) is written into the device. When 1, the data DO(7:0) from the device is read. In latter case, the chip will drive **SDO** at the start of bit 8.

bit 1-7: address AD(6:0). This is the address field of the indexed register.

bit 8-15: data DI(7:0) (write mode). This is the data that is written into the device (MSb first).

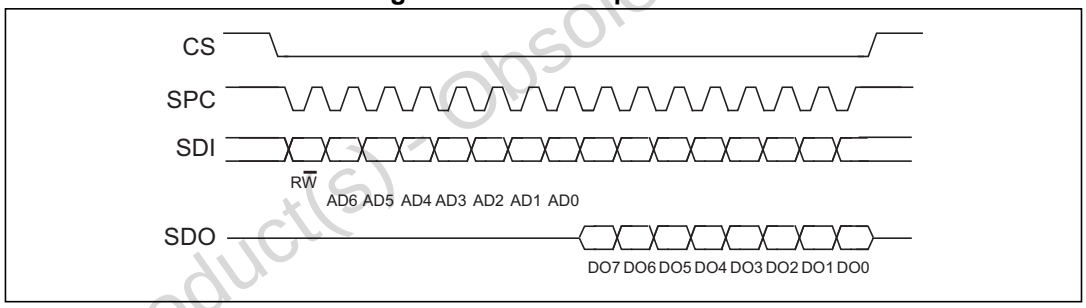
bit 8-15: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

In multiple read/write commands further blocks of 8 clock periods will be added. When the *CTRL_REG8 (22h)* (IF_ADD_INC) bit is '0', the address used to read/write data remains the same for every block. When the *CTRL_REG8 (22h)*(IF_ADD_INC) bit is '1', the address used to read/write data is increased at every block.

The function and the behavior of **SDI** and **SDO** remain unchanged.

4.2.1 SPI read

Figure 17. SPI read protocol



The SPI read command is performed with 16 clock pulses. A multiple byte read command is performed by adding blocks of 8 clock pulses to the previous one.

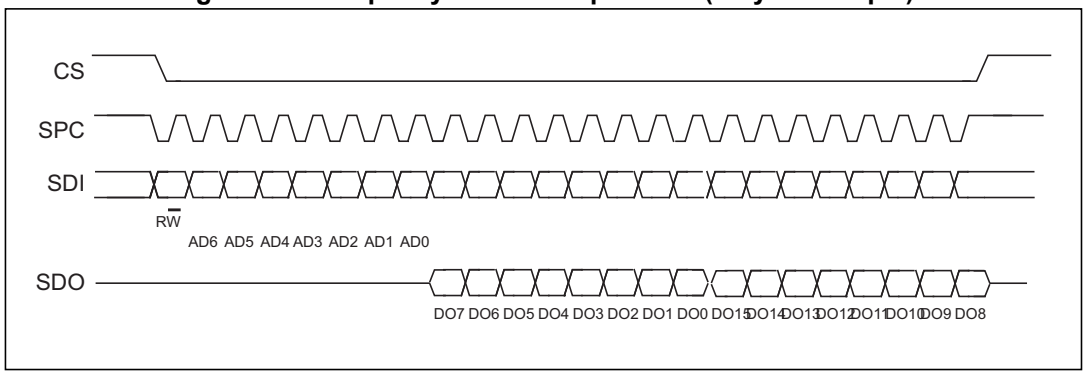
bit 0: READ bit. The value is 1.

bit 1-7: address AD(6:0). This is the address field of the indexed register.

bit 8-15: data DO(7:0) (read mode). This is the data that will be read from the device (MSb first).

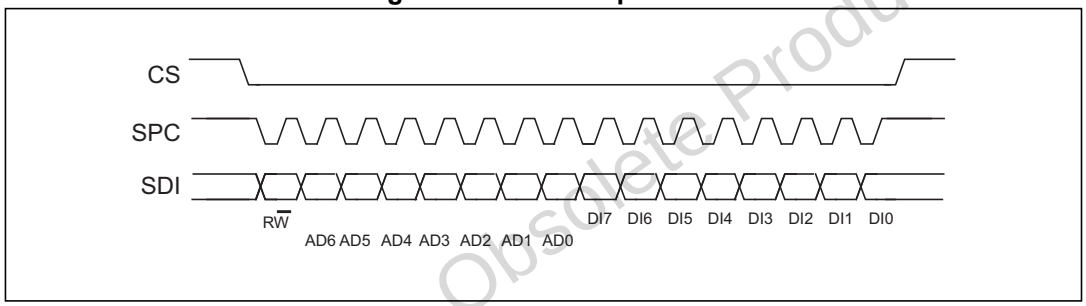
bit 16-... : data DO(...-8). Further data in multiple byte reads.

Figure 18. Multiple byte SPI read protocol (2-byte example)



4.2.2 SPI write

Figure 19. SPI write protocol



The SPI write command is performed with 16 clock pulses. A multiple byte write command is performed by adding blocks of 8 clock pulses to the previous one.

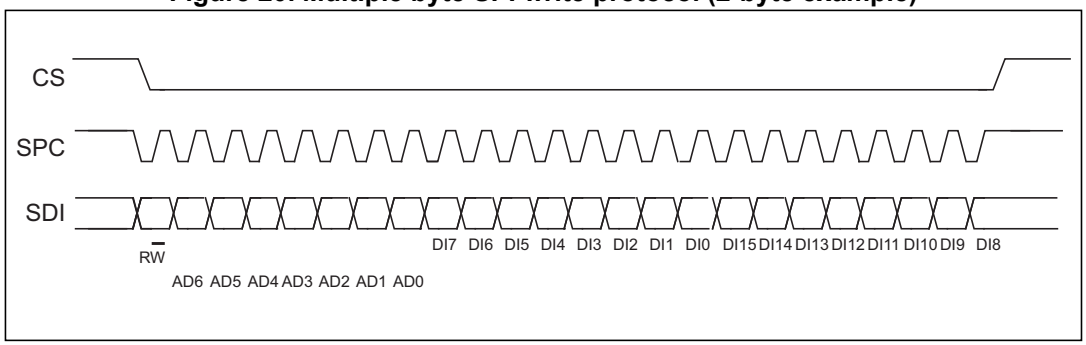
bit 0: WRITE bit. The value is 0.

bit 1 -7: address AD(6:0). This is the address field of the indexed register.

bit 8-15: data DI(7:0) (write mode). This is the data that is written inside the device (MSb first).

bit 16-... : data DI(...-8). Further data in multiple byte writes.

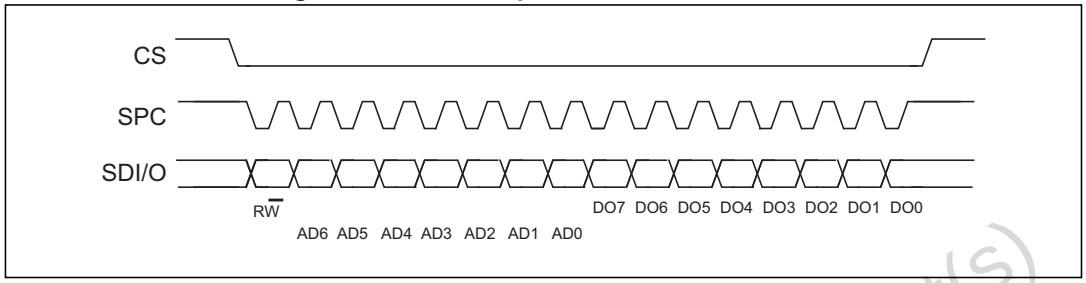
Figure 20. Multiple byte SPI write protocol (2-byte example)



4.2.3 SPI read in 3-wire mode

3-wire mode is entered by setting the *CTRL_REG8 (22h)*(SIM) bit equal to '1' (SPI serial interface mode selection).

Figure 21. SPI read protocol in 3-wire mode



The SPI read command is performed with 16 clock pulses:

bit 0: READ bit. The value is 1.

bit 1-7: address AD(6:0). This is the address field of the indexed register.

bit 8-15: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

A multiple read command is also available in 3-wire mode.

5 Register mapping

The table given below provides a list of the 8/16 bit registers embedded in the device and the corresponding addresses.

Table 20. Register mapping

Name	Type	Register address		Default	Note
		Hex	Binary		
Reserved		00	00000000	--	Reserved
INT_GEN_CFG2_XL	r/w	01	00000001	00000000	
INT_GEN_THS2_XL	r/w	02	00000010	00000000	
INT_GEN_DUR2_XL	r/w	03	00000011	00000000	
ACT_THS	r/w	04	00000100	00000000	
ACT_DUR	r/w	05	00000101	00000000	
INT_GEN_CFG1_XL	r/w	06	00000110	00000000	
INT_GEN_THS1_X_XL	r/w	07	00000111	00000000	
INT_GEN_THS1_Y_XL	r/w	08	00001000	00000000	
INT_GEN_THS1_Z_XL	r/w	09	00001001	00000000	
INT_GEN_DUR1_XL	r/w	0A	00001010	00000000	
REFERENCE_G	r/w	0B	00001011	00000000	
INT1_CTRL	r/w	0C	00001100	00000000	
INT2_CTRL	r/w	0D	00001101	00000000	
Reserved	--	0E	--	--	Reserved
WHO_AM_I	r	0F	00001111	01101000	
CTRL_REG1_G	r/w	10	00010000	00000000	
CTRL_REG2_G	r/w	11	00010001	00000000	
CTRL_REG3_G	r/w	12	00010010	00000000	
ORIENT_CFG_G	r/w	13	00010011	00000000	
INT_GEN_SRC_G	r	14	00010100	output	
OUT_TEMP_L	r	15	00010101	output	
OUT_TEMP_H	r	16	00010110	output	
STATUS_REG	r	17	00010111	output	
OUT_X_L_G	r	18	00011000	output	
OUT_X_H_G	r	19	00011001	output	
OUT_Y_L_G	r	1A	00011010	output	
OUT_Y_H_G	r	1B	00011011	output	
OUT_Z_L_G	r	1C	00011100	output	

Name	Type	Register address		Default	Note
		Hex	Binary		
OUT_Z_H_G	r	1D	00011101	output	
CTRL_REG4	r/w	1E	00011110	00111000	
CTRL_REG5_XL	r/w	1F	00011111	00111000	
CTRL_REG6_XL	r/w	20	00100000	00000000	
CTRL_REG7_XL	r/w	21	00100001	00000000	
CTRL_REG8	r/w	22	00100010	00000100	
CTRL_REG9	r/w	23	00100011	00000000	
CTRL_REG10	r/w	24	00100100	00000000	
INT2_GEN_SRC_XL	r	25	00100101	output	
INT1_GEN_SRC_XL	r	26	00100110	output	
STATUS_REG	r	27	00100111	output	
OUT_X_L_XL	r	28	00101000	output	
OUT_X_H_XL	r	29	00101001	output	
OUT_Y_L_XL	r	2A	00101010	output	
OUT_Y_H_XL	r	2B	00101011	output	
OUT_Z_L_XL	r	2C	00101100	output	
OUT_Z_H_XL	r	2D	00101101	output	
FIFO_CTRL	r/w	2E	00101110	00000000	
FIFO_SRC	r	2F	00101111	output	
INT_GEN_CFG_G	r/w	30	00110000	00000000	
INT_GEN_THS_XH_G	r/w	31	00110001	00000000	
INT_GEN_THS_XL_G	r/w	32	00110010	00000000	
INT_GEN_THS_YH_G	r/w	33	00110011	00000000	
INT_GEN_THS_YL_G	r/w	34	00110100	00000000	
INT_GEN_THS_ZH_G	r/w	35	00110101	00000000	
INT_GEN_THS_ZL_G	r/w	36	00110110	00000000	
INT_GEN_DUR_G	r/w	37	00110111	00000000	
Reserved	--	38-7F	--	--	Reserved
EXTERNAL_SENSORS_DATA	r	80-8F	--	output	
MASTER_SYNC_REG	r/w	90	10010000	00000000	
MASTER_FSM_REG	r/w	91	10010001	01011000	
Reserved	--	92-96	--	--	Reserved
MASTER_STATUS_REG	r	97	10010111	00000000	
Reserved	--	98-AF	--	--	Reserved

Name	Type	Register address		Default	Note
		Hex	Binary		
SLAVE0_I2C_ADD	r/w	B0	10110000	00000000	
SLAVE0_SUB_ADD	r/w	B1	10110001	00000000	
Reserved	--	B2-B4	--	--	Reserved
SLAVE0_DATA_TO_WRITE	r/w	B5	10110101	00000000	
SLAVE0_CONFIG	r/w	B6	10110110	00000000	
SLAVE0_BYTE_TO_READ	r/w	B7	10110111	00000000	
SLAVE1_I2C_ADDD	r/w	B8	10111000	00000000	
SLAVE1_SUB_ADD	r/w	B9	10111001	00000000	
SLAVE1_DATA_TO_WRITE	r/w	BA	10111010	00000000	
SLAVE1_CONFIG	r/w	BB	10111011	00000000	
SLAVE1_BYTE_TO_READ	r/w	BC	10111100	00000000	
SLAVE2_I2C_ADD	r/w	BD	10111101	00000000	
SLAVE2_SUB_ADD	r/w	BE	10111110	00000000	
SLAVE2_DATA_TO_WRITE	r/w	BF	10111111	00000000	
SLAVE2_CONFIG	r/w	C0	11000000	00000000	
SLAVE2_BYTE_TO_READ	r/w	C1	11000001	00000000	
MAGNETOMETER_ROUTINES	r/w	C2	11000010	00000000	
Reserved	--	C3-C8	11000011	--	Reserved
GYRO_OFS_XY_ON_OUT	r/w	C9	11001001	00100010	
MAG_CFG	r/w	CA	11001010	00000000	
Reserved	--	CB	11001011	--	Reserved
PITCH_ANGLE_L	r	CC	11001100	output	
PITCH_ANGLE_H	r	CD	11001101	output	
ROLL_ANGLE_L	r	CE	11001110	output	
ROLL_ANGLE_H	r	CF	11001111	output	
GYRO_OFS_PITCH_DATA_L	r	D0	11010000	output	
GYRO_OFS_PITCH_DATA_H	r	D1	11010001	output	
GYRO_OFS_ROLL_DATA_L	r	D2	11010010	output	
GYRO_OFS_ROLL_DATA_H	r	D3	11010011	output	
HEADING_DATA_L	r	D4	11010100	output	
HEADING_DATA_H	r	D5	11010101	output	

Registers marked as *Reserved* must not be changed. Writing to those registers may cause permanent damages to the device.

To guarantee proper behavior of the device, all register addresses not listed in the above table must not be accessed and the content stored on those registers must not be changed.

The content of the registers that are loaded at boot should not be changed. They contain the factory calibration values. Their content is automatically restored when the device is powered up.

6 Register description

The device contains a set of registers which are used to control its behavior and to retrieve linear acceleration, angular rate and temperature data. The register addresses, made up of 7 bits, are used to identify them and to write the data through the serial interface.

6.1 INT_GEN_CFG2_XL (01h)

Linear acceleration sensor interrupt generator 2 configuration register (r/w).

Table 21. INT_GEN_CFG2_XL register

AOI2_XL	6D2	ZHIE2_XL	ZLIE2_XL	YHIE2_XL	YLIE2_XL	XHIE2_XL	XLIE2_XL

Table 22. INT_GEN_CFG2_XL register description

AOI2_XL	And/Or combination of accelerometer's interrupt 2 events. Default value: 0 (0: OR combination; 1: AND combination)
6D2	6-direction detection function for interrupt 2. Default value: 0 (0: disabled; 1: enabled)
ZHIE2_XL	Enable interrupt 2 generation on accelerometer's Z-axis high event or on direction recognition. Default value: 0 (0: disable interrupt request; 1: enable interrupt request)
ZLIE2_XL	Enable interrupt 2 generation on accelerometer's Z-axis low event or on direction recognition. Default value: 0 (0: disable interrupt request; 1: enable interrupt request)
YHIE2_XL	Enable interrupt 2 generation on accelerometer's Y-axis high event or on direction recognition. Default value: 0 (0: disable interrupt request; 1: enable interrupt request)
YLIE2_XL	Enable interrupt 2 generation on accelerometer's Y-axis low event or on direction recognition. Default value: 0 (0: disable interrupt request; 1: enable interrupt request)
XHIE2_XL	Enable interrupt 2 generation on accelerometer's X-axis high event or on direction recognition. Default value: 0 (0: disable interrupt request; 1: enable interrupt request)
XLIE2_XL	Enable interrupt 2 generation on accelerometer's X-axis low event or on direction recognition. Default value: 0 (0: disable interrupt request; 1: enable interrupt request)

6.2 INT_GEN_THS2_XL (02h)

Linear acceleration sensor interrupt 2 threshold register (r/w).

Table 23. INT_GEN_THS2_XL register

THS2_XL7	THS2_XL6	THS2_XL5	THS2_XL4	THS2_XL3	THS2_XL2	THS2_XL1	THS2_XL0

Table 24. INT_GEN_THS2_XL register description

THS2_XL [7:0]	Interrupt 2 thresholds. Default value: 0000 0000

6.3 INT_GEN_DUR2_XL (03h)

Linear acceleration sensor interrupt 2 duration register (r/w).

Table 25. INT_GEN_DUR2_XL register

WAIT2_XL	DUR2_XL6	DUR2_XL5	DUR2_XL4	DUR2_XL3	DUR2_XL2	DUR2_XL1	DUR2_XL0

Table 26. INT_GEN_DUR2_XL register description

WAIT2_XL	Wait function enable on duration counter. Default value: 0 (0: wait function off; 1: wait for DUR2_XL [6:0] samples before exiting from interrupt 2)
DUR2_XL [6:0]	Enter/exit interrupt 2 duration value. Default value: 000 0000

6.4 ACT_THS (04h)

Activity threshold register.

Table 27. ACT_THS register

SLEEP_ON_ INACT_EN	ACT_THS6	ACT_THS5	ACT_THS4	ACT_THS3	ACT_THS2	ACT_THS1	ACT_THS0

Table 28. ACT_THS register description

SLEEP_ON_ INACT_EN	Gyroscope operating mode during inactivity. Default value: 0 (0: Gyroscope in power-down; 1: Gyroscope in sleep mode)
ACT_THS [6:0]	Inactivity threshold. Default value: 000 0000

6.5 ACT_DUR (05h)

Inactivity duration register.

Table 29. ACT_DUR register

ACT_DUR7	ACT_DUR6	ACT_DUR5	ACT_DUR4	ACT_DUR3	ACT_DUR2	ACT_DUR1	ACT_DUR0

Table 30. ACT_DUR register description

ACT_DUR [7:0]	Inactivity duration. Default value: 0000 0000

6.6 INT_GEN_CFG1_XL (06h)

Linear acceleration sensor interrupt 1 generator configuration register.

Table 31. INT_GEN_CFG1_XL register

AOI_XL	6D	ZHIE_XL	ZLIE_XL	YHIE_XL	YLIE_XL	XHIE_XL	XLIE_XL

Table 32. INT_GEN_CFG1_XL register description

AOI_XL	AND/OR combination of accelerometer's interrupt 1 events. Default value: 0 (0: OR combination; 1: AND combination)
6D1	6-direction detection function for interrupt 1. Default value: 0 (0: disabled; 1: enabled)
ZHIE_XL	Enable interrupt 1 generation on accelerometer's Z-axis high event. Default value: 0 (0: disable interrupt request; 1: interrupt request on measured acceleration value higher than preset threshold)
ZLIE_XL	Enable interrupt 1 generation on accelerometer's Z-axis low event. Default value: 0 (0: disable interrupt request; 1: interrupt request on measured acceleration value lower than preset threshold)
YHIE_XL	Enable interrupt 1 generation on accelerometer's Y-axis high event. Default value: 0 (0: disable interrupt request; 1: interrupt request on measured acceleration value higher than preset threshold)
YLIE_XL	Enable interrupt 1 generation on accelerometer's Y-axis low event. Default value: 0 (0: disable interrupt request; 1: interrupt request on measured acceleration value lower than preset threshold)
XHIE_XL	Enable interrupt 1 generation on accelerometer's X-axis high event. Default value: 0 (0: disable interrupt request; 1: interrupt request on measured acceleration value higher than preset threshold)
XLIE_XL	Enable interrupt 1 generation on accelerometer's X-axis low event. Default value: 0 (0: disable interrupt request; 1: interrupt request on measured acceleration value lower than preset threshold)

6.7 INT_GEN_THS1_X_XL (07h)

Linear acceleration sensor interrupt 1 threshold register.

Table 33. INT_GEN_THS1_X_XL register

THS1_XL_X7	THS1_XL_X6	THS1_XL_X5	THS1_XL_X4	THS1_XL_X3	THS1_XL_X2	THS1_XL_X1	THS1_XL_X0

Table 34. INT_GEN_THS1_X_XL register description

THS1_XL_X [7:0]	X-axis interrupt threshold. Default value: 0000 0000

6.8 INT_GEN_THS1_Y_XL (08h)

Linear acceleration sensor interrupt 1 threshold register.

Table 35. INT_GEN_THS1_Y_XL register

THS1_XL_Y7	THS1_XL_Y6	THS1_XL_Y5	THS1_XL_Y4	THS1_XL_Y3	THS1_XL_Y2	THS1_XL_Y1	THS1_XL_Y0

Table 36. INT_GEN_THS1_Y_XL register description

THS1_XL_Y [7:0]	Y-axis interrupt threshold. Default value: 0000 0000

6.9 INT_GEN_THS1_Z_XL (09h)

Linear acceleration sensor interrupt 1 threshold register.

Table 37. INT_GEN_THS1_Z_XL register

THS1_XL_Z7	THS1_XL_Z6	THS1_XL_Z5	THS1_XL_Z4	THS1_XL_Z3	THS1_XL_Z2	THS1_XL_Z1	THS1_XL_Z0

Table 38. INT_GEN_THS1_Z_XL register description

THS1_XL_Z [7:0]	Z-axis interrupt threshold. Default value: 0000 0000

6.10 INT_GEN_DUR1_XL (0Ah)

Linear acceleration sensor interrupt 1 duration register.

Table 39. INT_GEN_DUR1_XL register

WAIT_XL	DUR1_XL 6	DUR1_XL 5	DUR1_XL 4	DUR1_XL 3	DUR1_XL 2	DUR1_XL 1	DUR1_XL 0

Table 40. INT_GEN_DUR1_XL register description

WAIT_XL	Wait function enabled on duration counter. Default value: 0 (0: wait function off; 1: wait for DUR_XL [6:0] samples before exiting interrupt)
DUR1_XL [6:0]	Enter/exit interrupt duration value. Default value: 000 0000

6.11 REFERENCE_G (0Bh)

Angular rate sensor reference value register for digital high-pass filter (r/w).

Table 41. REFERENCE_G register

REF7_G	REF6_G	REF5_G	REF4_G	REF3_G	REF2_G	REF1_G	REF0_G

Table 42. REFERENCE_G register description

REF_G [7:0]	Reference value for gyroscope's digital high-pass filter (r/w). Default value: 0000 0000

6.12 INT1_CTRL (0Ch)

INT1 pin control register.

Table 43. INT1_CTRL register

INT1_IG_G	INT1_IG_XL	INT1_FSS5	INT1_OVR	INT1_FTH	INT1_ Boot	INT1_DRDY_G	INT1_DRDY_XL

Table 44. INT1_CTRL register description

INT1_IG_G	Gyroscope interrupt enable on INT1 pin. Default value: 0 (0: disabled; 1: enabled)
INT1_ IG_XL	Accelerometer interrupt generator on INT1 pin. Default value: 0 (0: disabled; 1: enabled)
INT1_ FSS5	FSS5 interrupt enable on INT1 pin. Default value: 0 (0: disabled; 1: enabled)
INT1_OVR	Overrun interrupt on INT1 pin. Default value: 0 (0: disabled; 1: enabled)
INT1_FTH	FIFO threshold interrupt on INT1 pin. Default value: 0 (0: disabled; 1: enabled)
INT1_ Boot	Boot status available on INT1 pin. Default value: 0 (0: disabled; 1: enabled)
INT1_DRDY_G	Gyroscope data ready on INT1 pin. Default value: 0 (0: disabled; 1: enabled)
INT1_DRDY_XL	Accelerometer data ready on INT1 pin. Default value: 0 (0: disabled; 1: enabled)

6.13 INT2_CTRL (0Dh)

INT2 pin control register.

Table 45. INT2_CTRL register

INT2_INACT	INT2_IG2_XL	INT2_FSS5	INT2_OVR	INT2_FTH	INT2_DRDY_TEMP	INT2_DRDY_G	INT2_DRDY_XL

Table 46. INT2_CTRL register description

INT2_INACT	Gyroscope interrupt enable on INT2 pin. Default value: 0 (0: disabled; 1: enabled)
INT2_ IG2_XL	Accelerometer interrupt 2 generator on INT2 pin. Default value: 0 (0: disabled; 1: enabled)
INT2_ FSS5	FSS5 interrupt enable on INT2 pin. Default value: 0 (0: disabled; 1: enabled)
INT2_OVR	Overrun interrupt on INT2 pin. Default value: 0 (0: disabled; 1: enabled)
INT2_FTH	FIFO threshold interrupt on INT2 pin. Default value: 0 (0: disabled; 1: enabled)
INT2_DRDY_TEMP	Temperature sensor data ready on INT2 pin. Default value: 0 (0: disabled; 1: enabled)
INT2_DRDY_G	Gyroscope data ready on INT2 pin. Default value: 0 (0: disabled; 1: enabled)
INT2_DRDY_XL	Accelerometer data ready on INT2 pin. Default value: 0 (0: disabled; 1: enabled)

6.14 WHO_AM_I (0Fh)

Who_AM_I register.

Table 47. WHO_AM_I register

0	1	1	0	1	0	0	0

6.15 CTRL_REG1_G (10h)

Angular rate sensor control register 1.

Table 48. CTRL_REG1_G register

ODR_G2	ODR_G1	ODR_G0	FS_G1	FS_G0	0(1)	BW_G1	BW_G0

1. This bit must be set to ‘0’ for the correct operation of the device

Table 49. CTRL_REG1_G register description

ODR_G [2:0]	Gyroscope output data rate selection. Default value: 000 (Refer to *Table 50* and *Table 51*)
FS_G [1:0]	Gyroscope full-scale selection. Default value: 00 (00: 245 dps; 01: 500 dps; 11: 2000 dps)
BW_G [1:0]	Gyroscope bandwidth selection. Default value: 00

ODR_G [2:0] are used to set ODR selection when both the accelerometer and gyroscope are activated. BW_G [1:0] are used to set the bandwidth selection of the gyroscope.

The following table summarizes all frequencies available for each combination of the ODR_G / BW_G bits after LPF1 (see *Table 50*) and LPF2 (see *Table 51*) when both the accelerometer and gyroscope are activated. For more details regarding signal processing scheme please refer to *Figure 22*.

Table 50. ODR and BW configuration setting (after LPF1)

ODR_G2	ODR_G1	ODR_G0	ODR [Hz]	Cutoff [Hz](1)
0	0	0	Power-down	n.a.
0	0	1	14.9	5
0	1	0	59.5	19
0	1	1	119	38
1	0	0	238	76
1	0	1	476	100
1	1	0	952	100
1	1	1	n.a.	n.a.

1. Values in the table are indicative and can vary proportionally with the specific ODR value.

Table 51. ODR and BW configuration setting (after LPF2)

ODR_G [2:0]	BW_G [1:0]	ODR [Hz]	Cutoff [Hz](1)
000	00	Power-down	n.a.
000	01	Power-down	n.a.
000	10	Power-down	n.a.
000	11	Power-down	n.a.
001	00	14.9	n.a.
001	01	14.9	n.a.
001	10	14.9	n.a.
001	11	14.9	n.a.
010	00	59.5	16
010	01	59.5	16
010	10	59.5	16
010	11	59.5	16
011	00	119	14
011	01	119	31
011	10	119	31
011	11	119	31
100	00	238	14
100	01	238	29
100	10	238	63
100	11	238	78
101	00	476	21
101	01	476	28
101	10	476	57
101	11	476	100
110	00	952	33
110	01	952	40
110	10	952	58
110	11	952	100
111	00	n.a.	n.a.
111	01	n.a.	n.a.
111	10	n.a.	n.a.
111	11	n.a.	n.a.

1. Values in the table are indicative and can vary proportionally with the specific ODR value.

6.16 CTRL_REG2_G (11h)

Angular rate sensor control register 2.

Table 52. CTRL_REG2_G register

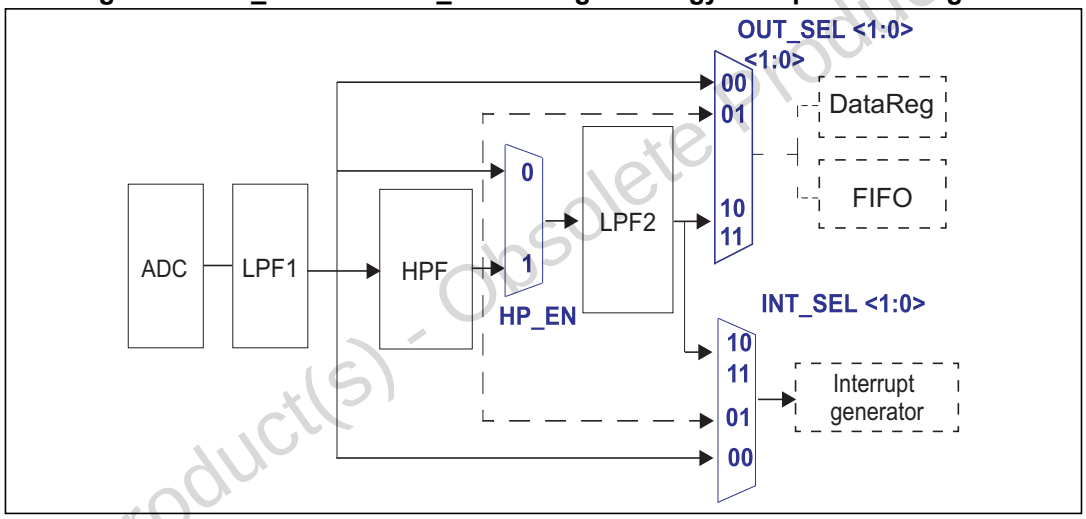
0(1)	0(1)	0(1)	0(1)	INT_SEL1	INT_SEL0	OUT_SEL1	OUT_SEL0

1. These bits must be set to '0' for the correct operation of the device

Table 53. CTRL_REG2_G register description

INT_SEL [1:0]	INT selection configuration. Default value: 00 (Refer to *Figure 22*)
OUT_SEL [1:0]	Out selection configuration. Default value: 00 (Refer to *Figure 22*)

Figure 22. INT_SEL and OUT_SEL configuration gyroscope block diagram



6.17 CTRL_REG3_G (12h)

Angular rate sensor control register 3.

Table 54. CTRL_REG3_G register

LP_mode	HP_EN	0(1)	0(1)	HPCF3_G	HPCF2_G	HPCF1_G	HPCF0_G

1. These bits must be set to '0' for the correct operation of the device

Table 55. CTRL_REG3_G register description

LP_mode	Low-power mode enable. Default value: 0 (0: Low-power disable; 1:Low power enable)
HP_EN	High-pass filter enable. Default value: 0 (0: HPF disabled; 1: HPF enabled, refer to *Figure 22*)
HPCF_G [3:0]	Gyroscope high-pass filter cutoff frequency selection. Default value: 0000 Refer to *Table 56*.

Table 56. Gyroscope high-pass filter cutoff frequency configuration [Hz](1)

HPCF_G [3:0]	ODR = 14.9 Hz	ODR = 59.5 Hz	ODR = 119 Hz	ODR = 238 Hz	ODR = 476 Hz	ODR = 952 Hz
0000	1	4	8	15	30	57
0001	0.5	2	4	8	15	30
0010	0.2	1	2	4	8	15
0011	0.1	0.5	1	2	4	8
0100	0.05	0.2	0.5	1	2	4
0101	0.02	0.1	0.2	0.5	1	2
0110	0.01	0.05	0.1	0.2	0.5	1
0111	0.005	0.02	0.05	0.1	0.2	0.5
1000	0.002	0.01	0.02	0.05	0.1	0.2
1001	0.001	0.005	0.01	0.02	0.05	0.1

1. Values in the table are indicative and can vary proportionally with the specific ODR value

6.18 ORIENT_CFG_G (13h).

Angular rate sensor sign and orientation register.

Table 57. ORIENT_CFG_G register

0(1)	0(1)	SignX_G	SignY_G	SignZ_G	Orient_2	Orient_1	Orient_0

1. These bits must be set to ‘0’ for the correct operation of the device

Table 58. ORIENT_CFG_G register description

SignX_G	Pitch axis (X) angular rate sign. Default value: 0 (0: positive sign; 1: negative sign)
SignY_G	Roll axis (Y) angular rate sign. Default value: 0 (0: positive sign; 1: negative sign)
SignZ_G	Yaw axis (Z) angular rate sign. Default value: 0 (0: positive sign; 1: negative sign)
Orient [2:0]	Directional user-orientation selection. Default value: 000

6.19 INT_GEN_SRC_G (14h)

Angular rate sensor interrupt source register.

Table 59. INT_GEN_SRC_G register

0	IA_G	ZH_G	ZL_G	YH_G	YL_G	XH_G	XL_G

Table 60. INT_GEN_SRC_G register description

IA_G	Interrupt active. Default value: 0 (0: no interrupt has been generated; 1: one or more interrupts have been generated)
ZH_G	Yaw (Z) high. Default value: 0 (0: no interrupt, 1: Z high event has occurred)
ZL_G	Yaw (Z) low. Default value: 0 (0: no interrupt; 1: Z low event has occurred)
YH_G	Roll (Y) high. Default value: 0 (0: no interrupt, 1: Y high event has occurred)
YL_G	Roll (Y) low. Default value: 0 (0: no interrupt, 1: Y low event has occurred)
XH_G	Pitch (X) high. Default value: 0 (0: no interrupt, 1: X high event has occurred)
XL_G	Pitch (X) low. Default value: 0 (0: no interrupt, 1: X low event has occurred)

6.20 OUT_TEMP_L (15h), OUT_TEMP_H (16h)

Temperature data output register. L and H registers together express a 16-bit word in two's complement right-justified.

Table 61. OUT_TEMP_L register

Temp7	Temp6	Temp5	Temp4	Temp3	Temp2	Temp1	Temp0

Table 62. OUT_TEMP_H register

Temp11	Temp11	Temp11	Temp11	Temp11	Temp10	Temp9	Temp8

Table 63. OUT_TEMP register description

Temp [11:0]	Temperature sensor output data. The value is expressed as two's complement sign extended on the MSB.

6.21 STATUS_REG (17h)

Status register.

Table 64. STATUS_REG register

0	IG_XL	IG_G	INACT	BOOT_ STATUS	TDA	GDA	XLDA

Table 65. STATUS_REG register description

IG_XL	Accelerometer interrupt output signal. Default value: 0 (0: no interrupt has been generated; 1: one or more interrupt events have been generated)
IG_G	Gyroscope interrupt output signal. Default value: 0 (0: no interrupt has been generated; 1: one or more interrupt events have been generated)
INACT	Inactivity interrupt output signal. Default value: 0 (0: no interrupt has been generated; 1: one or more interrupt events have been generated)
BOOT_ STATUS	Boot running flag signal. Default value: 0 (0: no boot running; 1: boot running)
TDA	Temperature sensor new data available. Default value: 0 (0: a new data is not yet available; 1: a new data is available)
GDA	Gyroscope new data available. Default value: 0 (0: a new set of data is not yet available; 1: a new set of data is available)
XLDA	Accelerometer new data available. Default value: 0 (0: a new set of data is not yet available; 1: a new set of data is available)

6.22 OUT_X_G (18h - 19h)

Angular rate sensor pitch axis (X) angular rate output register. The value is expressed as a 16-bit word in two's complement.

6.23 OUT_Y_G (1Ah - 1Bh)

Angular rate sensor roll axis (Y) angular rate output register. The value is expressed as a 16-bit word in two's complement.

6.24 OUT_Z_G (1Ch - 1Dh)

Angular rate sensor yaw axis (Z) angular rate output register. The value is expressed as a 16-bit word in two's complement.

6.25 CTRL_REG4 (1Eh)

Control register 4.

Table 66. CTRL_REG4 register

0(1)	0(1)	Zen_G	Yen_G	Xen_G	0(1)	LIR_XL1	4D_XL1

1. These bits must be set to '0' for the correct operation of the device

Table 67. CTRL_REG4 register description

Zen_G	Gyroscope's yaw axis (Z) output enable. Default value: 1 (0: Z-axis output disabled; 1: Z-axis output enabled)
Yen_G	Gyroscope's roll axis (Y) output enable. Default value: 1 (0: Y-axis output disabled; 1: Y-axis output enabled)
Xen_G	Gyroscope's pitch axis (X) output enable. Default value: 1 (0: X-axis output disabled; 1: X-axis output enabled)
LIR_XL1	Latched interrupt. Default value: 0 (0: interrupt request not latched; 1: interrupt request latched)
4D_XL1	4D option enabled on interrupt. Default value: 0 (0: interrupt generator uses 6D for position recognition; 1: interrupt generator uses 4D for position recognition)

6.26 CTRL_REG5_XL (1Fh)

Linear acceleration sensor control register 5.

Table 68. CTRL_REG5_XL register

DEC_1	DEC_0	Zen_XL	Yen_XL	Xen_XL	0(1)	0(1)	0(1)

1. These bits must be set to '0' for the correct operation of the device

Table 69. CTRL_REG5_XL register description

DEC_ [0:1]	Decimation of acceleration data on OUT REG and FIFO. Default value: 00 (00: no decimation; 01: update every 2 samples; 10: update every 4 samples; 11: update every 8 samples)
Zen_XL	Accelerometer's Z-axis output enable. Default value: 1 (0: Z-axis output disabled; 1: Z-axis output enabled)
Yen_XL	Accelerometer's Y-axis output enable. Default value: 1 (0: Y-axis output disabled; 1: Y-axis output enabled)
Xen_XL	Accelerometer's X-axis output enable. Default value: 1 (0: X-axis output disabled; 1: X-axis output enabled)

6.27 CTRL_REG6_XL (20h)

Linear acceleration sensor control register 6.

Table 70. CTRL_REG6_XL register

ODR_XL2	ODR_XL1	ODR_XL0	FS1_XL	FS0_XL	BW_SCAL_ODR	BW_XL1	BW_XL0

Table 71. CTRL_REG6_XL register description

ODR_XL [2:0]	Output data rate and Power Mode selection. Default value: 000 (see *Table 72*).
FS_XL [1:0]	Accelerometer full-scale selection. Default value: 00 (00: ±2*g*; 10: ±4*g*; 11: ±8*g*)
BW_SCAL_ODR	Bandwidth selection. Default value: 0 (0: bandwidth determined by ODR selection: - BW = 408 Hz when ODR = 952 Hz, 50 Hz, 10 Hz; - BW = 211 Hz when ODR = 476 Hz; - BW = 105 Hz when ODR = 238 Hz; - BW = 50 Hz when ODR = 119 Hz; 1: bandwidth selected according to BW_XL [2:1] selection)
BW_XL [1:0]	Anti-aliasing filter bandwidth selection. Default value: 00 (00: 408 Hz; 01: 211 Hz; 10: 105 Hz; 11: 50 Hz)

ODR_XL [2:0] is used to set power mode and ODR selection. *Table 72* summarizes all available frequencies when only the accelerometer is activated.

Table 72. ODR register setting (accelerometer only mode)

ODR_XL2	ODR_XL1	ODR_XL0	ODR selection [Hz]
0	0	0	Power-down
0	0	1	10 Hz
0	1	0	50 Hz
0	1	1	119 Hz
1	0	0	238 Hz
1	0	1	476 Hz
1	1	0	952 Hz
1	1	1	n.a.

6.28 CTRL_REG7_XL (21h)

Linear acceleration sensor control register 7.

Table 73. CTRL_REG7_XL register

HR	DCF1	DCF0	0(1)	0(1)	FDS	0(1)	HPIS1

1. These bits must be set to ‘0’ for the correct operation of the device

Table 74. CTRL_REG7_XL register description

HR	High resolution mode for accelerometer enable. Default value: 0 (0: disabled; 1: enabled). Refer to *Table 75*
DCF[1:0]	Accelerometer digital filter (high-pass and low-pass) cutoff frequency selection: the bandwidth of the high-pass filter depends on the selected ODR. Refer to *Table 75*
FDS	Filtered data selection. Default value: 0 (0: internal filter bypassed; 1: data from internal filter sent to output register and FIFO)
HPIS1	High-pass filter enabled for acceleration sensor interrupt function on Interrupt. Default value: 0 (0: filter bypassed; 1: filter enabled)

Table 75. Low-pass cutoff frequency in high resolution mode (HR = 1)

HR	CTRL_REG7 (DCF [1:0])	LP cutoff freq. [Hz]
1	00	ODR/50
1	01	ODR/100
1	10	ODR/9
1	11	ODR/400

6.29 CTRL_REG8 (22h)

Control register 8.

Table 76. CTRL_REG8 register

BOOT	BDU	H_LACTIVE	PP_OD	SIM	IF_ADD_INC	BLE	SW_RESET

Table 77. CTRL_REG8 register description

BOOT	Reboot memory content. Default value: 0 (0: normal mode; 1: reboot memory content(1))
BDU	Block Data Update. Default value: 0 (0: continuous update; 1: output registers not updated until MSB and LSB read
H_LACTIVE	Interrupt activation level. Default value: 0 (0: interrupt output pins active high; 1: interrupt output pins active low)
PP_OD	Push-pull/open-drain selection on INT1 and INT2 pin. Default value: 0. (0: push-pull mode; 1: open-drain mode)
SIM	SPI serial interface mode selection. Default value: 0 (0: 4-wire interface; 1: 3-wire interface)
IF_ADD_INC	Register address automatically incremented during a multiple byte access with a serial interface (I^2C or SPI). Default value: 1 (0: disabled; 1: enabled)
BLE	Big/Little Endian data selection. Default value 0 (0: data LSB @ lower address; 1: data MSB @ lower address)
SW_RESET	Software reset. Default value: 0 (0: normal mode; 1: reset device)

1. Boot request is executed as soon as the internal oscillator is turned on. It is possible to set the bit while in power-down mode, in this case it will be served at the next normal mode or sleep mode.

6.30 CTRL_REG9 (23h)

Control register 9.

Table 78. CTRL_REG9 register

0(1)	SLEEP_G	0(1)	FIFO_ TEMP_EN	DRDY_ mask_bit	I2C_disable	FIFO_EN	STOP_ON _FTH

1. These bits must be set to '0' for the correct operation of the device

Table 79. CTRL_REG9 register description

SLEEP_G	Gyroscope sleep mode enable. Default value: 0 (0: disabled; 1: enabled)
FIFO_TEMP_EN	Temperature data storing in FIFO enable. Default value: 0 (0: temperature data not stored in FIFO; 1: temperature data stored in FIFO)
DRDY_mask_bit	Data available enable bit. Default value: 0 (0: DA timer disabled; 1: DA timer enabled)
I2C_disable	Disable I^2C interface. Default value: 0 (0: both I^2C and SPI enabled; 1: I^2C disabled, SPI only)
FIFO_EN	FIFO memory enable. Default value: 0 (0: disabled; 1: enabled)
STOP_ON_FTH	Enable FIFO threshold level use. Default value: 0 (0: FIFO depth is not limited; 1: FIFO depth is limited to threshold level)

6.31 CTRL_REG10 (24h)

Control register 10.

Table 80. CTRL_REG10 register

0(1)	0(1)	0(1)	0(1)	0(1)	ST_G	0(1)	ST_XL

1. These bits must be set to '0' for the correct operation of the device

Table 81. CTRL_REG10 register description

ST_G	Angular rate sensor self-test enable. Default value: 0 (0: Self-test disabled; 1: Self-test enabled;)
ST_XL	Linear acceleration sensor self-test enable. Default value: 0 (0: Self-test disabled; 1: Self-test enabled;)

6.32 INT2_GEN_SRC_XL (25h)

Linear acceleration sensor interrupt 2 source register.

Table 82. INT2_GEN_SRC_XL register

0	IA2_XL	ZH2_XL	ZL2_XL	YH2_XL	YL2_XL	XH2_XL	XL2_XL

Table 83. INT2_GEN_SRC_XL register description

IA2_XL	Interrupt active. Default value: 0 (0: no interrupt has been generated; 1: one or more interrupts have been generated)
ZH2_XL	Accelerometer's Z high event. Default value: 0 (0: no interrupt, 1: Z high event has occurred)
ZL2_XL	Accelerometer's Z low event. Default value: 0 (0: no interrupt; 1: Z low event has occurred)
YH2_XL	Accelerometer's Y high event. Default value: 0 (0: no interrupt, 1: Y high event has occurred)
YL2_XL	Accelerometer's Y low event. Default value: 0 (0: no interrupt, 1: Y low event has occurred)
XH2_XL	Accelerometer's X high event. Default value: 0 (0: no interrupt, 1: X high event has occurred)
XL2_XL	Accelerometer's X low. event. Default value: 0 (0: no interrupt, 1: X low event has occurred)

6.33 INT1_GEN_SRC_XL (26h)

Linear acceleration sensor interrupt 1 source register.

Table 84. INT1_GEN_SRC_XL register

0	IA1_XL	ZH1_XL	ZL1_XL	YH1_XL	YL1_XL	XH1_XL	XL1_XL

Table 85. INT1_GEN_SRC_XL register description

IA1_XL	Interrupt active. Default value: 0 (0: no interrupt has been generated; 1: one or more interrupts have been generated)
ZH1_XL	Accelerometer's Z high event. Default value: 0 (0: no interrupt, 1: Z high event has occurred)
ZL1_XL	Accelerometer's Z low event. Default value: 0 (0: no interrupt; 1: Z low event has occurred)
YH1_XL	Accelerometer's Y high event. Default value: 0 (0: no interrupt, 1: Y high event has occurred)
YL1_XL	Accelerometer's Y low event. Default value: 0 (0: no interrupt, 1: Y low event has occurred)
XH1_XL	Accelerometer's X high event. Default value: 0 (0: no interrupt, 1: X high event has occurred)
XL1_XL	Accelerometer's X low. event. Default value: 0 (0: no interrupt, 1: X low event has occurred)

6.34 STATUS_REG (27h)

Status register.

Table 86. STATUS_REG register

0	IG_XL	IG_G	INACT	BOOT_ STATUS	TDA	GDA	XLDA

Table 87. STATUS_REG register description

IG_XL	Accelerometer interrupt output signal. Default value: 0 (0: no interrupt has been generated; 1: one or more interrupt events have been generated)
IG_G	Gyroscope interrupt output signal. Default value: 0 (0: no interrupt has been generated; 1: one or more interrupt events have been generated)
INACT	Inactivity interrupt output signal. Default value: 0. (0: no interrupt has been generated; 1: one or more interrupt events have been generated)
BOOT_ STATUS	Boot running flag signal. Default value: 0 (0: no boot running; 1: boot running)
TDA	Temperature sensor new data available. Default value: 0 (0: new data is not yet available; 1: new data is available)
GDA	Gyroscope new data available. Default value: 0 (0: a new set of data is not yet available; 1: a new set of data is available)
XLDA	Accelerometer new data available. Default value: 0 (0: a new set of data is not yet available; 1: a new set of data is available)

6.35 OUT_X_XL (28h - 29h)

Linear acceleration sensor X-axis output register. The value is expressed as a 16-bit word in two's complement.

6.36 OUT_Y_XL (2Ah - 2Bh)

Linear acceleration sensor Y-axis output register. The value is expressed as a 16-bit word in two's complement.

6.37 OUT_Z_XL (2Ch - 2Dh)

Linear acceleration sensor Z-axis output register. The value is expressed as a 16-bit word in two's complement.

6.38 FIFO_CTRL (2Eh)

FIFO control register.

Table 88. FIFO_CTRL register

FMODE2	FMODE1	FMODE0	FTH4	FTH3	FTH2	FTH1	FTH0

Table 89. FIFO_CTRL register description

FMODE [2:0]	FIFO mode selection bits. Default value: 000 For further details refer to *Table 90*.
FTH [4:0]	FIFO threshold level setting. Default value: 0 0000

Table 90. FIFO mode selection

FMODE2	FMODE1	FMODE0	Mode
0	0	0	Bypass mode. FIFO turned off
0	0	1	FIFO mode. Stop collecting data when FIFO is full.
0	1	0	Reserved
0	1	1	Continuous mode until trigger is deasserted, then FIFO mode.
1	0	0	Bypass mode until trigger is deasserted, then Continuous mode.
1	1	0	Continuous mode. If the FIFO is full, the new sample over-writes the older sample.

6.39 FIFO_SRC (2Fh)

FIFO status control register.

Table 91. FIFO_SRC register

FTH	OVRN	FSS5	FSS4	FSS3	FSS2	FSS1	FSS0

Table 92. FIFO_SRC register description

FTH	FIFO threshold status. (0: FIFO filling is lower than threshold level; 1: FIFO filling is equal or higher than the threshold level
OVRN	FIFO overrun status. (0: FIFO is not completely filled; 1: FIFO is completely filled and at least one sample has been overwritten) For further details refer to *Table 93*.
FSS [5:0]	Number of unread samples stored into FIFO. (000000: FIFO empty; 100000: FIFO full, 32 unread samples) For further details refer to *Table 93*.

Table 93. FIFO_SRC example: OVR/FSS details

FTH	OVRN	FSS5	FSS4	FSS3	FSS2	FSS1	FSS0	Description
0	0	0	0	0	0	0	0	FIFO empty
--(1)	0	0	0	0	0	0	1	1 unread sample
...								
--(1)	0	1	0	0	0	0	0	32 unread sample
1	1	1	0	0	0	0	0	At least one sample has been overwritten

1. When the number of unread samples in FIFO is greater than the threshold level set in register *FIFO_CTRL (2Eh)*, the FTH value is '1'.

6.40 INT_GEN_CFG_G (30h)

Angular rate sensor interrupt generator configuration register.

Table 94. INT_GEN_CFG_G register

AOI_G	LIR_G	ZHIE_G	ZLIE_G	YHIE_G	YLIE_G	XHIE_G	XLIE_G

Table 95. INT_GEN_CFG_G register description

AOI_G	AND/OR combination of gyroscope's interrupt events. Default value: 0 (0: OR combination; 1: AND combination)
LIR_G	Latch gyroscope interrupt request. Default value: 0 (0: interrupt request not latched; 1: interrupt request latched)
ZHIE_G	Enable interrupt generation on gyroscope's yaw (Z) axis high event. Default value: 0 (0: disable interrupt request; 1: interrupt request on measured angular rate value higher than preset threshold)
ZLIE_G	Enable interrupt generation on gyroscope's yaw (Z) axis low event. Default value: 0 (0: disable interrupt request; 1: interrupt request on measured angular rate value lower than preset threshold)
YHIE_G	Enable interrupt generation on gyroscope's roll (y) axis high event. Default value: 0 (0: disable interrupt request; 1: interrupt request on measured angular rate value higher than preset threshold)
YLIE_G	Enable interrupt generation on gyroscope's roll (y) axis low event. Default value: 0 (0: disable interrupt request; 1: interrupt request on measured angular rate value lower than preset threshold)
XHIE_G	Enable interrupt generation on gyroscope's pitch (X) axis high event. Default value: 0 (0: disable interrupt request; 1: interrupt request on measured angular rate value higher than preset threshold)
XLIE_G	Enable interrupt generation on gyroscope's pitch (X) axis low event. Default value: 0 (0: disable interrupt request; 1: interrupt request on measured angular rate value lower than preset threshold)

6.41 INT_GEN_THS_X_G (31h - 32h)

Angular rate sensor interrupt generator threshold registers. The value is expressed as a 15-bit word in two's complement.

Table 96. INT_GEN_THS_XH_G register

DCRM_G	THS_G_X14	THS_G_X13	THS_G_X12	THS_G_X11	THS_G_X10	THS_G_X9	THS_G_X8

Table 97. INT_GEN_THS_XL_G register

THS_G_X7	THS_G_X6	THS_G_X5	THS_G_X4	THS_G_X3	THS_G_X2	THS_G_X1	THS_G_X0

Table 98. INT_GEN_THS_X_G register description

DCRM_G	Decrement or reset counter mode selection. Default value: 0 (0: reset; 1: decrement, as per Counter behavior in *Figure 23* and *Figure 24*)
THS_G_X [14:0]	Angular rate sensor interrupt threshold on pitch (X) axis. Default value: 0000000 00000000

6.42 INT_GEN_THS_Y_G (33h - 34h)

Angular rate sensor interrupt generator threshold registers. The value is expressed as a 15-bit word in two's complement.

Table 99. INT_GEN_THS_YH_G register

0(1)	THS_G_Y14	THS_G_Y13	THS_G_Y12	THS_G_Y11	THS_G_Y10	THS_G_Y9	THS_G_Y8

1. This bit must be set to '0' for the correct operation of the device

Table 100. INT_GEN_THS_YL_G register

THS_G_Y7	THS_G_Y6	THS_G_Y5	THS_G_Y4	THS_G_Y3	THS_G_Y2	THS_G_Y1	THS_G_Y0

Table 101. INT_GEN_THS_Y_G register description

THS_G_Y [14:0]	Angular rate sensor interrupt threshold on roll (Y) axis. Default value: 0000000 00000000

6.43 INT_GEN_THS_Z_G (35h - 36h)

Angular rate sensor interrupt generator threshold registers. The value is expressed as a 15-bit word in two's complement.

Table 102. INT_GEN_THS_ZH_G register

0(1)	THS_G_Z14	THS_G_Z13	THS_G_Z12	THS_G_Z11	THS_G_Z10	THS_G_Z9	THS_G_Z8

1. This bit must be set to '0' for the correct operation of the device

Table 103. INT_GEN_THS_ZL_G register

THS_G_Z7	THS_G_Z6	THS_G_Z5	THS_G_Z4	THS_G_Z3	THS_G_Z2	THS_G_Z1	THS_G_Z0

Table 104. INT_GEN_THS_Z_G register description

THS_G_Z [14:0]	Angular rate sensor interrupt thresholds on yaw (Z) axis. Default value: 0000000 00000000

6.44 INT_GEN_DUR_G (37h)

Angular rate sensor interrupt generator duration register.

Table 105. INT_GEN_DUR_G register

WAIT_G	DUR_G6	DUR_G5	DUR_G4	DUR_G3	DUR_G2	DUR_G1	DUR_G0

Table 106. INT_GEN_DUR_G register description

WAIT_G	Exit interrupt wait function enable. Default value: 0 (0: wait function off; 1: wait for DUR_G [6:0] samples before exiting interrupt)
DUR_G [6:0]	Enter/exit interrupt duration value. Default value: 000 0000

The **DUR_G [6:0]** bits set the minimum duration of the interrupt event to be recognized. The duration steps and maximum values depend on the ODR chosen.

the WAIT_G bit has the following meaning:

- '0': the interrupt falls immediately if the signal crosses the selected threshold
- '1': if the signal crosses the selected threshold, the interrupt falls after a number of samples equal to the value of the duration counter register.

For further details refer to *Figure 23* and *Figure 24*.

Figure 23. Wait bit disabled

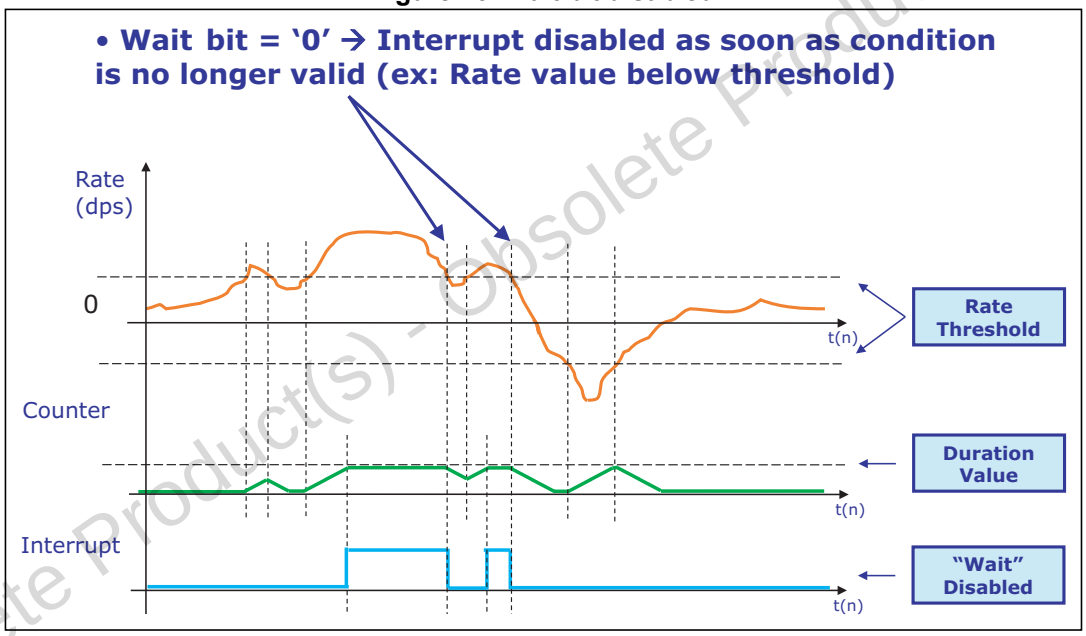
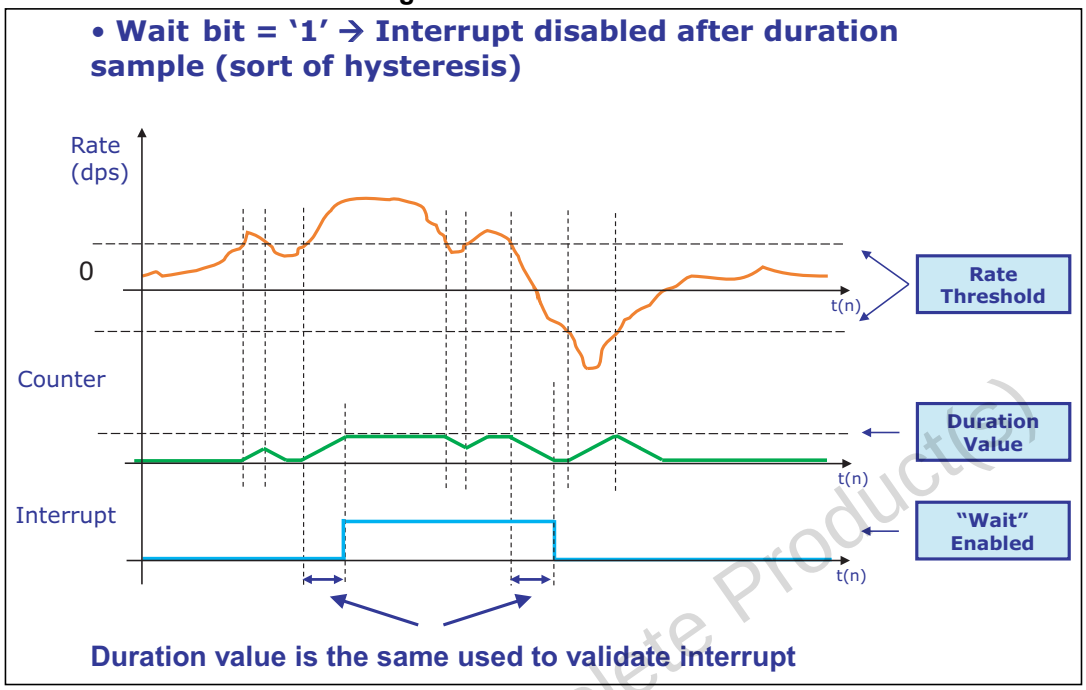


Figure 24. Wait bit enabled



6.45 EXTERNAL_SENSORS_DATA (80h-8Fh)

These registers (16 bytes) are used to store data read from the slave devices.

Table 107. EXTERNAL_SENSORS_DATA register

Data7	Data6	Data5	Data4	Data3	Data2	Data1	Data0

Table 108. EXTERNAL_SENSORS_DATA register description

Data [7:0]	Data read from the slave device.

6.46 MASTER_SYNC_REG (90h)

Synchronization of I^2C master register.

Table 109. MASTER_SYNC_REG register

FIFO_ write_trig	INT1_MST _DRDY	FREE_ RUNNING	MST_trig1	MST_trig0	write_ slave_sel1	write_ slave_sel0	AUX_pull_ up

Table 110. MASTER_SYNC_REG register description

FIFO_write_trig	When FIFO is enabled, this bit selects the synchronization strategy used to write data in FIFO. Default: 0 (0: synchronous with XL/GYRO; 1: synchronous with master)
INT1_MST_DRDY	When high data-ready signal of master is sent to INT1 pin. Default: 0 (0: disable; 1: enable) This setting works properly if the *INT1_CTRL (0Ch)* is set to 00h.
FREE_RUNNING	Master operates in continuous mode. Default: 0 (0: trigger is needed to start the operation specified in FSM_cmd[2:0] in the *MASTER_FSM_REG (91h)* register; 1: free running mode enable)
MST_trig[1:0]	Master trigger mode selection. Default: 0 This setting works properly if the FREE_RUNNING bit is set to '0'. (Refer to *Table 111*)
write_slave_sel[1:0]	Selected bits to apply write operation on desired slave. Default: 0 (Refer to *Table 112*)
AUX_pull_up	Auxiliary master-to-slave line pull-up enable. Default: 0 (0: internal pull-up disable; 1: internal pull-up enable)

Table 111. Master trigger mode configuration

MST_trig[1:0]	Description
00	Master is off and state machine (FSM) is steady
01	State machine (FSM) of the master is synchronous with the data-ready signal of XL/GYRO.
10	State machine (FSM) is synchronous with an external signal coming from TRIG_M pin.
11	Not used

Table 112. Slave address writing mode selection

write_slave_sel[1:0]	Description
00	Write operation is done on slave address *SLAVE0_I2C_ADD (B0h)*
01	Write operation is done on slave address *SLAVE1_I2C_ADD (B8h)*
10	Write operation is done on slave address *SLAVE2_I2C_ADD (BDh)*
11	Not used

6.47 MASTER_FSM_REG (91h)

Master FSM register.

Table 113. MASTER_FSM_REG register

MASTER_ ON	1(1)	PASS_ THROUGH	1(1)	1(1)	FSM_cmd2	FSM_cmd1	FSM_cmd0

1. These bits must be set to '1' for a proper functionality of the device.

Table 114. MASTER_FSM_REG register description

MASTER_ON	Enable master in sensor hub. Default: 0 (0: master disable; 1: master enable)
PASS_THROUGH	Enable pass-through mode. Default: 0 (0: pass-through mode disable; 1: pass-through mode enable: used to bypass the master of the sensor hub, connecting directly the main bus to the auxiliary bus.)
FSM_cmd[2:0]	Select type of operation to be performed by master state machine (FSM). Refer to *Table 115*

Table 115. Master state machine type of operation

FSM_cmd [2:0]	Description
000	Idle
010	Write
011	Read
100	Stop

6.48 MASTER_STATUS_REG (97h)

Master status register.

Table 116. MASTER _STATUS_REG register

0(1)	DATA_ READY_G	DATA_ READY_XL	DATA_ READY_ MASTER	ACK_ STATUS	I2C_BUS	ARB_ LOST	BYTE_ TRANSMISSION

1. These bits must be set to '0' for a proper functionality of the device.

Table 117. MASTER _STATUS_REG register description

DATA_READY_G	Data-ready signal of gyroscope. Default: 0 (0: data is not ready to be transmitted; 1: a new set of data is ready to be transmitted)
DATA_READY_XL	Data-ready signal of accelerometer. Default: 0 (0: data is not ready to be transmitted; 1: a new set of data is ready to be transmitted)
DATA_READY_MASTER	Last read completed flag. Default: 0 (0: read is not complete; 1: read is complete)
ACK_STATUS	Acknowledge signal during current transmission. Default: 0 (0: acknowledge found; 1: acknowledge not found)
I2C_BUS	I^2C auxiliary bus status. Default: 0 (0: I^2C stop sequence has been detected; 1: I^2C start sequence has been detected)
ARB_LOST	Arbitration status of auxiliary bus. Default: 0 (0: master is communicating on the bus; 1: arbitration is lost)
BYTE_TRANSMISSION	Transmission status. Default: 0 (0: transmission is running; 1: transmission of an entire byte is complete)

6.49 SLAVE0_I2C_ADD (B0h)

I^2C slave address of Slave 0 register.

Table 118. SLAVE0_I2C_ADD register

Slave0_ I2C_add6	Slave0_ I2C_add5	Slave0_ I2C_add4	Slave0_ I2C_add3	Slave0_ I2C_add2	Slave0_ I2C_add1	Slave0_ I2C_add0	0(1)

1. These bits must be set to '0' for a proper functionality of the device.

Table 119. SLAVE0_I2C_ADD register description

Slave0_I2C_add[6:0]	I^2C slave address of Slave 0.

6.50 SLAVE0_SUB_ADD (B1h)

Sub slave address of Slave 0 register.

Table 120. SLAVE0_SUB_ADD register

Slave0_ sub_add7	Slave0_ sub_add6	Slave0_ sub_add5	Slave0_ sub_add4	Slave0_ sub_add3	Slave0_ sub_add2	Slave0_ sub_add1	Slave0_ sub_add0

Table 121. SLAVE0_SUB_ADD register description

Slave0_sub_add[7:0]	Register address for Slave 0 device. Register address of the first location to be read or written by the master (select proper operation with FSM_cmd[2:0] bits in the *MASTER_FSM_REG (91h)* register.

6.51 SLAVE0_DATA_TO_WRITE (B5h)

Slave 0 data to write register.

Table 122. SLAVE0_DATA_TO_WRITE register

Slave0_ DataW7	Slave0_ DataW6	Slave0_ DataW5	Slave0_ DataW4	Slave0_ DataW3	Slave0_ DataW2	Slave0_ DataW1	Slave0_ DataW0

Table 123. SLAVE0_DATA_TO_WRITE register description

Slave0_DataW[7:0]	Data byte to be written into Slave 0 at address specified in *SLAVE0_SUB_ADD (B1h)*.

6.52 SLAVE0_CONFIG (B6h)

Slave 0 configuration register.

Table 124. SLAVE0_CONFIG register

Slave0_ polling_read	Swap_even _odd	Start_restart	Slave0_ rate4	Slave0_ rate3	Slave0_ rate2	Slave0_ rate1	Slave0_ rate0

Table 125. SLAVE0_CONFIG register description

Slave0_polling_read	Start of polling routine for Slave 0 device. Default: 0 Read continuously Slave0, polling the register addressed by the bits specified in the *SLAVE0_SUB_ADD (B1h)* register. If the content is different from 00h, it starts a burst read from the next address and performs a number of reads equal to the value specified in the Slave0_numop[3:0] bits in the *SLAVE0_BYTE_TO_READ (B7h)* register. (0: disable polling routine; 1: enable polling routine)
Swap_even_odd	Exchange storage order of two bytes. Default: 0 (0: disable swap; 1: enable swap)
Start_restart	Transition during a read operation between slaves. Default: 0 (0: I^2C stop and start operation, the bus is free during the transition; 1: I^2C restart operation, the bus is always busy).
Slave0_rate[4:0]	Decimation of data storage frequency. If the values are different from '0000', the master uses the first trigger (XL/GYRO data-ready or the signal from TRIG_M) to perform the read operation and then jumps the number of triggers specified in these bits before the next read operation.

6.53 SLAVE0_BYTE_TO_READ (B7h)

Slave 0 bytes to read register.

Table 126. SLAVE0_BYTE_TO_READ register

Slave0_on	0(1)	0(1)	0(1)	Slave0_numop3	Slave0_numop2	Slave0_numop1	Slave0_numop0

1. These bits must be set to '0' for a proper functionality of the device.

Table 127. SLAVE0_BYTE_TO_READ register description

Slave0_on	Enable Slave 0 auxiliary communication channel. Default: 0 Use the Slave0_numop[3:0] bits in order to correctly map the slave device registers. (0: Slave 0 not used; 1: Slave 0 used)
Slave0_numop[3:0]	Number of bytes read during the read sequence. Reads are performed on Slave 0 starting from the address specified in the *SLAVE0_SUB_ADD (B1h)* register.

6.54 SLAVE1_I2C_ADD (B8h)

I^2C slave address of slave 1 register.

Table 128. SLAVE1_I2C_ADD register

Slave1_I2C_add6	Slave1_I2C_add5	Slave1_I2C_add4	Slave1_I2C_add3	Slave1_I2C_add2	Slave1_I2C_add1	Slave1_I2C_add0	0(1)

1. These bits must be set to '0' for proper functionality of the device.

Table 129. SLAVE1_I2C_ADD register description

Slave1_I2C_add[6:0]	I^2C slave address of Slave 1.

6.55 SLAVE1_SUB_ADD (B9h)

Sub-slave address of Slave 1 register.

Table 130. SLAVE1_SUB_ADD register

Slave1_sub_add7	Slave1_sub_add6	Slave1_sub_add5	Slave1_sub_add4	Slave1_sub_add3	Slave1_sub_add2	Slave1_sub_add1	Slave1_sub_add0

Table 131. SLAVE1_SUB_ADD register description

Slave1_sub_add[7:0]	Register address for Slave 1 device. Register address of the first location to be read or written by the master (select proper operation with FSM_cmd[2:0] bits in the *MASTER_FSM_REG (91h)* register.

6.56 SLAVE1_DATA_TO_WRITE (BAh)

Slave 1 data to write register.

Table 132. SLAVE1_DATA_TO_WRITE register

Slave1_ DataW7	Slave1_ DataW6	Slave1_ DataW5	Slave1_ DataW4	Slave1_ DataW3	Slave1_ DataW2	Slave1_ DataW1	Slave1_ DataW0

Table 133. SLAVE1_DATA_TO_WRITE register description

Slave1_DataW[7:0]	Data byte to be written into Slave 1 at address specified in the *SLAVE1_SUB-_ADD (B9h)* register.

6.57 SLAVE1_CONFIG (BBh)

Slave 1 configuration register.

Table 134. SLAVE1_CONFIG register

Slave1_ polling_read	Swap_ even_odd	0	Slave1_ rate4	Slave1_ rate3	Slave1_ rate2	Slave1_ rate1	Slave1_ rate0

Table 135. SLAVE1_CONFIG register description

Slave1_polling_read	Start of polling routine for Slave 1 device. Default: 0 Read continuously Slave1 polling the register addressed by the bits specified in the *SLAVE1_SUB_ADD (B9h)* register. If the content is different from 00h, it starts a burst read from the next address and performs a number of reads equal to the value specified in the Slave1_numop[3:0] bits in the *SLAVE1_BYTE_TO_READ (BCh)* register. (0: disable polling routine; 1: enable polling routine)
Swap_even_odd	Exchange storage order of two bytes. Default: 0 (0: disable swap; 1: enable swap)
Slave1_rate[4:0]	Decimation of data storage frequency. If values are different from '0000', the master uses the first trigger (XL/GYRO data-ready or the signal from TRIG_M) to perform the read operation and then jumps the number of triggers specified in these bits before the next read operation.

6.58 SLAVE1_BYTE_TO_READ (BCh)

Slave 1 bytes to read register.

Table 136. SLAVE1_BYTE_TO_READ register

Slave1_on	0(1)	0(1)	0(1)	Slave1_ numop3	Slave1_ numop2	Slave1_ numop1	Slave1_ numop0

1. These bits must be set to '0' for a proper functionality of the device.

Table 137. SLAVE1_BYTE_TO_READ register description

Slave1_on	Enable Slave 1 auxiliary communication channel. Default: 0 Use the Slave1_numop[3:0] bits in order to correctly map the slave device registers. (0: Salve 1 not used; 1: Slave 1 used)
Slave1_numop[3:0]	Number of bytes read during the read sequence. Reads are performed on slave 1 starting from the address specified in the *SLAVE1_SUB_ADD (B9h)* register.

6.59 SLAVE2_I2C_ADD (BDh)

I^2C slave address of slave 2 register.

Table 138. SLAVE2_I2C_ADD register

Slave2_ I2C_add6	Slave2_ I2C_add5	Slave2_ I2C_add4	Slave2_ I2C_add3	Slave2_ I2C_add2	Slave2_ I2C_add1	Slave2_ I2C_add0	0(1)

1. These bits must be set to '0' for proper functionality of the device.

Table 139. SLAVE2_I2C_ADD register description

Slave2_I2C_add[6:0]	I^2C slave address of slave 2.

6.60 SLAVE2_SUB_ADD (BEh)

Sub-slave address of slave 2 register.

Table 140. SLAVE2_SUB_ADD register

Slave2_ sub_add7	Slave2_ sub_add6	Slave2_ sub_add5	Slave2_ sub_add4	Slave2_ sub_add3	Slave2_ sub_add2	Slave2_ sub_add1	Slave2_ sub_add0

Table 141. SLAVE2_SUB_ADD register description

Slave2_sub_add[7:0]	Register address for slave 2 device. Register address of the first location to be read or written by the master (select proper operation with FSM_cmd[2:0] bits in the *MASTER_FSM_REG (91h)* register.

6.61 SLAVE2_DATA_TO_WRITE (BFh)

Slave 2 data to write register.

Table 142. SLAVE2_DATA_TO_WRITE register

Slave2_ DataW7	Slave2_ DataW6	Slave2_ DataW5	Slave2_ DataW4	Slave2_ DataW3	Slave2_ DataW2	Slave2_ DataW1	Slave2_ DataW0

Table 143. SLAVE2_DATA_TO_WRITE register description

Slave2_DataW[7:0]	Data byte to be written into Slave 2 at address specified in the *SLAVE2_SUB_ADD (BEh)* register.

6.62 SLAVE2_CONFIG (C0h)

Slave 2 configuration register.

Table 144. SLAVE2_CONFIG register

Slave2_ polling_read	Swap_ even_odd	0	Slave2_ rate4	Slave2_ rate3	Slave2_ rate2	Slave2_ rate1	Slave2_ rate0

Table 145. SLAVE2_CONFIG register description

Slave2_polling_read	Start of polling routine for slave 2 device. Default: 0 Read continuously Slave2 polling the register addressed by the bits specified in the *SLAVE2_SUB_ADD (BEh)* register. If the content is different from 00h, it starts a burst read from the next address and performs a number of reads equal to the value specified in the Slave2_numop[3:0] bits in the *SLAVE2_BYTE_TO_READ (C1h)* register. (0: disable polling routine; 1: enable polling routine)
Swap_even_odd	Exchange storage order of two bytes. Default: 0 (0: disable swap; 1: enable swap)
Slave2_rate[4:0]	Decimation of data storage frequency. If values are different from ‘0000’, the master uses the first trigger (XL/GYRO data-ready or the signal from TRIG_M) to perform the read operation and then jumps the number of triggers specified in these bits before the next read operation.

6.63 SLAVE2_BYTE_TO_READ (C1h)

Slave 2 bytes to read register.

Table 146. SLAVE2_BYTE_TO_READ register

Slave2_on	0(1)	0(1)	0(1)	Slave2_ numop3	Slave2_ numop2	Slave2_ numop1	Slave2_ numop0

1. These bits must be set to '0' for a proper functionality of the device.

Table 147. SLAVE2_BYTE_TO_READ register description

Slave2_on	Enable Slave 2 auxiliary communication channel. Default: 0 Use the Slave2_numop[3:0] bits in order to correctly map the slave device registers. (0: Slave 2 not used; 1: Slave 2 used)
Slave2_numop[3:0]	Number of bytes read during the read sequence. Reads are performed on Slave 2 starting from the address specified in the *SLAVE2_SUB_ADD (BEh)* register.

6.64 MAGNETOMETER_ROUTINES (C2h)

Routines for magnetometer register.

Table 148. MAGNETOMETER_ROUTINES register

LIS3MD_ ODR	LIS3MD_ wakeup	LIS3MDL_ ODR	LIS3MDL_ wakeup	0(1)	0(1)	0(1)	0(1)

1. These bits must be set to '0' for proper functionality of the device.

Table 149. MAGNETOMETER_ROUTINES register description

LIS3MD_ODR	Enables automatic routine for ST's LIS3MD device. Default: 0 This routine activates the device in continuous mode at 100 Hz, the master's read of the output registers is synchronous with the data-ready signal from the device. (0: disable routine; 1: enable routine)
LIS3MD_wakeup	Enable automatic routine for ST's LIS3MD device. Default: 0 This routine is composed of a write synchronous with the XL/GYRO data-ready and by a read operation synchronous with the signal from TRIG_M (data-ready of the device) (0: disable routine; 1: enable routine)

LIS3MDL_ODR	Enable automatic routine for ST's LIS3MDL device. Default: 0 This routine activates the device in continuous mode at 80 Hz, the master's read of the output registers is synchronous with the data-ready signal from the device. (0: disable routine; 1: enable routine)
LIS3MDL_wakeup	Enable automatic routine for ST's LIS3MDL device. Default: 0 This routine is composed of a write synchronous with the XL/GYRO data-ready and by a read operation synchronous with the signal from TRIG_M (data-ready of the device) (0: disable routine; 1: enable routine)

6.65 GYRO_OFS_XY_ON_OUT (C9h)

Table 150. GYRO_OFS_XY_ON_OUT register

0(1)	Offset_ Enable	1(2)	0(1)	0(1)	0(1)	1(2)	0(1)

1. These bits must be set to '0' for proper functionality of the device.
2. These bits must be set to '1' for proper functionality of the device.

Table 151. GYRO_OFS_XY_ON_OUT register description

Offset_Enable	Define the values of the gyroscope to be stored in the pitch output registers *GYRO_OFS_PITCH_DATA_L/GYRO_OFS_PITCH_DATA_H (D0h, D1h)* and roll output registers *GYRO_OFS_ROLL_DATA_L/GYRO_OFS_ROLL_-DATA_H (D2h, D3h)*. Default: 0 (Refer to *Table 152*)

Table 152. Offset_Enable description

Offset_Enable	Description
0	*GYRO_OFS_PITCH_DATA_L/GYRO_OFS_PITCH_DATA_H (D0h, D1h)* registers contain the gyro output data for the pitch axis; *GYRO_OFS_ROLL_-DATA_L/GYRO_OFS_ROLL_DATA_H (D2h, D3h)* registers contain the gyro output data for the roll axis
1	*GYRO_OFS_PITCH_DATA_L/GYRO_OFS_PITCH_DATA_H (D0h, D1h)* registers contain the offset value for the pitch axis calculated with the Kalmann filter and used to correct the gyro output data (*OUT_X_G (18h - 19h)* registers); *GYRO_OFS_ROLL_DATA_L/GYRO_OFS_ROLL_DATA_H (D2h, D3h)* registers contain the offset value for the roll axis calculated with the Kalmann filter and used to correct the gyro output data (*OUT_Y_G (1Ah - 1Bh)*)

6.66 MAG_CFG (CAh)

Magnetometer configuration axes register.

Table 153. MAG_CFG register

FUNCTIONS_EN	0(1)	Mag_SwapXY	MagX_sign	MagY_sign	MagZ_sign	PR_sel_out	0(1)

1. These bits must be set to '0' for proper functionality of the device.

Table 154. MAG_CFG register description

FUNCTIONS_EN	Enable for pitch/roll/heading computation blocks. Default: 0 (0: disable; 1: enable)
Mag_SwapXY	Swap XY magnetic axes for compass/heading computation. Default: 0 (0: disable swap; 1: enable swap)
MagX_sign	Inversion of X magnetic axis for compass/heading. The inversion is done after XY swap. Default: 0 (0: disable inversion; 1: enable inversion)
MagY_sign	Inversion of Y magnetic axis for compass/heading. The inversion is done after XY swap. Default: 0 (0: disable inversion; 1: enable inversion)
MagZ_sign	Inversion of Z magnetic axis for compass/heading. Default: 0 (0: disable inversion; 1: enable inversion
PR_sel_out	Send to registers *PITCH_ANGLE_L/PITCH_ANGLE_H (CCh, CDh)* and *ROLL_ANGLE_L/ROLL_ANGLE_H (CEh, CFh)* the filtered pitch/roll angles obtained by the Kalmann filter or by XL data. Default: 0 (0: pitch/roll angles from accelerometer; 1: pitch/roll angles filtered from the Kalmann filter)

6.67 PITCH_ANGLE_L/PITCH_ANGLE_H (CCh, CDh)

Output register of pitch angle obtained from tilt computation.

Output values are based on the PR_sel_out bit configuration in *MAG_CFG (CAh)*. If PR_sel_out is set to '0', the value is expressed in 16-bit signed, wraparound. If PR_sel_out is set to '1', the angle value is expressed in a 16-bit word in two's complement with the same sensitivity of the gyroscope output data.

6.68 ROLL_ANGLE_L/ROLL_ANGLE_H (CEh, CFh)

Output register of roll angle obtained from tilt computation.

Output values are based on the PR_sel_out bit configuration in *MAG_CFG (CAh)*. If PR_sel_out is set to '0', the value is expressed in 16-bit signed, wraparound. If PR_sel_out is set to '1', the angle value is expressed in a 16-bit word in two's complement with the same sensitivity of the gyroscope output data.

6.69 GYRO_OFS_PITCH_DATA_L/GYRO_OFS_PITCH_DATA_H (D0h, D1h)

Output register of offset correction block of pitch angle. The value is expressed as a 16-bit word in two's complement.

Output values are based on the Offset_Enable bit configuration in *GYRO_OFS_XY_ON_OUT (C9h)*

6.70 GYRO_OFS_ROLL_DATA_L/GYRO_OFS_ROLL_DATA_H (D2h, D3h)

Output register of offset correction block of roll angle. The value is expressed as a 16-bit word in two's complement.

Output values are based on the Offset_Enable bit configuration in *GYRO_OFS_XY_ON_OUT (C9h)*

6.71 HEADING_DATA_L/HEADING_DATA_H (D4h, D5h)

Output register of azimuth obtained from heading calculation block. The value is 10-bit unsigned right-aligned, wraparound.

7 Soldering information

The LGA package is compliant with the ECOPACK®, RoHS and “Green” standard.
It is qualified for soldering heat resistance according to JEDEC J-STD-020.

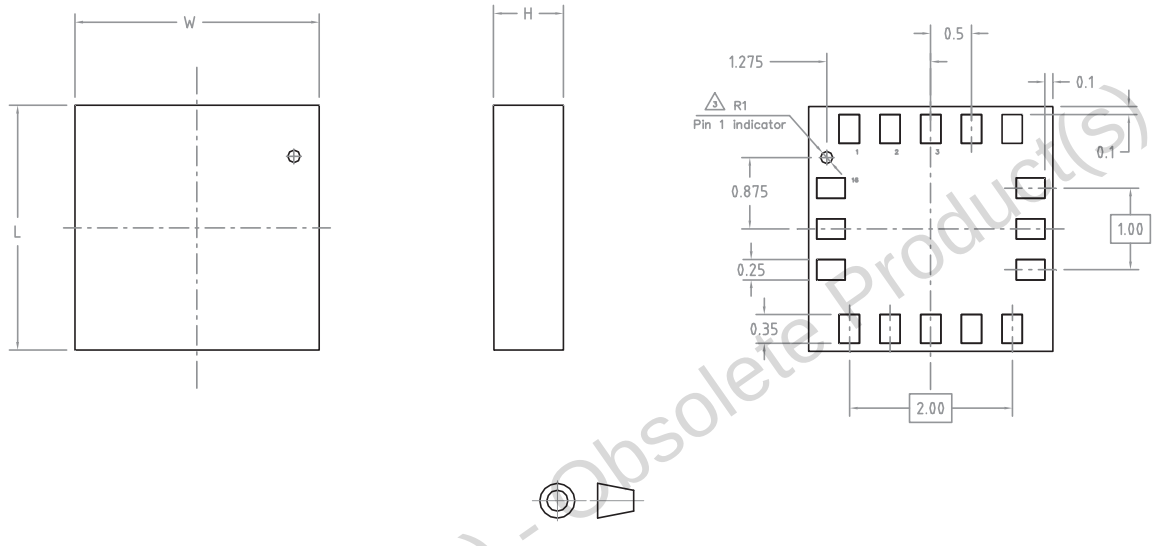
Leave “Pin 1 Indicator” unconnected during soldering.

Land pattern and soldering recommendations are available at www.st.com/mems.

8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Figure 25. LGA 3x3x0.86 16L package outline and dimensions



Dimensions are in millimeter unless otherwise specified
General Tolerance is +/-0.1mm unless otherwise specified

OUTER DIMENSIONS

ITEM	DIMENSION [mm]	TOLERANCE [mm]
Length [L]	3.00	±0.1
Width [W]	3.00	±0.1
Height [H]	0.86	MAX

9 Revision history

Table 155. Document revision history

Date	Revision	Changes
28-Nov-2013	1	Initial release
31-Mar-2014	2	Updated Vdd to 2.2 V in *Section 2: Module specifications* Added *Section 6.32: INT2_GEN_SRC_XL (25h)* Updated *Section 6.33: INT1_GEN_SRC_XL (26h)* and *Table 20: Register mapping* Updated *Section 6.57: SLAVE1_CONFIG (BBh)* and *Section 6.62: SLAVE2_CONFIG (C0h)* Updated *Table 49: CTRL_REG1_G register description* and *Table 71: CTRL_REG6_XL register description* Updated SW_RESET bit in *Table 77: CTRL_REG8 register description* Updated dimensions and revised package presentation in *Section 8: Package information*
03-Nov-2014	3	Updated footnote *2* of *Table 2: Pin description*

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