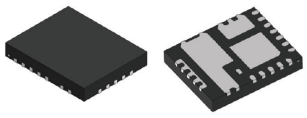
PM7050A

Datasheet

50 A Smart power stage with current sensing and temperature monitor



QFN 4x5 26L

Product status link
PM7050A

Product summary	
Order code	PM7050ATR
Temperature range	-40 to +125
Package	QFN 4x5 26L
Packing	Tape & Reel

Features

- Input range: 4.5 V to 18 V
- Supports 50 A DC current
- Compatible with 3.3 V tri-state PWM
- Down slope current sensing
- ± 3 % accuracy current monitor (IMON) with REF_{IN} input
- 8 mV /°C temperature monitor with OT flag
- Dedicated low-side FET control input
- Fault protection:
  - High-side FET short and overcurrent protection
  - Overtemperature protection
  - V_{CC} and V_{IN} undervoltage lockout (UVLO)
- Open drain fault reporting output
- Up to 2 MHz switching frequency

Applications

- High frequency and high efficiency VRM and VRD.
- Core, graphic, and memory regulators for microprocessors
- High density VR for server, networking, and cloud computing
- POL DC/DC converters and video gaming consoles

Description

The PM7050A is a smart device that integrates a high-side and low-side MOSFET, and a high performance driver with integrated bootstrap FET. The PM7050A offers high accuracy current and temperature monitors that can be provided to the controller of a multiphase DC/DC system. They simplify design and increase performance by eliminating the DCR sensing network and associated thermal compensation. An industry leading, thermally enhanced, 4 x 5 mm package allows minimal overall PCB real estate and low profile construction.

The device features a 3.3 V compatible tri-state PWM input that, together with multiphase controllers, provides a robust solution in the event of abnormal operating conditions. The PM7050A also integrates UVLO monitoring and fault protections such as overtemperature, overcurrent and HS MOSFET short failures.

1 Pins description

Figure 1. **Pinout (top view)**

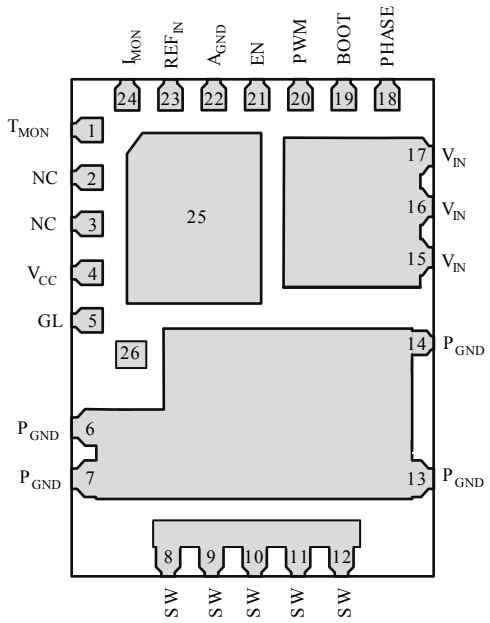


Table 1. Pins description

Pin#	Name	Function
1	TMON	Temperature monitor output. For multiphase, the TMON pins can be connected together as a common bus; the highest voltage (representing the highest temperature) is sent to the PWM controller. TMON is pulled high (to 2.5 V) to indicate an overtemperature fault. No more than 250 pF total capacitance can be directly connected across TMON and GND pins; with a series resistor, a higher capacitance load is allowed, such as 1 kΩ for 100 nF load.
2, 3	NC	Not internally connected. Leave this pin floating.
4	V_{CC}	+5 V logic and gate drive bias supply. Place a high quality low ESR ceramic capacitor (~1 µF/X7R) in close proximity from this pin to A_{GND}.
5, 26	GL	No connect (this is a low-side gate driver output (GL), optional to monitor for system debugging).
6, 7, 13, 14	P_{GND}	Power ground (source connection of low-side MOSFET).
8, 9, 10, 11, 12	SW	Switching junction node between HFET source and LFET drain. Connect directly to output inductor.
15, 16, 17	V_{IN}	Input of power stage (to drain of high-side MOSFET). Place at least 2 ceramic capacitors (10 µF or higher, X5R or X7R) in close proximity across V_{IN} and P_{GND}. For optimal performance, place as many vias as possible in the bottom side V_{IN} paddle.
18	PHASE	Return of boot capacitor. Internally connected to SW node so no external routing required for SW connection.
19	BOOT	Floating bootstrap supply pin for the upper gate drive. Place a high quality low ESR ceramic capacitor (0.1 µF/X7R to 0.22 µF/X7R) in close proximity across BOOT and PHASE pins.
20	PWM	PWM input of gate driver, compatible with 3.3 V and 5 V tri-state PWM signal.
21	EN	Active high to enable driver.
22, 25	A_{GND}	A_{GND} of driver IC.
23	REF_{IN}	Input for external reference voltage for IMON signal. This voltage should be between 0.8 V and 1.6 V. Connect REF_{IN} to the appropriate current sense input of the controller. Place a high quality low ESR ceramic capacitor (~ 0.1 µF) in close proximity from this pin to A_{GND}.
24	IMON	Current monitor output, referenced to REF_{IN}. IMON is pulled high (to REF_{IN} +1.2 V) to indicate a high-side MOSFET shorted or overcurrent fault. Connect the IMON output to the appropriate current sense input of the controller. No more than 56 pF capacitance can be directly connected across IMON and REF_{IN} pins. With a 100 Ω series resistor, up to 470 pF may be used.

2 Typical application circuit and block diagram

2.1 Block diagram

Figure 2. **Typical application block diagram**

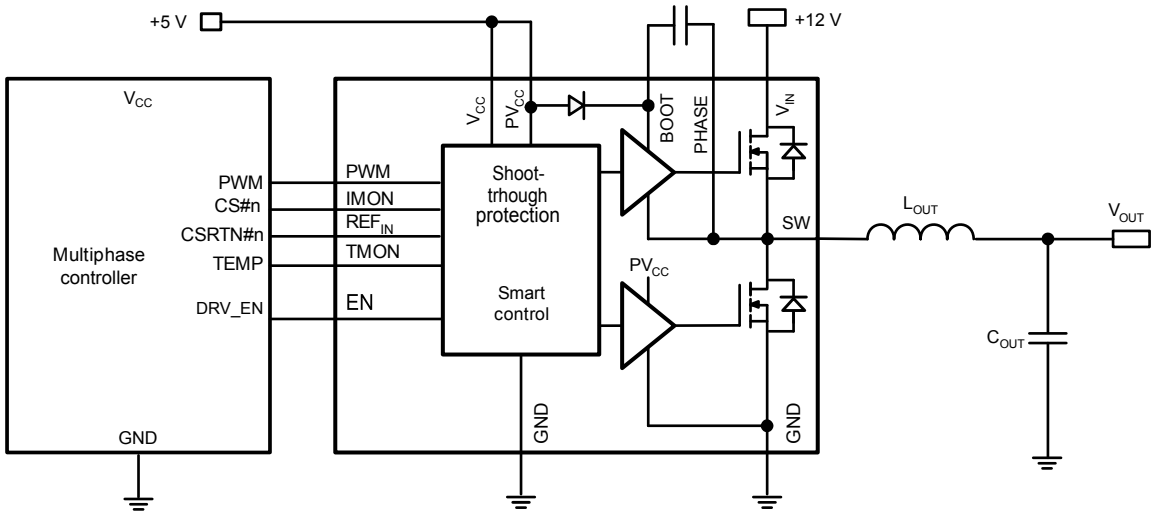
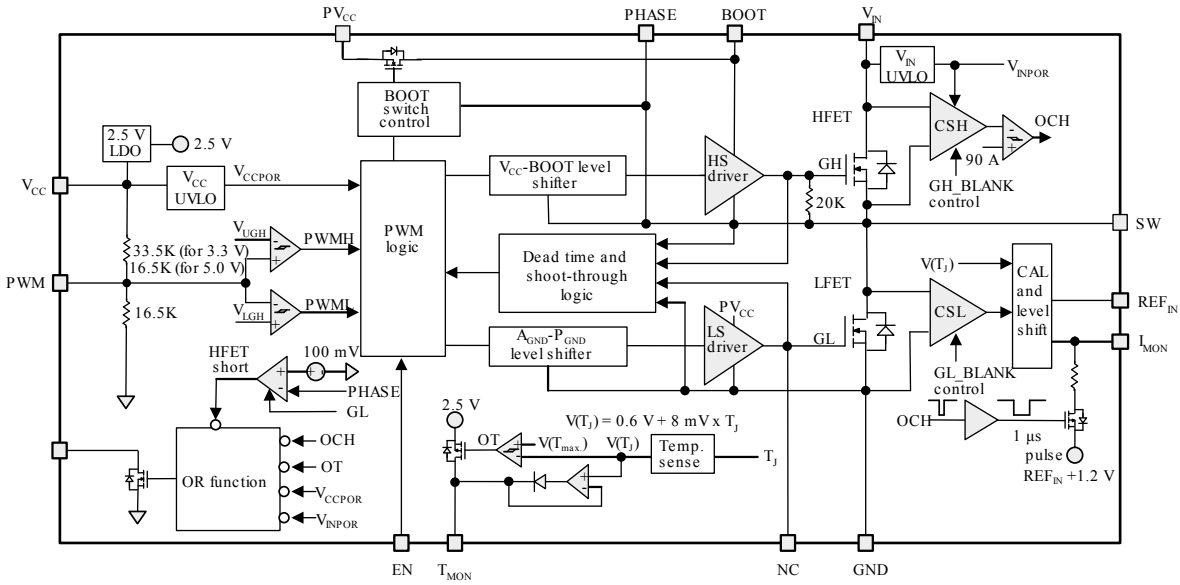


Figure 3. **Functional block diagram**



2.2 Application circuit

Figure 4. **Typical application circuit 1**

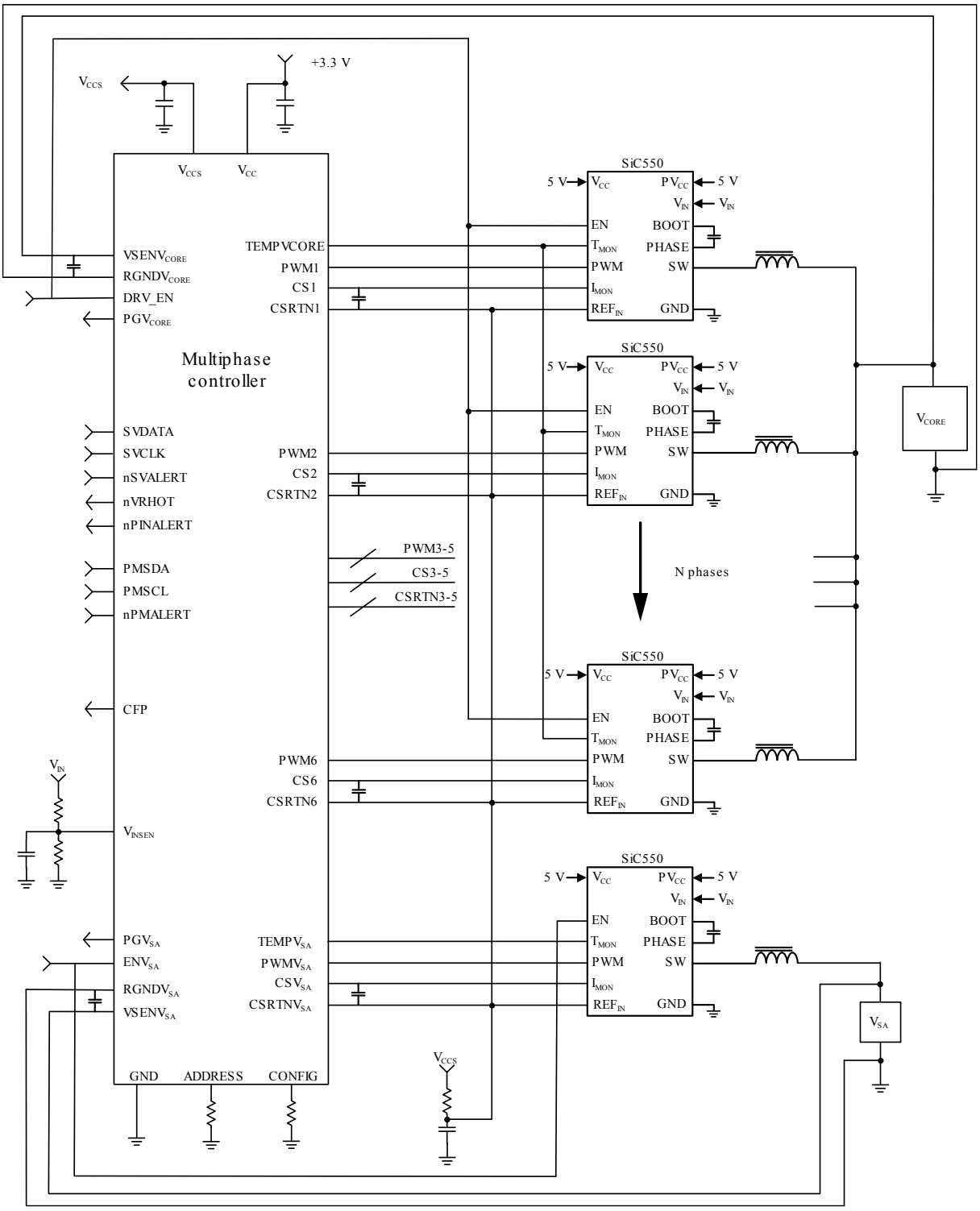
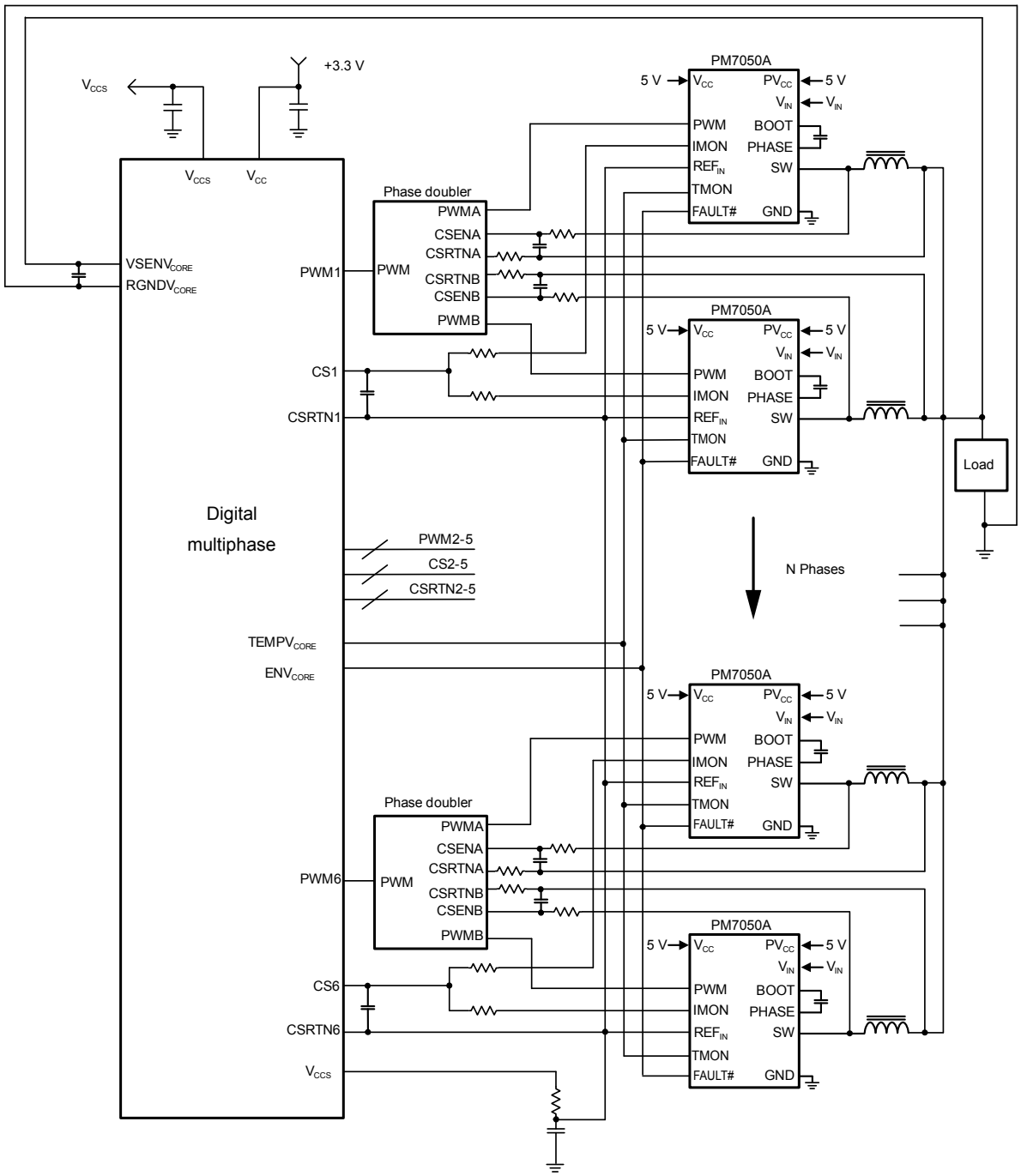


Figure 5. **Typical application circuit 2**



3 Absolute maximum ratings

Table 2. Absolute maximum ratings

Electrical parameter	Symbol	Conditons	Limit	Unit
Supply voltage	V_{CC}		-0.3 to +6	V
Input supply voltage	V_{IN}		-0.3 to +25	
PHASE, SW voltage	V_{PH-GND},V_{SW-GND}	GND - 10 V, < 20 ns pulse width, 10 µJ	-0.3 to +25	
BOOT voltage	V_{BOOT_GND}		-0.3 to +36	
Other I/O pin voltage			-0.3 to V_{CC} +0.3	
Maximum junction temperature (plastic package)			150	°C
Maximum storage temperature range			-65 to +150	
Lead (Pb)-free reflow profile			-	-

Electrical parameter	Min.	Typ.	Max.	Unit
Operating junction temperature range	-40	-	125	°C
Supply voltage (V_{CC}, PV_{CC})	-	5 ±5 %	-	V
Input supply voltage (V_{IN})	4.5	-	18	

Thermal resistance	θ_{JA}(°C/W)	θ_{JC}(°C/W)
PowerPAK MLP24-45L (1) (2) (3)	10.7	1.6

1. *θ_{JA} is measured in free air with the component mounted on a highly effective thermal conductivity test board with direct attach features.*
2. *For θ_{JC}, the case temperature location is the center of the exposed metal pad on the package underside.*
3. *These ratings vary with PCB layout and operating condition, and limited by device temperature and thermal shutdown trip point.*

4 Electrical characteristics

(Recommended operating conditions, unless otherwise noted. TJ = TA = -40 to 125 °C)

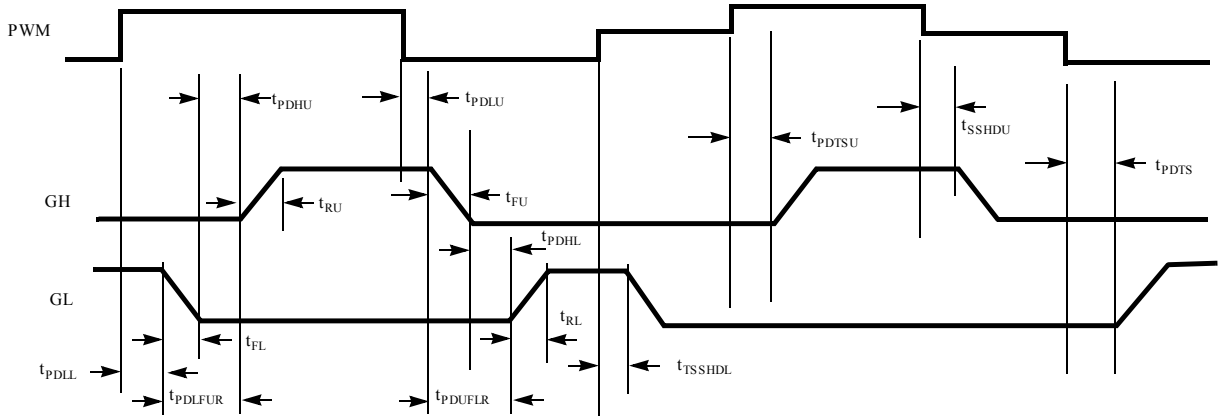
Table 3. Electrical specifications

Parameter	Symbol	Test conditions	Min.(1)	Typ.	Max.(1)	Unit
Power rating						
Maximum instant power dissipation		T_A = 25 °C, 150 A (2)	-	100	-	W
Maximum continuous power dissipation		T_A = 25 °C, θ_{JA} = 10 °C/W, T_J = 150 °C (2)	-	12.5	-	
Thermal resistance						
Thermal resistance junction to PCB	θ_{JB}	(2)	-	5.2	-	°C/W
Thermal resistance junction to ambient	θ_{JA}	0 LFM(2)	-	10.7	-	
		400 LFM (2)	-	9.3	-	
V_{CC} supply current						
Logic standby current	IV_{CC}	PWM = open	-	4.75	-	mA
Gate drive standby current	IPV_{CC}	PWM = open	-	100	-	µA
Logic operational current	IV_{CC}	PWM = 300 kHz	-	4.75	-	mA
Gate drive operational current	IPV_{CC}	PWM = 300 kHz	-	15	-	
Power-on reset and enable						
V_{CC} rising POR threshold			-	3.86	4.20(3)	V
V_{CC} falling POR threshold			3.20(3)	3.58	-	
V_{CC} POR hysteresis			-	280	-	mV
V_{CC} POR delay to operation			-	125	197(3)	µs
V_{IN} rising POR threshold			-	4	4.2 (3)	V
V_{IN} falling POR threshold			3.4 (3)	3.5	-	
V_{IN} POR hysteresis			-	445	-	mV
3.3 V Pwm input (see “Timing diagram”)						
Sink impedance			-	33.5	-	kΩ
Source impedance			-	16.5	-	
Tri-state lower gate falling threshold		V_{CC} = 5 V	-	1.11	-	V
Tri-state lower gate rising threshold			-	0.87	-	
Tri-state upper gate rising threshold			-	2.13	-	
Tri-state upper gate falling threshold			-	1.95	-	
Tri-state shutdown window			1.3(3)	-	1.8(3)	
5 V PWM INPUT (see “Timing diagram”)						
Sink impedeance			-	16.5	-	kΩ
Source impedance			-	16.5	-	
Tri-state lower gate falling threshold		V_{CC} = 5 V	-	1.51	-	V
Tri-state lower gate rising threshold			-	1.14	-	
Tri-state upper gate rising threshold			-	3.24	-	
Tri-state upper gate falling threshold			-	3.02	-	

Parameter	Symbol	Test conditions	Min.(1)	Typ.	Max.(1)	Unit
Tri-state shutdown window		V_{CC} = 5 V	1.6 c	-	2.8 c	
Switching time						
GH turn-on propagation delay	t_{PDHU}	GL low to GH high, see Section 4	-	8	-	ns
GH turn-off propagation delay	t_{PDLU}	PWM low to GH low, see Section 4	-	40	-	
GL turn-on propagation delay	t_{PDHL}	GH low to GL high, see Section 4	-	8	-	
GL turn-off propagation delay	t_{PDLL}	PWM high to GL low, see Section 4	-	23		
GL exit tri-state propagation delay	t_{PDTSL}	Tri-state to GL high, see Section 4	-	25	-	
GH exit tri-state propagation delay	t_{PDTSU}	Tri-state to GH high, see Section 4	-	35	-	
PWML tri-state shutdown hold-off time	t_{TSSHDL}	PWM low to GL low, see Section 4	-	40	-	
PWMH tri-state shutdown hold-off time	t_{TSSHDU}	PWM low to GH low, see Section 4	-	50	-	
Current monitor						
$IREF_{IN}$ voltage range			0.8 (3)	1.2	1.6 (3)	V
IMON current gain accuracy (V_{CC} = 5 V)		10 A, T_J = 90 °C	-	±2	-	%
		≥10 A, T_J = 40 °C to 25 °C	-	±3	-	
		≥10 A, T_J = 20 °C to 125 °C	-	±4	-	
		≥10A, T_J = 0 °C to 125 °C	-	±5	-	
Downslope blanking time			-	160	-	ns
HFET overcurrent trip			-	90	-	A
IMON to $IREF_{IN}$ at OCP			1.1(3)	1.2	1.3 (3)	V
Temperature monitor						
Overtemperature rising threshold			-	140	-	°C
Overtemperature falling threshold			-	125	-	
Overtemperature hysteresis			-	15	-	
Temperature coefficient		T_J = 25 °C to 125 °C	-	8	-	mV/K
		T_J = -40 °C to +25 °C	-	8	-	
TMON voltage at 25 °C temperature		$V(T_J)$ = 0.6 V + (8 mV x T_J)	-	0.80	-	V
TMON high at overtemperature			2.3 (3)	2.5	2.7 (3)	
Bootstrap diode						
Forward voltage drop		5 mA	-	0.09	-	V
On-resistance	R_F		-	16	-	W

1. *Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.*
2. *These ratings vary with PCB layout and operating condition, and limited by SPS temperature and thermal shutdown trip point.*
3. *Limits apply across theoperating temperature range.*

Figure 6. **Timing diagram**



4.1 Electrical characteristic diagrams

Figure 7. 1.8 V V_{OUT} power stage efficiency

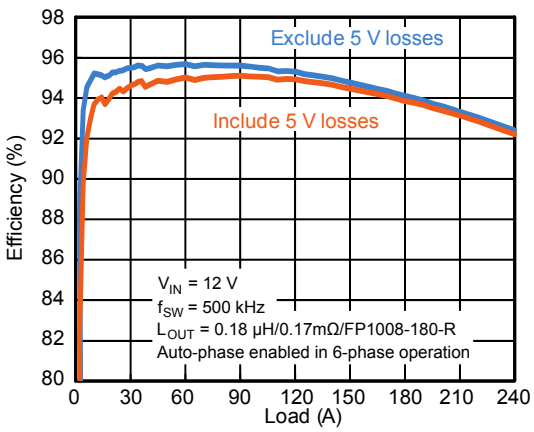


Figure 8. 1.2 V V_{OUT} power stage efficiency

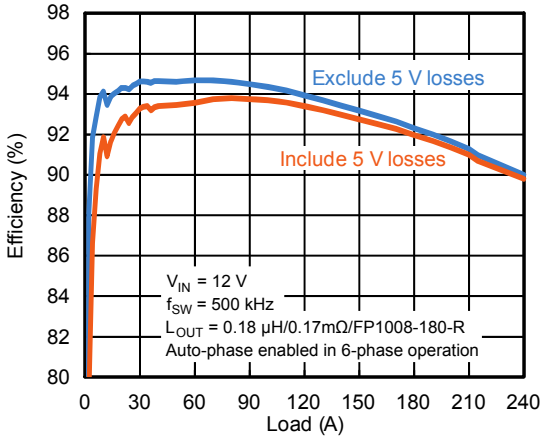


Figure 9. Power stage efficiency vs. V_{OUT}

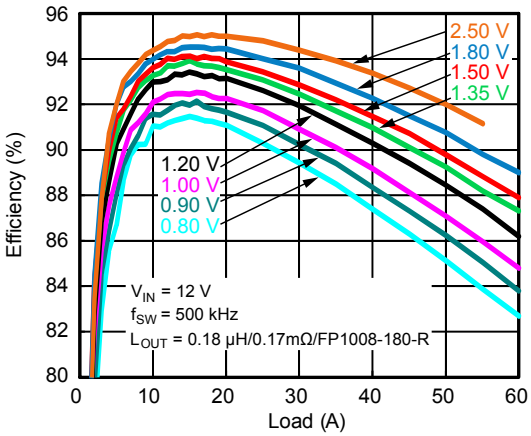


Figure 10. Power stage efficiency vs. frequency

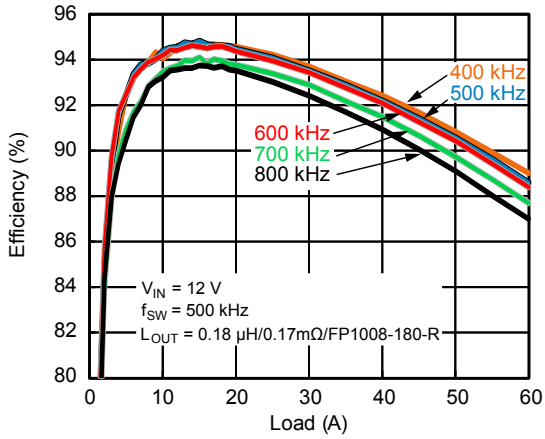


Figure 11. Power dissipation vs. V_{OUT}

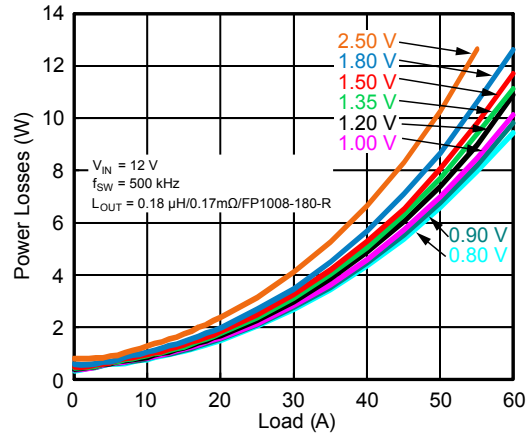
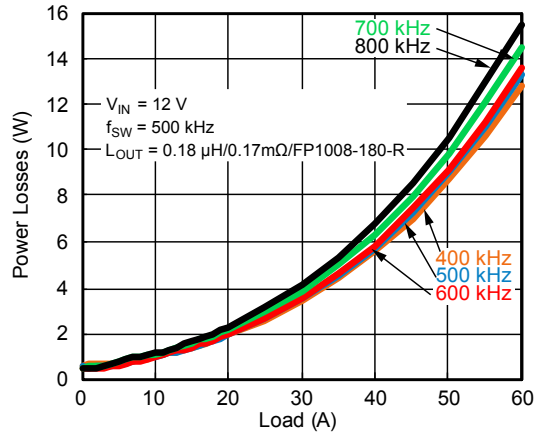


Figure 12. Power dissipation vs. frequency



5 Detailed operational description

The PM7050A is an optimized driver and power stage solution for high density synchronous DC/DC power conversion.

It includes high performance GH and GL drivers, an NFET controlled to function as a bootstrap diode, and MOSFET pair optimized for high switching frequency buck voltage regulators. It also includes advanced power management features:

- Accurate current and thermal reporting outputs.
- Fault protections of HFET overcurrent, HFET short, overtemperature, V_{CC} UVLO, and V_{IN} UVLO.

5.1 Power-on reset (POR)

During initial startup, the V_{CC} voltage rise is monitored. Once the rising V_{CC} voltage exceeds 3.86 V (typical) for 125 µs, then normal operation of the driver is enabled.

The PWM signals are passed through to the gate drivers, the TMON output is valid, and the IMON output starts at zero, and becomes valid on the first GL signal. If V_{CC} drops below the falling threshold of 3.58 V (typical), operation of the driver is disabled.

The PV_{CC} voltage is not monitored as it should be from the same supply as V_{CC}.

V_{IN} POR is also monitored. When both V_{CC} and V_{IN} reach above their POR trip points, it enables HFET overcurrent protection.

Both V_{CC} and V_{IN} POR are gated to the FAULT# pin, which goes high once both V_{CC} and V_{IN} are above their POR levels and no other faults occur.

5.2 Shoot-through protection

Prior to POR, the undervoltage protection function is activated and both GH and GL are held active low (HFET and LFET off).

After POR (the rising thresholds; see Electrical characteristics), and 125 µs delay, the PWM and LGCTRL signals are used to control both high-side and low-side MOSFETs as shown in Gh and gl operation truth table.

PM7050A's deadtime control is optimized for high efficiency and guarantees that simultaneous conduction of both FETs cannot occur.

Should the driver have no bias voltage applied (either V_{CC} or PV_{CC} missing) and be unable to actively hold the MOSFETs off, an integrated 20 kΩ resistor from the upper MOSFET gate to source helps in keeping the HFET device in its OFF state.

This can be especially critical in applications where the input voltage rises prior to the PM7050A V_{CC} and PV_{CC} supplies.

Table 4. Gh and gl operation truth table

Pwm	Lgctrl	Gh	Gl	Hfet, Lfet	Comment
Tri-state	X	0	0	Both off	-
0	1	0	1	LFET on	Normal
1	1	1	0	HFETon	Normal
0	0	0	0	LFEToff	GLlow
1	0	1	0	HFETon	Normal

5.3 Tri-state PWM input

The PM7050A supports a 3.3 V PWM tri-level input, compatible with digital multiphase controllers as well as other control ICs utilizing 3.3 V PWM logic. Should the pin be pulled into and remain in the tri-state window for a set hold off time (~25 ns), the driver forces both MOSFETs into their OFF states. When the PWM signal moves outside the shutdown window, the driver immediately resumes driving the MOSFETs according to the PWM commands.

This feature is utilized by PWM controllers as a method of forcing both MOSFETs off. Should the PWM input be left floating, the pin is pulled into the tri-state window internally and thus force both MOSFETs into a safe OFF state.

Although the PWM input can sustain a voltage as high as V_{cc}, the PM7050A is not compatible with a controller that actively drives its mid-level in tri-state higher than 1.7 V.

5.4 Bootstrap function

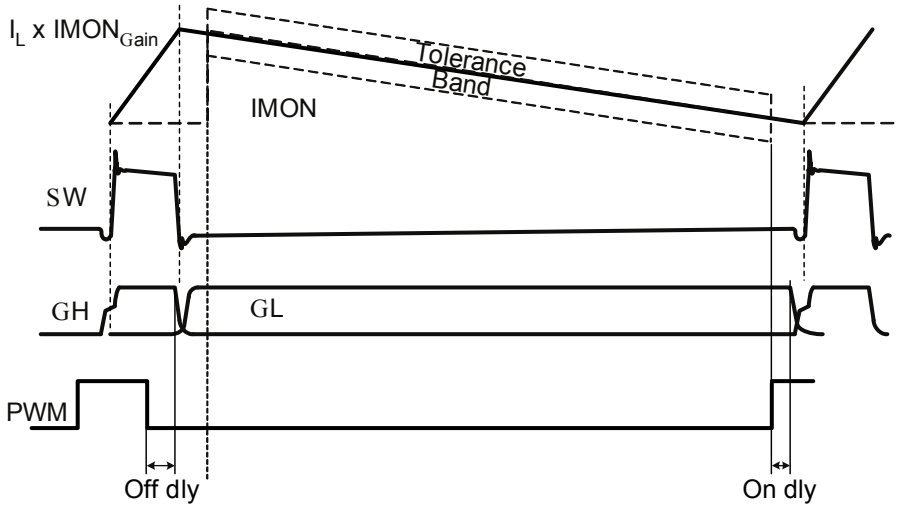
The PM7050A features an internal NFET that is controlled to function as a bootstrap diode. A high quality ceramic capacitor should be placed in close proximity across the BOOT and PHASE pins. The bootstrap capacitor can range between 0.1 µF to 0.22 µF (0402 to 0603 and X5R to X7R) for normal buck switching applications.

5.5 Current monitoring

LFET current is monitored and a signal proportional to that current is output on the IMON pin (relative to the REF_{IN} pin). The IMON and REF_{IN} pins should be connected to the appropriate current sense input pin of the controller. This method does not require external R_{SENSE} or DCR sensing of inductor current.

Figure 13 depicts the low-side current sense concept and demonstrates how the accuracy is defined. After the falling edge of PWM, there are two delays; one that represents the expected propagation delay from PWM to GH/SW, and a second blanking delay to allow time for the transition to settle; typical total time is ~ 350 ns. The IMON output approximates the actual I_L waveform shown within the tolerance band.

Figure 13. LFET current sample diagram



The HFET current is not monitored in the same way, so no valid measured current is available while PWM is high (and the short delays before and after). During this time, the IMON outputs the last valid LFET current before the sampling stopped. On startup after POR, the IMON outputs zero (relative to REF_{IN}, which represents zero current) until the switching begins, and then the current can be properly measured.

The high-side FET current is separately monitored for OC conditions; see the Overcurrent protection section.

5.6 Overcurrent protection

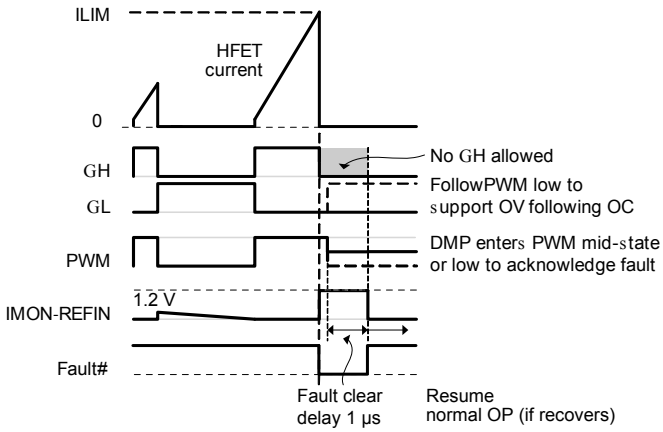
Figure 14 shows the timing diagram of an overcurrent fault. There is a comparator monitoring the HFET current while it is on (GH high; also requires V_{IN} POR above its trip point). If the current is higher than 90 A (typical; not user-programmable), then an OC fault is detected.

The GH is forced low, even if PWM is still high; this effectively shortens the PWM (and GH) pulse width, to limit the current. The IMON pin is pulled up to REF_{IN} +1.2 V , which is detected by the controller as an overcurrent fault.

The controller is then expected to force PWM to tri-state (which gates off both FETs) or low state (turns on LFET), either of which signals the SPS that the fault has been acknowledged. This starts a ~1 µs fault clear delay. The IMON flag is released after the delay. The driver then responds to PWM inputs normally.

Note that if the controller does NOT acknowledge, the IMON flag stays high indefinitely, which also holds GH low. If OC is detected, the FAULT# pin is also pulled low; the timing on the FAULT# pin follows that of the IMON pin.

Figure 14. Overcurrent fault timing diagram



5.7 Shorted HFET protection

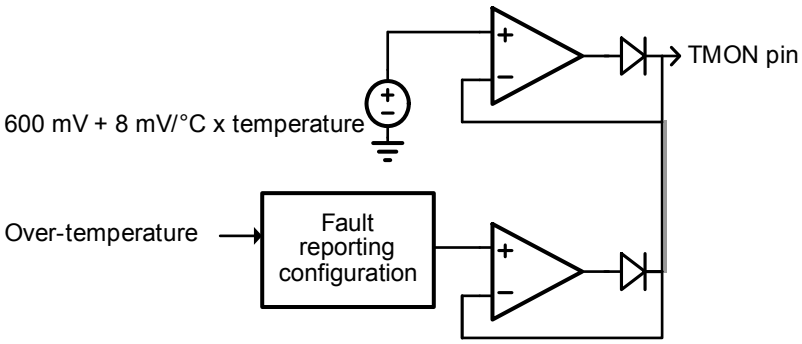
In the case of a shorted HFET, the SW node has excessive positive voltage present even when the LFET is turned on. The PM7050A monitors the SW node during periods when the LFET is on (GL is high), and should that voltage exceed 100 mV (typical), the HFET short fault is declared. The PM7050A pulls the IMON pin high, and the FAULT# is pulled low. But the fault is latched; V_{CC} POR is needed to reset it. GH is gated low (ignore PWM = high), but the PM7050A still responds to PWM tri-state and logic low.

5.8 Thermal monitoring

The PM7050A monitors its internal temperature and provides a signal proportional to that temperature on the TMON pin. TMON has a voltage of 600 mV at 0 °C and reflects temperature at 8 mV/°C. The TMON output is valid 125 µs after V_{CC} POR.

Figure 15 shows a simplified functional representation. The top section includes the sensor and the output buffer. The bottom section includes the protection sensing, that pulls the output high. The TMON pin is configured internally so that a user can tie multiple pins together externally and the resulting TMON bus assumes the voltage of the highest contributor (representing the highest temperature).

Figure 15. Overcurrent fault



5.9 Thermal protection

If the internal temperature exceeds the overtemperature trip point (+140 °C typical), the TMON pin is pulled high (to ~2.5 V), and the FAULT# pin is pulled low. No other action is taken on-chip. Both the TMON and FAULT# pins remain in the fault mode, until the junction temperature drops below +125 °C typical; at that point, the TMON and FAULT# pins resume normal operation; the DMP can detect that the fault condition has gone away, and decide what to do next.

5.10 FAULT reporting

Overcurrent and shorted HFET detections pull the IMON pin to a high (fault) level, such that the DMP should quickly recognize it as out of the normal range. Overtemperature detection pulls the TMON pin to a high (fault) level, such that the PWM controller should quickly recognize it as out of the normal range. All of the above faults, plus the V_{CC} and V_{IN} POR (UVLO) conditions, also pull down the FAULT# pin. This can be used by the controller (or system) as fault detection, and can also be used to disable the controller, through its enable pin. The fault reporting and respective SPS response are summarized in Table 5.

Table 5. Fault reporting summary

Fault event	Imon	Tmon	Fault#	Response
OC	High	n/a	Low	GH gated off. The controller should acknowledge and force its PWM to tri-state to keep both HFET and LFET off. The fault is cleared ~1 µs after PWM enters tri-state, otherwise, it stays asserted. (if system OVP occurs, the controller may send PWM to turn on LEFT).
Shorted HFET	IMON - latched high	n/a	FAULT# latched low	GH gated off, until fault latch is cleared by VCC POR. GL follows PWM
OT	n/a	High	Low	GH and GL follow PWM.
V_{CC} UVLO	IMON - REF_{IN} = 0 V	TMON not valid	Low	Switching stops while in UVLO. Once above V_{CC} POR after 125 µs: GH and GL follow PWM; the FAULT# is released; TMON is valid; IMON - REF_{IN} is valid after GL first goes low.
V_{IN} UVLO	OC not valid	n/a	Low	GH and GL follow PWM.

6 PCB layout considerations

Proper PCB layout reduces noise coupling to other circuits, improves thermal performance, and maximizes the efficiency. The following is meant to lead to an optimized layout:

- Place multiple 10 µF or greater ceramic capacitors directly at device between V_{IN} and P_{GND} as indicated in Fig. 16. This is the most critical decoupling and reduced parasitic inductance in the power switching loop. This reduces overall electrical stress on the device as well as reducing coupling to other circuits. Best practice is to place the decoupling capacitors on the same PCB side as the device. For a design with tight space requirements, these decoupling capacitors can be placed under the device, i.e., bottom layer, as shown in Fig. 18.
- Connect GND to the system GND plane with a large via array as close to the GND pins as design rules allow. This improves thermal and electrical performance.
- Place PV_{CC}, V_{CC} and BOOT-PHASE decoupling capacitors at the IC pins as shown in Fig. 16.
- Note that the SW plane connecting the PM7050A and inductor must carry full load current and create resistive loss if not sized properly. However, it is also a very noisy node that should not be oversized or routed close to any sensitive signals. Best practice is to place the inductor as close to the device as possible, thus minimizing the required area for the SW connection. If one must choose a long route of either the V_{OUT} side of the inductor or the SW side, choose the quiet V_{OUT} side. Best practice is to locate the PM7050A as close to the final load as possible and thus avoid noisy or lossy routes to the load.
- The IMON and IREF network and their vias should not sit on the top of the V_{IN} plane, a keep out area is recommended, as shown in Fig. 18.
- The PCB is a better thermal heatsink material than any top side cooling materials. The PCB always has enough vias to connect V_{IN} and GND planes. Insufficient vias yield lower efficiency and very poor thermal performance. Fig. 17 and Fig. 18 show a multiphase PCB layout example.

7 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

7.1 QFN 4X5 26L package information

Figure 16. QFN 4X5 26L package outline

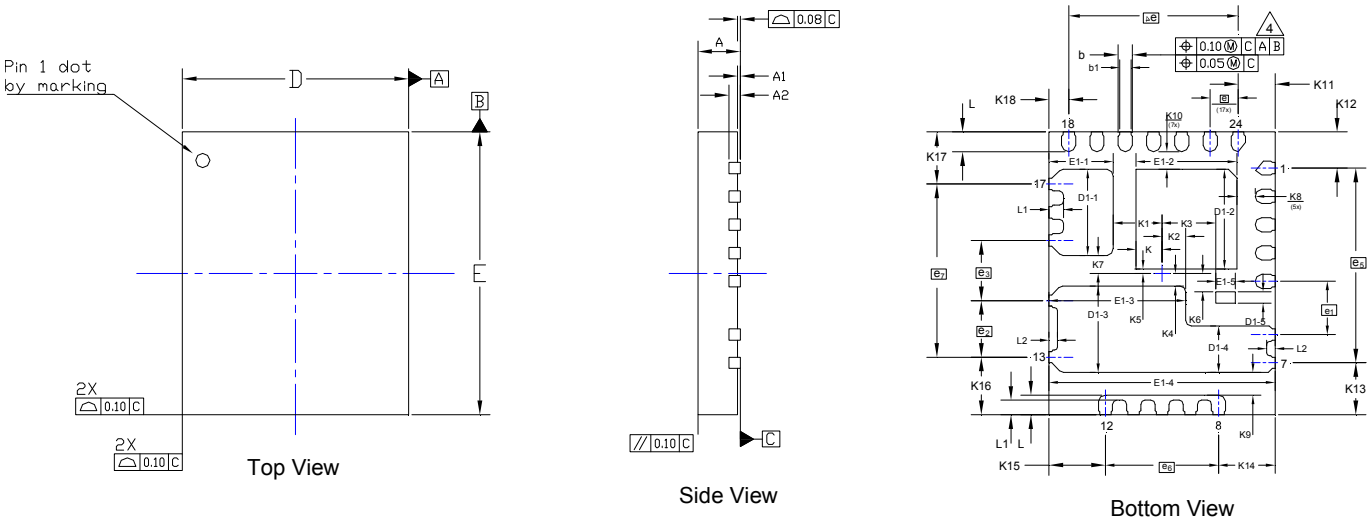


Table 6. QFN 4X5 26L mechanical data

Symbol	Dimensions (mm)		
	Min.	Nom.	Max.
A	0.70	0.75	0.80
A1	0.00	-	0.05
A2		0.20 REF	
b	0.20	0.25	0.30
b1	0.15	0.20	0.25
D	3.90	4.00	4.10
e		0.50 BSC	
e1		0.94 BSC	
e2		1.00 BSC	
e3		1.06 BSC	
e4		3.00 BSC	
e5		3.44 BSC	
e6		2.00 BSC	
e7		3.06 BSC	
E	4.90	5.00	5.10
L	0.25	0.35	0.45

Symbol	Dimensions (mm)		
	Min.	Nom.	Max.
L1	0.16	0.26	0.36
L2	0.05	0.15	0.25
N		24	
D1-1	1.43	1.53	1.63
D1-2	1.67	1.77	1.87
D1-3	1.42	1.52	1.62
D1-4	0.72	0.82	0.92
D1-5	0.10	0.20	0.30
E1-1	1.04	1.14	1.24
E1-2	1.69	1.79	1.89
E1-3	2.32	2.42	2.52
E1-4	3.90	4.00	4.10
E1-5	0.25	0.35	0.45
K		0.46 REF	
K1		0.86 REF	
K2		0.42 REF	
K3		0.95 REF	
K4		0.23 REF	
K5		0.08 REF	
K6		0.33 REF	
K7		0.32 REF	
K8		0.33 REF	
K9		0.40 REF	
K10		0.31 REF	
K11		0.65 REF	
K12		0.64 REF	
K13		0.92 REF	
K14		1.00 REF	
K15		1.00 REF	
K16		1.02 REF	
K17		0.92 REF	
K18		0.35 REF	

Revision history

Table 7. **Document revision history**

Date	Version	Changes
2-Dec-2024	1	Initial release.

Contents

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