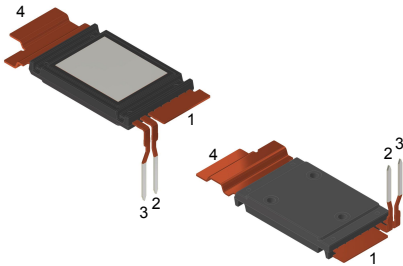
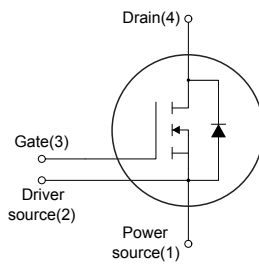


Automotive-grade silicon carbide Power MOSFET 1200 V, 8.5 mΩ typ., 239 A in a STPAK high creepage package



**STPAK
high creepage**



NG3DS2PS1D4



Product status link


[SCTHCT250N12G3AG](#)

Product summary

Order code	SCTHCT250N12G3AG
Marking	HCT25N12G3AG
Package	STPAK high creepage
Packing	Tray

Features

Order code	V _{DS}	R _{DS(on)} typ.	I _D
SCTHCT250N12G3AG	1200 V	8.5 mΩ	239 A

- AEC-Q101 qualified 
- Very low R_{DS(on)} over the entire temperature range
- High speed switching performances
- Very fast and robust intrinsic body diode
- Very high operating junction temperature capability (T_J = 200 °C)
- Source sensing pin for increased efficiency
- Low thermal resistance multi sintering package
- 7.3 mm minimum creepage (including 0.6 mm particles)
- 1020 Vrms PD2

Application

- [Main inverter \(electric traction\)](#)

Description

This silicon carbide Power MOSFET device has been developed using ST's advanced and innovative 3rd generation SiC MOSFET technology. The device features a very low R_{DS(on)} over the entire temperature range combined with low capacitances and very high switching operations, which improve application performance in frequency, energy efficiency, system size and weight reduction.

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	-10 to 22	V
	Gate-source voltage (recommended operating values)	-5 to 18	
	Gate-source transient voltage, $t_p < 1 \mu s$, $t \leq 10$ hours over lifetime	-11 to 25	
I_D	Drain current (continuous) at $T_C = 25 \text{ }^\circ\text{C}$	239	A
	Drain current (continuous) at $T_C = 100 \text{ }^\circ\text{C}$	180	
$I_{DM}^{(1)}$	Drain current (pulsed)	720	A
P_{TOT}	Total power dissipation at $T_C = 25 \text{ }^\circ\text{C}$	994	W
V_{ISO}	Insulation withstand voltage applied between each pin and the heat sink plate (DC voltage, $t = 1 \text{ s}$)	4.3	kV
T_{stg}	Storage temperature range	-55 to 200	$^\circ\text{C}$
T_J	Operating junction temperature range		

1. Pulse width is limited by safe operating area.

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	0.176	$^\circ\text{C}/\text{W}$

2 Electrical characteristics

$T_C = 25\text{ °C}$ unless otherwise specified.

Table 3. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}$	1200			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}, V_{DS} = 1200\text{ V}$			20	μA
I_{GSS}	Gate-body leakage current	$V_{DS} = 0\text{ V}, V_{GS} = -10\text{ to }22\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 10\text{ mA}$	2.0	3.2	4.4	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 18\text{ V}, I_D = 120\text{ A}$		8.5	10.5	m Ω
		$V_{GS} = 18\text{ V}, I_D = 120\text{ A}, T_J = 175\text{ °C}$		14		
		$V_{GS} = 18\text{ V}, I_D = 120\text{ A}, T_J = 200\text{ °C}$		15.3		

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 800\text{ V}, f = 1\text{ MHz}, V_{GS} = 0\text{ V}$	-	7370	-	pF
C_{oss}	Output capacitance		-	363	-	pF
C_{rss}	Reverse transfer capacitance		-	56	-	pF
R_g	Gate input resistance	$f = 1\text{ MHz}, I_D = 0\text{ A}$	-	0.65	-	Ω
Q_g	Total gate charge	$V_{DD} = 800\text{ V}, V_{GS} = -5\text{ to }18\text{ V}, I_D = 120\text{ A}$	-	304	-	nC
Q_{gs}	Gate-source charge		-	81	-	nC
Q_{gd}	Gate-drain charge		-	114	-	nC

Table 5. Switching energy (inductive load)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
E_{on}	Turn-on switching energy	$V_{DD} = 800\text{ V}, I_D = 120\text{ A},$	-	2156	-	μJ
E_{off}	Turn-off switching energy	$R_G = 4.7\text{ }\Omega, V_{GS} = -5\text{ V to }18\text{ V}$	-	2611	-	μJ

Table 6. Reverse SiC diode characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{SD}	Diode forward voltage	$I_{SD} = 120\text{ A}, V_{GS} = 0\text{ V}$	-	3.1	-	V
t_{rr}	Reverse recovery time	$I_{SD} = 120\text{ A}, di/dt = 1\text{ kA}/\mu\text{s},$ $V_{GS} = -5\text{ to }18\text{ V}, V_{DD} = 800\text{ V}$	-	38.6	-	ns
Q_{rr}	Reverse recovery charge		-	530	-	nC
I_{RRM}	Reverse recovery current		-	24.5	-	A

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

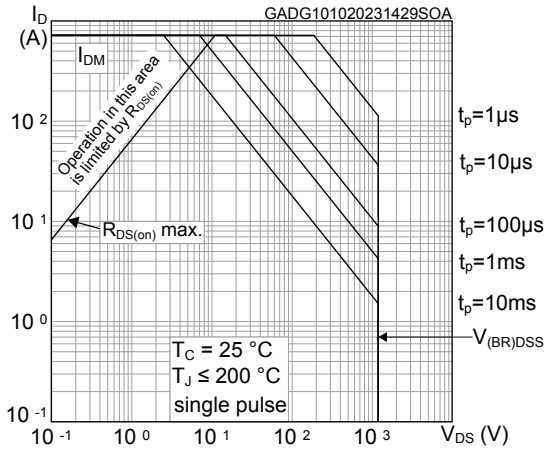


Figure 2. Maximum transient thermal impedance

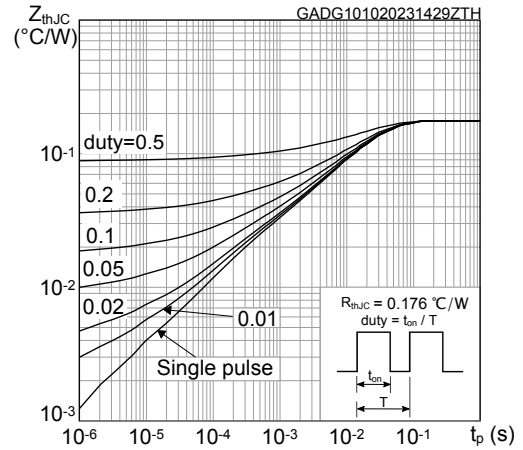


Figure 3. Typical output characteristics ($T_J = 25\text{ °C}$)

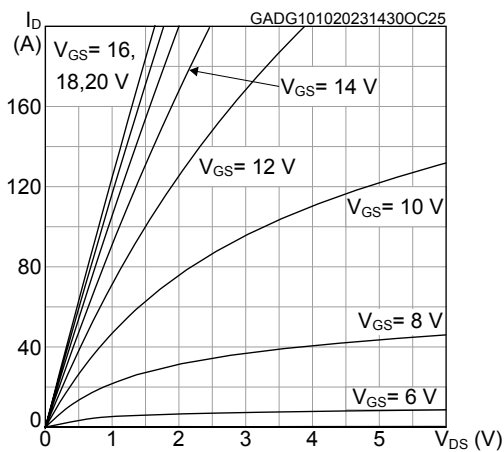


Figure 4. Typical output characteristics ($T_J = 200\text{ °C}$)

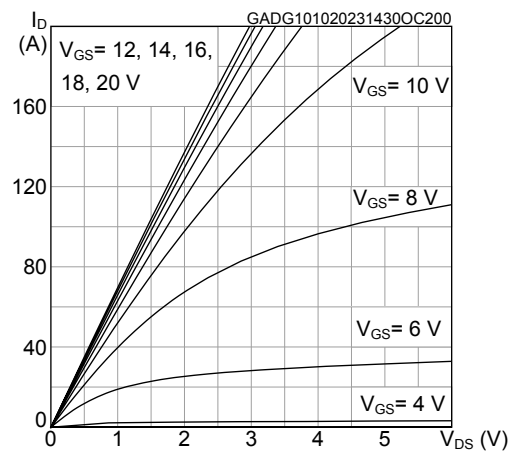


Figure 5. Typical transfer characteristics

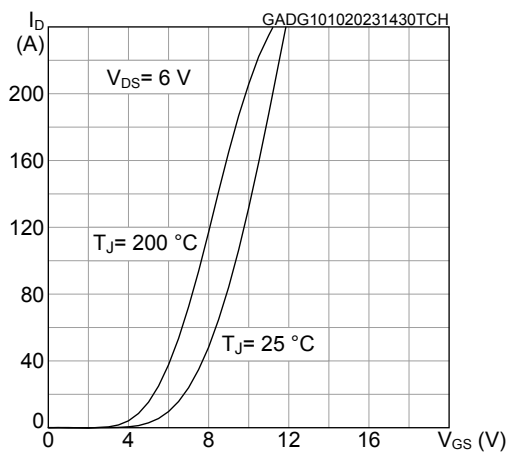


Figure 6. Total power dissipation

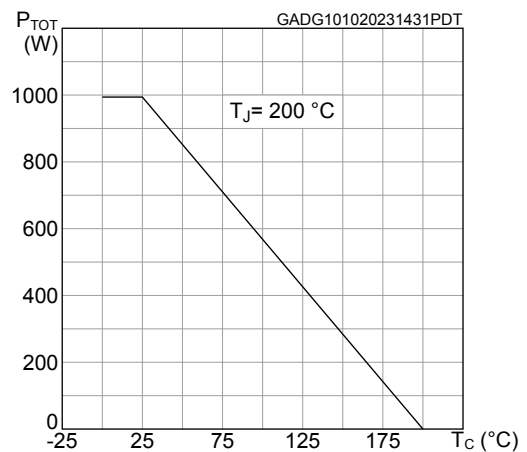


Figure 7. Typical gate charge characteristics

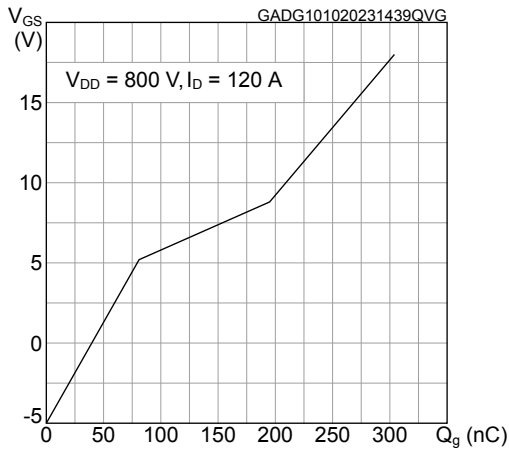


Figure 8. Typical capacitance characteristics

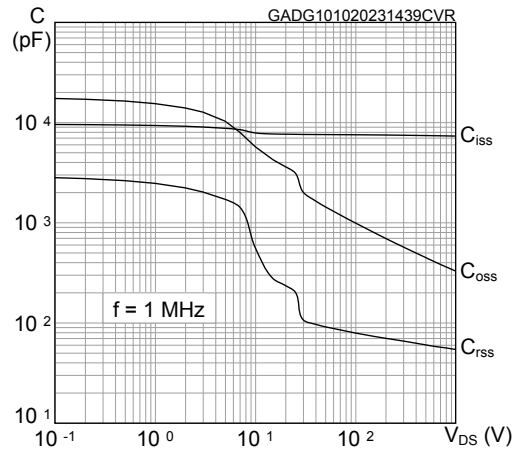


Figure 9. Typical switching energy vs drain current

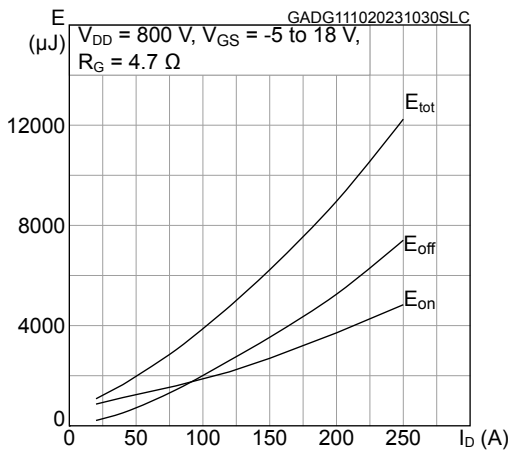


Figure 10. Typical switching energy vs gate resistance

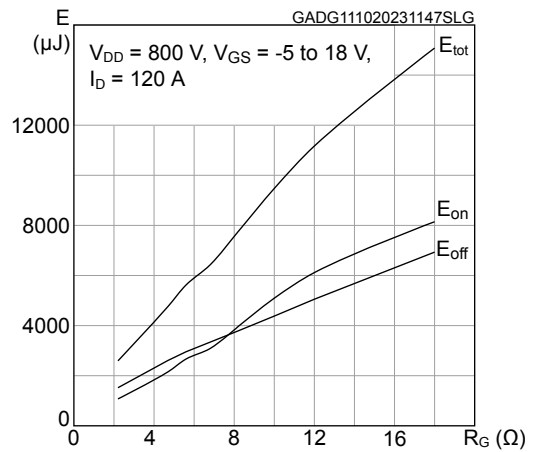


Figure 11. Switching energy vs. junction temperature

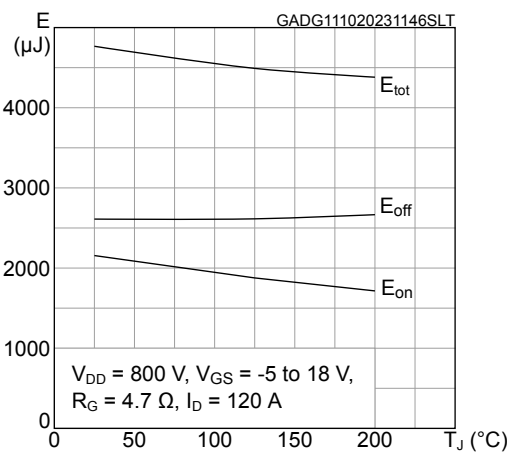


Figure 12. Normalized breakdown voltage vs temperature

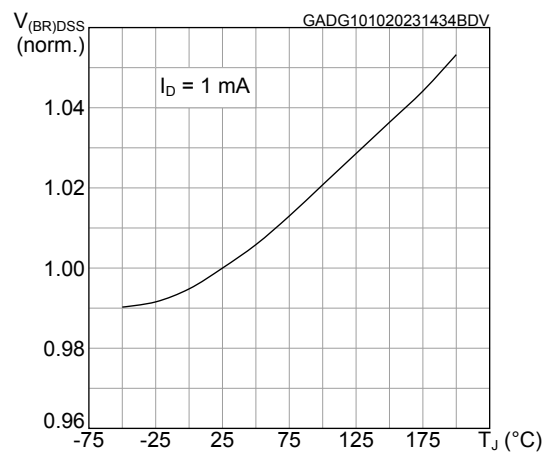


Figure 13. Normalized gate threshold vs temperature

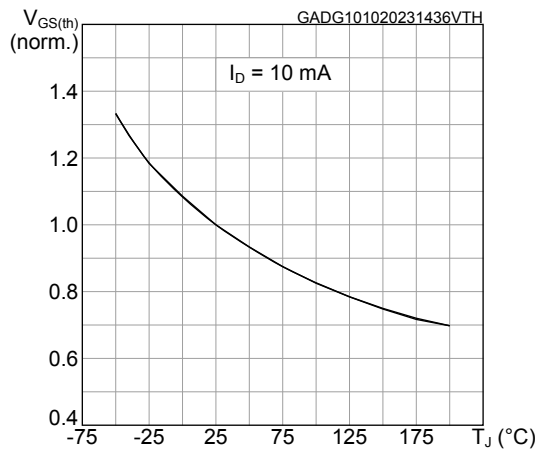


Figure 14. Normalized on-resistance vs temperature

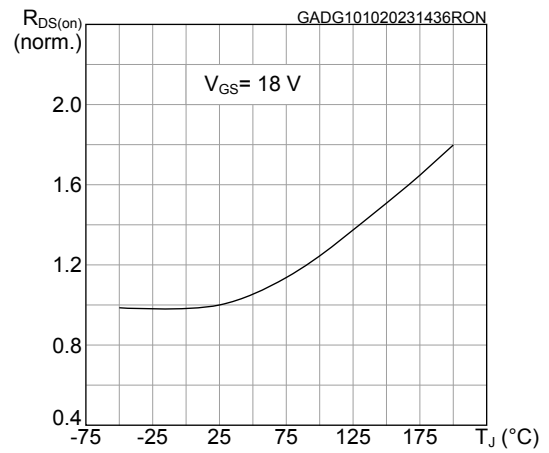


Figure 15. Typical reverse conduction characteristics (T_J = 25 °C)

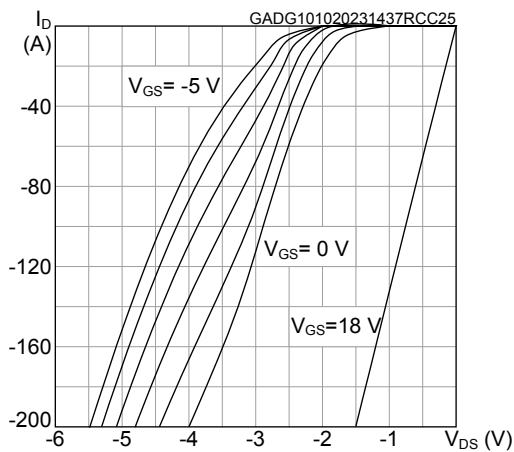
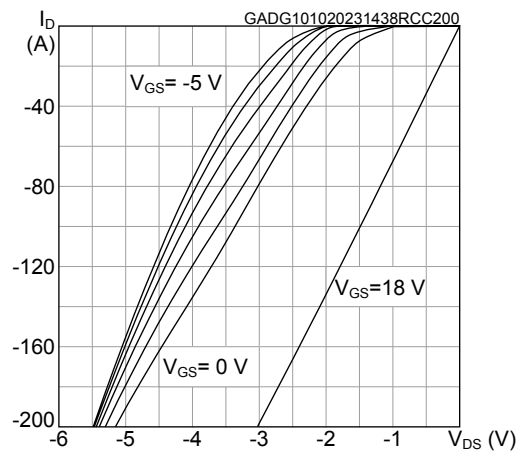


Figure 16. Typical reverse conduction characteristics (T_J = 200 °C)

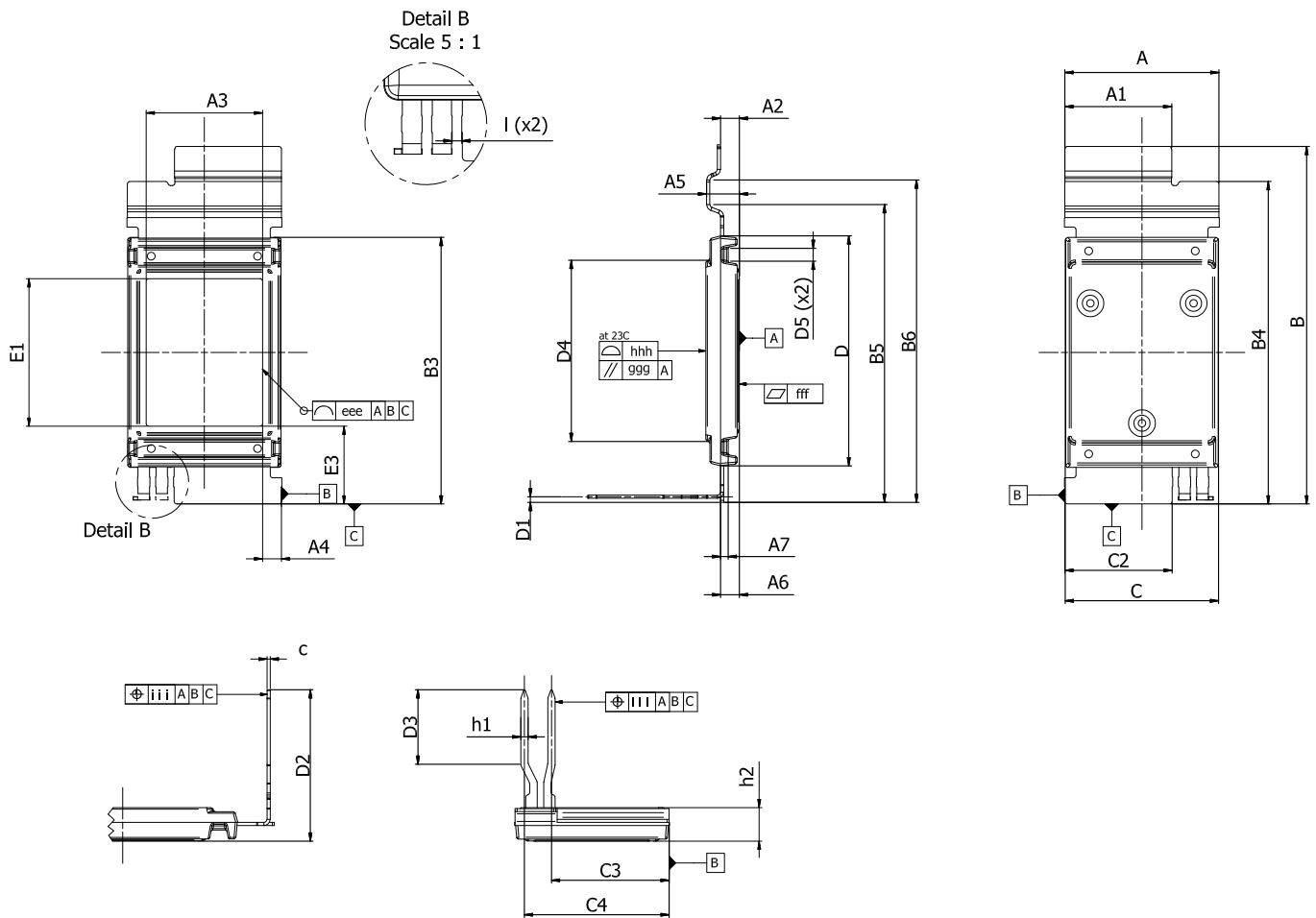


3 Package information

To meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

3.1 STPAK high creepage package information

Figure 17. STPAK high creepage package outline



DM00305987_HC_10

Table 7. STPAK high creepage package mechanical data

Ref.	Dimensions			Notes
	mm			
	Min.	Typ.	Max.	
A	18.60	18.80	19.00	
A1	12.85	13.05	13.25	
A2	2.00	2.30	2.60	
A3	14.20	14.70	15.20	Exposed Pad
A4	1.55	2.05	2.55	
A5	3.80	4.00	4.20	
A6	2.10	2.30	2.50	
A7	0.85	0.95	1.05	Indent (x2)
B	43.40	43.70	44.00	
B3	32.20	32.50	32.80	
B4	39.10	39.40	39.70	
B5	36.07	36.37	36.67	
B6	39.07	39.37	39.67	
c	0.34	0.39	0.44	
C		18.55	19.10	
C2	12.90	13.10	13.30	
C3		14.35		
C4		17.65		
D	27.90	28.10	28.30	
D1		0.69		
D2	18.50	19.00	19.50	
D3	9.10	9.60	10.10	
D4	21.95	22.15	22.35	
D5	1.45	1.55	1.65	Indent (x2)
E1	18.00	18.50	19.00	Exposed Pad
E3	8.75	9.25	9.75	
h1	0.85	0.90	0.95	x2 – Pins width
h2	4.00	4.10	4.20	
I	0.60	0.70	0.80	
eee	0.50			
fff	0.10 at 23 °C – 0.05 at 220 °C			Convex with center higher than edges
ggg	0.05			
hhh	0.10			
iii	0.60			

Revision history

Table 8. Document revision history

Date	Revision	Changes
04-Nov-2024	1	First release.

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