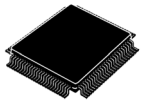
SPC584Nx, SPC58ENx, SPC58NNx

32-bit Power Architecture microcontroller for automotive ASIL-D applications

Datasheet - production data

FPBGA292 (17 x 17 x 1.8 mm)



eLQFP176 (24 x 24 x 1.4 mm)

Features

- AEC-Q100 qualified
- 32-bit Power Architecture VLE compliant CPU cores:
  - Five enhanced main e200z4256n3 cores, dual issue, two paired in lockstep
  - Floating Point, End-to-End Error Correction
- 6576 KB (6288 KB code flash + 288 KB data flash) on-chip flash memory:
  - supports read during program and erase operations, and multiple blocks allowing EEPROM emulation
  - Supports read while read between the two code Flash partitions.
- 128 KB on-chip general-purpose SRAM (in addition to 384 KB included in the CPUs)
- 96-channel direct memory access controller (eDMA)
- Comprehensive new generation ASIL-D safety concept
  - ASIL-D of ISO 26262
  - FCCU for collection and reaction to failure notifications
  - Memory Error Management Unit (MEMU) for collection and reporting of error events in memories
  - Cyclic redundancy check (CRC) unit
- Junction temperature range -40 °C to 165 °C
- Dual-channel FlexRay controller
- Hardware Security Module (HSM)
- GTM344 - generic timer module
  - Intelligent complex timer module
  - 144 channels (48 input and 96 output)
  - 5 programmable fine grain multi-threaded cores
  - 61 KB of dedicated RAM
  - 24-bit wide channels
- Enhanced analog-to-digital converter system with:
  - 1 supervisor 12-bit SAR analog converter
  - 2 separate 10-bit SAR analog converter
  - 4 separate fast 12-bit SAR analog converters
  - 6 separate 16-bit Sigma-Delta analog converter with programmable decimation filters
- SAR ADC Queued digital interfaces for individual channel ordering and command sequencing
- Communication interfaces
  - 7 LINFlexD modules
  - 8 deserial serial peripheral interface (DSPI) modules
  - 7 modular controller area network (MCAN) modules, and one time-triggered controller area network (M-TTCAN), all supporting flexible data rate (ISO CAN-FD)
- One Ethernet controller 10/100 Mbps, compliant IEEE 802.3-2008
- Flexible Power Supply options:
  - External Regulators (1.2 V core, 3.3 V–5 V IO)
  - Single internal SMPS regulator
- Nexus development interface (NDI) per IEEEISTO 5001-2003 standard, with some support for 2010 standard
- Boot assist Flash (BAF) supports factory programming using a serial bootload through the asynchronous CAN or LIN/UART

Table 1. Device summary

Package	Part number			
	4 MB		6 MB	
	Single core	Dual core	Dual core	Triple core
eLQFP176	SPC584N80E7	SPC58EN80E7	SPC58EN84E7	SPC58NN84E7
FPBGA292	SPC584N80C3	SPC58EN80C3	SPC58EN84C3	SPC58NN84C3

Contents

1 Introduction

1.1 Document overview

This document provides electrical specifications, pin assignments, and package diagrams for the SPC5x series of microcontroller units (MCUs). For functional characteristics, see the SPC5x microcontroller reference manual.

1.2 Description

The SPC58xNx microcontroller belongs to a family of devices superseding the SPC5x family. SPC58xNx is built on the legacy of the SPC5x family, while introducing new features coupled with higher throughput to provide substantial reduction of cost per feature and significant power and performance improvement (MIPS per mW).

1.3 Device feature summary

Table 2 lists a summary of major features for the SPC58xNx device. The feature column represents a combination of module names and capabilities of certain modules. A detailed description of the functionality provided by each on-chip module is given later in this document.

Table 2. SPC58xNx feature summary

Feature	Description
SPC58 family	40 nm
Computing Shell 0	
Number of Cores	up to 2
Number of checker cores	up to 1
Local RAM	32 KB Instruction
	128 KB Data
Single Precision Floating Point	Yes
SIMD (LSP)	Yes
VLE	Yes
Cache	16 KB Instruction
	8 KB Data
Computing Shell 1	
Number of Cores	1
Number of checker cores	up to 1
Local RAM	32 KB Instruction
	128 KB Data
Single Precision Floating Point	Yes

Table 2. SPC58xNx feature summary (continued)

Feature	Description
SIMD (LSP)	Yes
VLE	Yes
Cache	16 KB Instruction
	8 KB Data
Other	
Security (HSM Module)	up to 1
MPU	Yes
Semaphores	Yes
CRC Channels	2 x 4
Software Watchdog Timer (SWT)	4
Core Nexus Class	3+
Event Processor	4 x SCU
	4 x PMC
Run control Module	Yes
System SRAM	128 KB
User Flash memory	up to 6144 KB code / 256 KB data
Security Flash memory	up to 144 KB code / 32 KB data
Flash fetch accelerator	2 x 2 x 4 x 256-bit
Flash Overlay RAM	2 x 16 KB
Calibration Interface	64-bit IPS Slave
DMA channels	96
DMA Nexus Class	3
LINFlexD	7
M_CAN supporting CAN-FD according to ISO 11898-1 2015 (instances supporting also TTCAN)	8 (1)
DSPI	8
Microsecond channel downlink	2
SENT bus	15
I2C	1
PSI5 / PSI5-S bus	2 / 1
FlexRay	1 x Dual channel
Ethernet	1
SIPI / LFAST Interprocessor bus	High Speed

Table 2. SPC58xNx feature summary (continued)

Feature	Description
System Timers	8 PIT channels
	4 AUTOSAR® (STM)
	RTC/API
GTM Timer	48 Input Channels, 96 Output Channels
GTM RAM	61 KB
Interrupt controller	> 620 sources
ADC (SAR)	7
ADC (SD)	6
Temp. sensor	Yes
Self Test Controller	Yes
PLL	Dual PLL with FM
Integrated switch mode voltage regulator (SMPS)	Yes
External Power Supplies	3.3 V - 5V, 1.2 V
Low Power Modes	Stop Mode
	Halt Mode

1.4 Block Diagram

The figures below show the top-level block diagrams.

Figure 1. Block Diagram

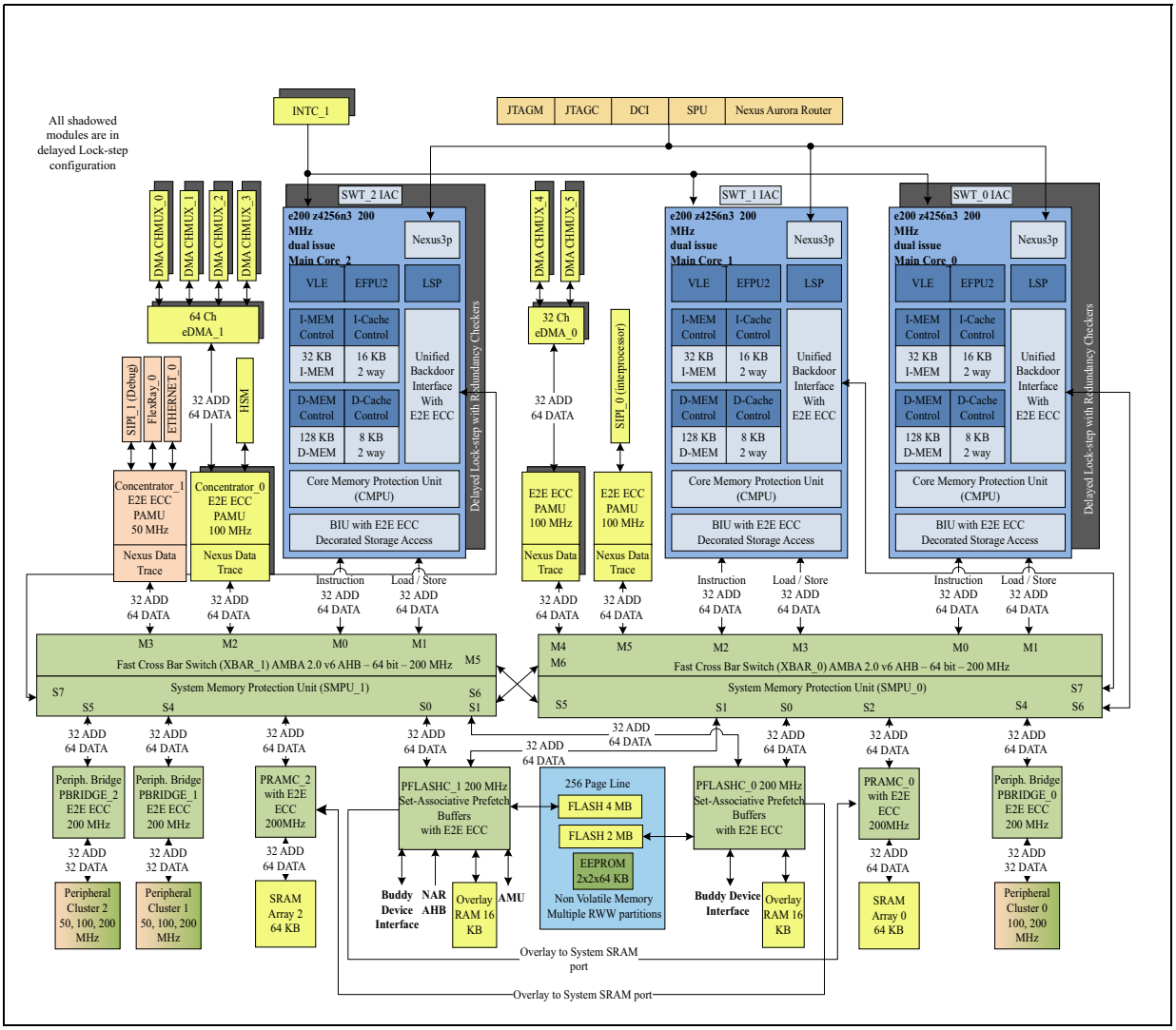
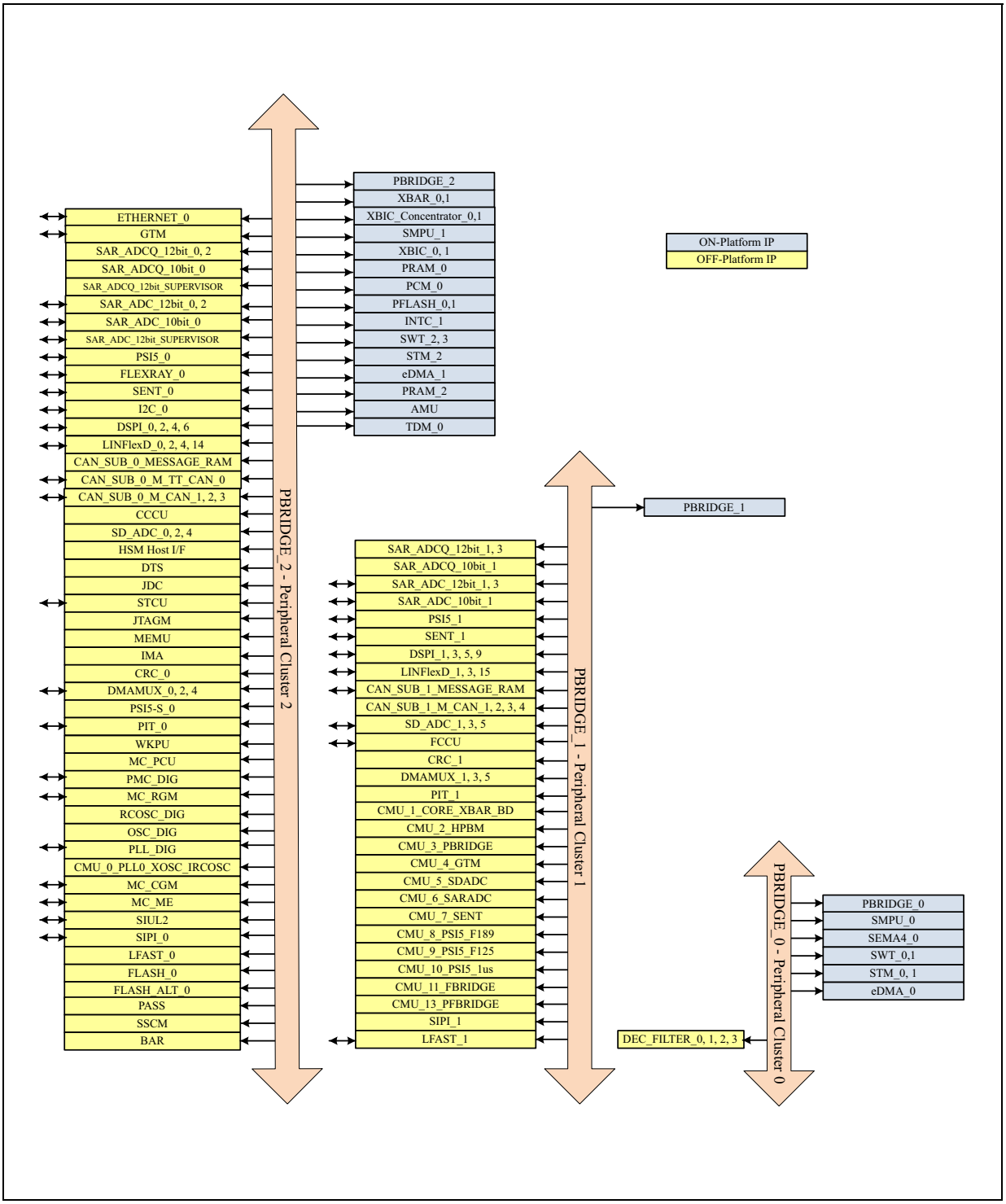


Figure 2. Periphery allocation



1.5 Features

On-chip modules within SPC58xNx include the following features:

- Three enhanced main CPUs, dual issue, 32-bit CPU core complexes (e200z4256n3), two of them having a checker core in lock-step.
  - Power Architecture embedded specification compliance
  - Instruction set enhancement allowing variable length encoding (VLE), encoding a mix of 16-bit and 32-bit instructions, for code size footprint reduction
  - Single-precision floating point operations
  - Lightweight signal processing auxiliary processing unit (LSP APU) instruction support for digital signal processing (DSP on Core_2)
  - 32 KB Local instruction RAM and 128 KB local data RAM for Core_0, Core_1 and Core_2
  - 16 KB I-Cache and 8 KB D-Cache for Core_0, Core_1 and Core_2
- 6582 KB on-chip Flash
  - Supports read during program and erase operations, and multiple blocks allowing EEPROM emulation
  - Supports read while read between the two code Flash partitions.
- 128 KB on-chip general-purpose SRAM (+ 384 KB data RAM included in the CPUs)
- Multi channel direct memory access controllers (eDMA paired in lock-step)
  - One eDMA with 64 channels
  - One eDMA with 32 channels
- One interrupt controller (INTC) in lock-step
- Dual phase-locked loops with stable clock domain for peripherals and FM modulation domain for computational shell
- Dual crossbar switch architecture for concurrent access to peripherals, Flash, or RAM from multiple bus masters with end-to-end ECC
- Hardware security module (HSM) to provide robust integrity checking of Flash memory
- System integration unit lite (SIUL)
- Boot assist Flash (BAF) supports factory programming using a serial bootload through the asynchronous CAN or LIN/UART.
- GTM344 - generic timer module
  - Intelligent complex timer module
  - 144 channels (48 input and 96 output)
  - 5 programmable fine grain multi-threaded cores
  - 61 KB of dedicated RAM
  - 24-bit wide channels
  - Hardware support for engine control, motor control and safety related applications
- Enhanced analog-to-digital converter system with
  - One supervisor 12-bit SAR analog converter
  - Four separate fast 12-bit SAR analog converters
  - Two separate 10-bit SAR analog converters
  - Six separate 16-bit Sigma-Delta analog converters
- Eight deserial serial peripheral interface (DSPI) modules

- Seven LIN and UART communication interface (LINFlexD) modules
  - LINFlexD_0 is a Master/Slave
  - All others are Masters
- Eight MCAN interfaces with advanced shared memory scheme and ISO CAN-FD support, one supporting time-triggered controller area network (TTCAN)
- Dual-channel FlexRay controller
- One ethernet controller 10/100 Mbps, compliant IEEE 802.3-2008
  - IEEE 1588-2008 Time stamping (internal 64-bit time stamp)
  - IEEE 802.1AS and IEEE 802.1Qav (AVB-Feature)
  - IEEE 802.1Q VLAN tag detection
  - IPv4 and IPv6 checksum modules
- Flexible Power Supply options:
  - External Regulators (1.2V core, 3.3V–5V IO)
  - Single internal SMPS regulator
- Nexus development interface (NDI) per IEEE-ISTO 5001-2003 standard, with some support for 2010 standard.
- Device and board test support per Joint Test Action Group (JTAG) (IEEE 1149.1)

2 Package pinouts and signal descriptions

Refer to the SPC58xNx IO_ Definition document.

It includes the following sections:

1. Package pinouts
2. Pin descriptions
   a) Power supply and reference voltage pins
   b) System pins
   c) LVDS pins
   d) Generic pins

3 Electrical characteristics

3.1 Introduction

The present document contains the target Electrical Specification for the 40 nm family 32-bit MCU SPC58xNx products.

In the tables where the device logic provides signals with their respective timing characteristics, the symbol “CC” (Controller Characteristics) is included in the “Symbol” column.

In the tables where the external system must provide signals with their respective timing characteristics to the device, the symbol “SR” (System Requirement) is included in the “Symbol” column.

The electrical parameters shown in this document are guaranteed by various methods. To give the customer a better understanding, the classifications listed in *Table 3* are used and the parameters are tagged accordingly in the tables where appropriate.

Table 3. Parameter classifications

Classification tag	Tag description
P	Those parameters are guaranteed during production testing on each individual device. NOTE: Parameters specified at junction temperature T_J = 165 °C are tested at T_J = 150 °C in production. Evaluation at higher temperature is performed during Design and Validation phases.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design validation on a small sample size from typical devices.
D	Those parameters are derived mainly from simulations.

3.2 Absolute maximum ratings

Table 4 describes the maximum ratings for the device. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Stress beyond the listed maxima, even momentarily, may affect device reliability or cause permanent damage to the device.

Table 4. Absolute maximum ratings

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
V_{DD_LV}	SR	D	Core voltage operating life range(1)	—	–0.3	—	1.4	V
$V_{DD\_LV\_BD}$	SR	D	Buddy device voltage operating life range(2)	—	–0.3	—	1.5	V
$V_{DD\_HV\_IO\_MAIN}$ $V_{DD\_HV\_IO\_JTAG}$ $V_{DD\_HV\_IO\_FLEX}$ $V_{DD\_HV\_IO\_BD}$ $V_{DD\_HV\_FLA}$	SR	D	I/O supply voltage(3)	—	–0.3	—	6.0	V
$V_{SS\_HV\_ADV}$	SR	D	ADC ground voltage	Reference to digital ground	–0.3	—	0.3	V
$V_{DD\_HV\_ADV}$	SR	D	ADC Supply voltage(3)	Reference to $V_{SS\_HV\_ADV}$	–0.3	—	6.0	V
$V_{SS\_HV\_ADR\_D}$	SR	D	SD ADC ground reference	—	–0.3	—	0.3	V
$V_{DD\_HV\_ADR\_D}$	SR	D	SD ADC voltage reference(3)	Reference to $V_{SS\_HV\_ADR\_D}$	–0.3	—	6.0	V
V_{SS}-$V_{SS\_HV\_ADR\_D}$	SR	D	$V_{SS\_HV\_ADR\_D}$ differential voltage	—	–0.3	—	0.3	V
$V_{SS\_HV\_ADR\_S}$	SR	D	SAR ADC ground reference	—	–0.3	—	0.3	V
$V_{DD\_HV\_ADR\_S}$	SR	D	SAR ADC voltage reference(3)	Reference to $V_{SS\_HV\_ADR\_S}$	–0.3	—	6.0	V
V_{SS}-$V_{SS\_HV\_ADR\_S}$	SR	D	$V_{SS\_HV\_ADR\_S}$ differential voltage	—	–0.3	—	0.3	V
V_{SS}-$V_{SS\_HV\_ADV}$	SR	D	$V_{SS\_HV\_ADV}$ differential voltage	—	–0.3	—	0.3	V

Table 4. Absolute maximum ratings (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
V_{IN}	SR	D	I/O input voltage range(3)(4) (5)	—	–0.3	—	6.0	V
				Relative to V_{ss}	–0.3	—	—	
				Relative to $V_{DD\_HV\_IO}$ and $V_{DD\_HV\_ADV}$	—	—	0.3	
T_{TRIN}	SR	D	Digital Input pad transition time(6)	—	—	—	1	ms
I_{INJ}	SR	T	Maximum DC injection current for each analog/digital PAD(7)	—	–5	—	5	mA
T_{STG}	SR	T	Maximum non-operating Storage temperature range	—	–55	—	125	°C
T_{PAS}	SR	C	Maximum non-operating temperature during passive lifetime	—	–55	—	150(8)	°C
$T_{STORAGE}$	SR	—	Maximum storage time, assembled part programmed in ECU	No supply; storage temperature in range –40 °C to 60 °C	—	—	20	years
T_{SDR}	SR	T	Maximum solder temperature Pb-free packaged(9)	—	—	—	260	°C
MSL	SR	T	Moisture sensitivity level(10)	—	—	—	3	—
T_{XRAY} dose	SR	T	Maximum cumulated XRAY dose	Typical range for X-rays source during inspection:80 ÷ 130 KV; 20 ÷ 50 µA	—	—	1	grey

1. V_{DD_LV}: allowed 1.335 V - 1.400 V for 60 seconds cumulative time at the given temperature profile. Remaining time allowed 1.260 V - 1.335 V for 10 hours cumulative time at the given temperature profile. Remaining time as defined in *Section 3.3: Operating conditions*. In the range [1.26-1.33] V and if the above-mentioned cumulative times are not exceeded, the device functionality is granted and is expected to receive a flag by the internal HVD134 monitors to warn that the regulator (internal or external), providing the VDD_LV supply, exited the expected operating conditions. If the internal HVD134 monitors are disabled by the application, then an external voltage monitor with equivalent thresholds measured at the device pad, has to be implemented. Please refer to *Section 3.16.3: Voltage monitors* for the list of available internal monitors and to the Reference Manual for the configurability of the monitors. In this range, the device may exceed the maximum consumptions reported in *Table 9: Device consumption*.
2. $V_{DD\_LV\_BD}$: allowed 1.450 V - 1.500 V for 60 seconds cumulative time at the given temperature profile. Remaining time allowed 1.375 V - 1.450 V for 10 hours cumulative time at maximum T_J = 125 °C. Remaining time as defined in *Section 3.3: Operating conditions*.
3. V_{DD_HV}: allowed 5.5 V – 6.0 V for 60 seconds cumulative time at the given temperature profile, for 10 hours cumulative time with the device in reset at the given temperature profile. Remaining time as defined in *Section 3.3: Operating conditions*.
4. The maximum input voltage on an I/O pin tracks with the associated I/O supply maximum. For the injection current condition on a pin, the voltage will be equal to the supply plus the voltage drop across the internal ESD diode from I/O pin to supply. The diode voltage varies greatly across process and temperature, but a value of 0.3 V can be used for nominal calculations.
5. Relative value can be exceeded if design measures are taken to ensure injection current limitation (parameter IINJ).
6. This limitation applies to pads with digital input buffer enabled. If the digital input buffer is disabled, there are no maximum limits to the transition time.
7. The limits for the sum of all normal and injected currents on all pads within the same supply segment can be found in *Section 3.8.3: I/O pad current specifications*.
8. 175°C are allowed for limited time. Mission profile with passive lifetime temperature >150°C have to be evaluated by ST to confirm that are granted by product qualification.
9. Solder profile per IPC/JEDEC J-STD-020D.
10. Moisture sensitivity per JDEC test method A112.

3.3 Operating conditions

Table 5 describes the operating conditions for the device, and for which all the specifications in the data sheet are valid, except where explicitly noted. The device operating conditions must not be exceeded or the functionality of the device is not guaranteed.

Table 5. Operating conditions

Symbol		C	Parameter	Conditions	Value(1)			Unit
					Min	Typ	Max	
F_{SYS}(2)	SR	P	Operating system clock frequency(3)	—	—	—	200	MHz
$T_{J\_140\ Grade}$	SR	C	Operating Junction temperature	—	–40	—	165	°C
$T_{J\_125\ Grade}$	SR	P	Operating Junction temperature	—	–40	—	150	°C
$T_{A\_140\ Grade}$	SR	C	Operating Ambient temperature	—	–40	—	140	°C
$T_{A\_125\ Grade}$	SR	P	Operating Ambient temperature	—	–40	—	125	°C
V_{DD_LV}	SR	P	Core supply voltage(4)	—	1.14(5)	1.20	1.26(6) (7)	V
$V_{DD\_LV\_BD}$	SR	P	Buddy core supply voltage	—	1.20	—	1.32	V
$V_{DD\_HV\_IO\_MAIN}$ $V_{DD\_HV\_IO\_JTAG}$ $V_{DD\_HV\_IO\_FLEX}$ $V_{DD\_HV\_FLA}$ $V_{DD\_HV\_IO\_BD}$	SR	P	IO supply voltage	—	3.0	—	5.5	V
$V_{DD\_HV\_ADV}$	SR	P	ADC supply voltage	—	3.0(8)	—	5.5	V
$V_{SS\_HV\_ADV}$- V_{SS}	SR	D	ADC ground differential voltage	—	–25	—	25	mV
$V_{DD\_HV\_ADR\_D}$	SR	P	SD ADC supply reference voltage	—	3.0(8)	—	5.5	V
$V_{DD\_HV\_ADR\_D}$- $V_{DD\_HV\_ADV}$	SR	D	SD ADC reference differential voltage	—	—	—	25	mV

Table 5. Operating conditions (continued)

Symbol		C	Parameter	Conditions	Value(1)			Unit
					Min	Typ	Max	
$V_{SS\_HV\_ADR\_D}$	SR	P	SD ADC ground reference voltage	—	$V_{SS\_HV\_ADV}$			V
$V_{SS\_HV\_ADR\_D}$-$V_{SS\_HV\_ADV}$	SR	D	$V_{SS\_HV\_ADR\_D}$ differential voltage	—	–25	—	25	mV
$V_{DD\_HV\_ADR\_S}$	SR	P	SAR ADC reference voltage	—	3.0	—	5.5	V
$V_{DD\_HV\_ADR\_S}$-$V_{DD\_HV\_ADV}$	SR	D	SAR ADC reference differential voltage	—	$V_{DD\_HV\_ADV}$ -10%	—	25	mV
$V_{SS\_HV\_ADR\_S}$	SR	P	SAR ADC ground reference voltage	—	$V_{SS\_HV\_ADV}$			V
$V_{SS\_HV\_ADR\_S}$-$V_{SS\_HV\_ADV}$	SR	D	$V_{SS\_HV\_ADR\_S}$ differential voltage	—	–25	—	25	mV
V_{RAMP_LV}	SR	D	Slew rate on core power supply pins	V_{DD_LV} $V_{DD\_LV\_BD}$	—	—	20	V/ms
V_{RAMP_HV}	SR	D	Slew rate on HV power supply	—	—	—	100	V/ms
V_{IN}	SR	P	I/O input voltage range	—	0	—	5.5	V
I_{INJ1}	SR	T	DC Injection current (per pin) without performance degradation(9) (10) (11)	Digital pins and analog pins	–3.0	—	3.0	mA
I_{INJ2}	SR	D	Dynamic Injection current (per pin) with performance degradation(11) (12)	Digital pins and analog pins	–10	—	10	mA

1. The ranges in this table are design targets and actual data may vary in the given range.
2. The maximum number of PRAM wait states has to be configured accordingly to the system clock frequency. Refer to *Table 6*.

3. Maximum operating frequency is applicable to the cores and platform of the device. See the Clock Chapter in the Microcontroller Reference Manual for more information on the clock limitations for the various IP blocks on the device.
4. Core voltage as measured on device pin to guarantee published silicon performance.
5. In the range [1.14-1.08]V, the device functionality and specifications are granted and the device is expected to receive a flag by the internal LVD100 monitors to warn that the regulator (internal or external), providing the V_{DD_LV} supply, exited the expected operating conditions. If the internal LVD100 monitors are disabled by the application, then an external voltage monitor with minimum threshold of V_{DD_LV}(min) = 1.08 V measured at the device pad, has to be implemented. Refer to *Section 3.16.3: Voltage monitors* for the list of available internal monitors and to the Reference Manual for the configurability of the monitors.
6. Core voltage can exceed 1.26 V with the limitations provided in *Section 3.2: Absolute maximum ratings*, provided that HVD134_C monitor reset is disabled.
7. 1.260 V - 1.290 V range allowed periodically for supply with sinusoidal shape and average supply value below or equal to 1.236 V at the given temperature profile.
8. S/D ADC is functional in the range 3.0 V < $V_{DD\_HV\_ADV}$ < 4.0 V and 3.0 V < $V_{DD\_HV\_ADR\_D}$ < 4.0 V, but precision of conversion is not guaranteed.
9. Full device lifetime. I/O and analog input specifications are only valid if the injection current on adjacent pins is within these limits. See *Section 3.2: Absolute maximum ratings* for maximum input current for reliability requirements.
10. The I/O pins on the device are clamped to the I/O supply rails for ESD protection. When the voltage of the input pins is above the supply rail, current will be injected through the clamp diode to the supply rails. For external RC network calculation, assume typical 0.3 V drop across the active diode. The diode voltage drop varies with temperature.
11. The limits for the sum of all normal and injected currents on all pads within the same supply segment can be found in *Section 3.8.3: I/O pad current specifications*.
12. Positive and negative Dynamic current injection pulses are allowed up to this limit, with different specifications for I/O, ADC accuracy and analog input. See the dedicated chapters for the different specification limits. See the Absolute Maximum Ratings table for maximum input current for reliability requirements. Refer to the following pulses definitions: Pulse1 (ISO 7637-2:2011), Pulse 2a(ISO 7637-2:2011 5.6.2), Pulse 3a (ISO 7637-2:2011 5.6.3), Pulse 3b (ISO 7637-2:2011 5.6.3).

Table 6. PRAM wait states configuration

PRAMC WS	Clock Frequency (MHz)
1	≤ 200
0	≤ 120

3.3.1 Power domains and power up/down sequencing

The following table shows the constraints and relationships for the different power domains. Supply1 (on rows) can exceed Supply2 (on columns), only if the cell at the given row and column is reporting ‘ok’. This limitation is valid during power-up and power-down phases, as well as during normal device operation.

Table 7. Device supply relation during power-up/power-down sequence

		Supply2							
		V_{DD_LV}	**$V_{DD\_HV\_IO\_FLEX}$**	**$V_{DD\_HV\_IO\_JTAG}$**	**$V_{DD\_HV\_IO\_MAIN}$ $V_{DD\_HV\_FLA}$**	**$V_{DD\_HV\_ADV}$**	**$V_{DD\_HV\_ADR}$**	**$V_{DD\_LV\_BD}$**	**$V_{DD\_HV\_BD}$**
Supply1	V_{DD_LV}(1)		ok	ok	ok	ok	ok	ok	ok
	$V_{DD\_HV\_IO\_FLEX}$	ok		ok	not allowed	ok	ok	ok	ok
	$V_{DD\_HV\_IO\_JTAG}$	ok	ok		not allowed	ok	ok	ok	ok
	$V_{DD\_HV\_IO\_MAIN}$ $V_{DD\_HV\_FLA}$	ok	ok	ok		ok	ok	ok	ok
	$V_{DD\_HV\_ADV}$	ok	ok	ok	not allowed		ok	ok	ok
	$V_{DD\_HV\_ADR}$	ok	ok	ok	not allowed	not allowed		ok	ok
	$V_{DD\_LV\_BD}$	ok	ok	ok	ok	ok	ok		ok
	$V_{DD\_HV\_BD}$	ok	ok	ok	ok	ok	ok	ok	

1. V_{DD_LV} can be higher than V_{DD_HV} supplies only during power-up/down transient ramps, in case of external LV regulator and if V_{DD_HV} supply voltage level is lower than V_{DD_LV} allowed max operating condition.

During power-up, all functional terminals are maintained in a known state as described in the device pinout Microsoft Excel file attached to the IO_Definition document.

3.4 Electrostatic discharge (ESD)

The following table describes the ESD ratings of the device:

- All ESD testing are in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits,
- Device failure is defined as: “If after exposure to ESD pulses, the device does not meet the device specification requirements, which include the complete DC parametric and functional testing at room temperature and hot temperature, maximum DC parametric variation within 10% of maximum specification”.

Table 8. ESD ratings

Parameter	C	Conditions	Value	Unit
ESD for Human Body Model (HBM)(1)	T	All pins	2000	V
ESD for field induced Charged Device Model (CDM)(2)	T	All pins	500	V
	T	Corner Pins	750	V

1. This parameter tested in conformity with ANSI/ESD STM5.1-2007 Electrostatic Discharge Sensitivity Testing.
2. This parameter tested in conformity with ANSI/ESD STM5.3-1990 Charged Device Model - Component Level.

3.5 Electromagnetic compatibility characteristics

EMC measurements at IC-level IEC standards are available from STMicroelectronics on request.

3.6 Temperature profile

The device is qualified in accordance to AEC-Q100 Grade1 requirements, such as HTOL 1,000 h and HTDR 1,000 hrs, T_J = 150 °C.

Mission profile with junction Temperature higher than 150 °C and up to 165 °C have to be evaluated by ST to confirm to be granted by product qualification. Please contact your STMicroelectronics Sales representative for validation.

3.7 Device consumption

Table 9. Device consumption

Symbol		C	Parameter	Conditions	Value(1)			Unit
					Min	Typ	Max	
I_{DD_LKG}(2),(3)	CC	C	Leakage current on the V_{DD_LV} supply	T_J = 40 °C	—	—	45	mA
		D		T_J = 120 °C	—	—	190	
		P		T_J = 150 °C	—	—	340	
		D		T_J = 165 °C	—	—	550	
I_{DD_LV}(3)	CC	P	Dynamic current on the V_{DD_LV} supply, very high consumption profile(4)	—	—	—	530	mA
I_{DD_HV}	CC	P	Total current on the V_{DD_HV} supply(4)	f_{MAX}	—	—	93	mA
$I_{DD\_MAIN\_CORE\_AC}$	CC	T	Main Core dynamic current(5)	f_{MAX}	—	—	55	mA
$I_{DD\_CHKR\_CORE\_AC}$	CC	T	Checker Core dynamic operating current	f_{MAX}	—	—	35	mA
$I_{DD\_HSM\_AC}$	CC	T	HSM platform dynamic operating current(6)	$f_{MAX}/2$	—	—	23	mA
$I_{DD\_AMU\_AC}$	CC	T	AMU dynamic operating current(7)	f_{MAX}	—	—	20	mA
I_{DDSTOP}(8)	CC	T	Dynamic current on the V_{DD_LV} supply +Total current on the V_{DD_HV} supply	—	—	21	50	mA
$I_{DD\_LV\_BD}$	CC	P	Buddy Device Consumption on V_{DD_LV} supply(9)	T_J = 150 °C	—	—	500	mA
		D		T_J = 165 °C	—	—	600	
$I_{DD\_HV\_BD}$	CC	T	Buddy Device Consumption on V_{DD_HV} supply(9)	—	—	—	130	mA
I_{SPIKE}	CC	T	Maximum short term current spike(10)	< 20 µs observation window	—	—	100	mA
dI	SR	D	Current difference ratio to average current (dI/avg(I))(11)	20 µs observation window	—	—	20	%
I_{SR}(12)	CC	D	Current variation during power up/down	See footnote(13)	—	—	200	mA
I_{DDOFF}	CC	T	Power-off current on high voltage supply rails(14)	V_{DD_HV} = 2.5 V	100	—	—	µA

1. The ranges in this table are design targets and actual data may vary in the given range.

2. The leakage considered is the sum of core logic and RAM memories. The contribution of analog modules is not considered, and they are computed in the dynamic I_{DD_LV} and I_{DD_HV} parameters.
3. I_{DD_LKG} (leakage current) and I_{DD_LV} (dynamic current) are reported as separate parameters, to give an indication of the consumption contributors. The tests used in validation, characterization and production are verifying that the total consumption (leakage+dynamic) is lower or equal to the sum of the maximum values provided (I_{DD_LKG}+I_{DD_LV}). The two parameters, measured separately, may exceed the maximum reported for each, depending on the operative conditions and the software profile used.
4. Use case: 3 x e200Z4 @200 MHz with all locksteps on, HSM @100 MHz, all IPs clock enabled, all SARADC and SDADC in continuous conversion, DMA continuously triggered by ADC conversion, GTM @ 200 MHz (16 TOM channels, 4 ATOM, 4 TIM, DPLL, TBU), 4 CAN / 6 DSPI / PSI5, PLL0-1 running.
5. Dynamic consumption of one core, including the dedicated I/D-caches and I/D-MEMS contribution.
6. Dynamic consumption of the HSM module, including the dedicated memories, during the execution of Electronic Code Book crypto algorithm on 1 block of 16 byte of shared RAM.
7. Dynamic consumption of the AMU module standalone.
8. Sysclk = RC16 MHz, RC16 MHz ON, RC1 MHz ON, PLL OFF. All possible peripherals off and clock gated. Flash in power down mode.
9. Worst case usage (data trace, data overlay, full Aurora utilization). If Aurora and JTAGM/LFAST not used, $V_{DD\_LV\_BD}$ current is reduced by ~20mA.
10. Current spike may occur during normal operation that are above average current, valid for an application running and if the following conditions are unchanged: clock configuration, frequency and gating; peripherals activation and configuration; number of cores and checker-cores activation and configuration; no functional/destructive reset occurring; no mbist/lbist execution. An internal auxiliary and clamp regulator can be enabled, in order to support internal current variations. Please refer to the Power Management chapter for the details and the external component requirements.
11. Moving window, measured on application specific pattern, with a maximum of 100 mA for the worst case application.
12. This specification is the maximum value and is a boundary for the dI specification.
13. Condition1: For power on period from 0 V up to normal operation with reset asserted. Condition 2: From reset asserted until PLL running free. Condition 3: Increasing PLL from free frequency to full frequency. Condition 4: reverse order for power down to 0 V. Internal schemes must be used by the application (example: frequency ramping feature enable) to ensure that incremental demands are made on the external power supply within the maximum value. Mbist/Lbist must be configured to avoid exceeding the maximum value.
14. I_{DDOFF} is the minimum guaranteed consumption of the device during power-up. It can be used to correctly size power-off ballast in case of current injection during power-off state.

3.8 I/O pad specification

The following table describes the different pad type configurations.

Table 10. I/O pad specification descriptions

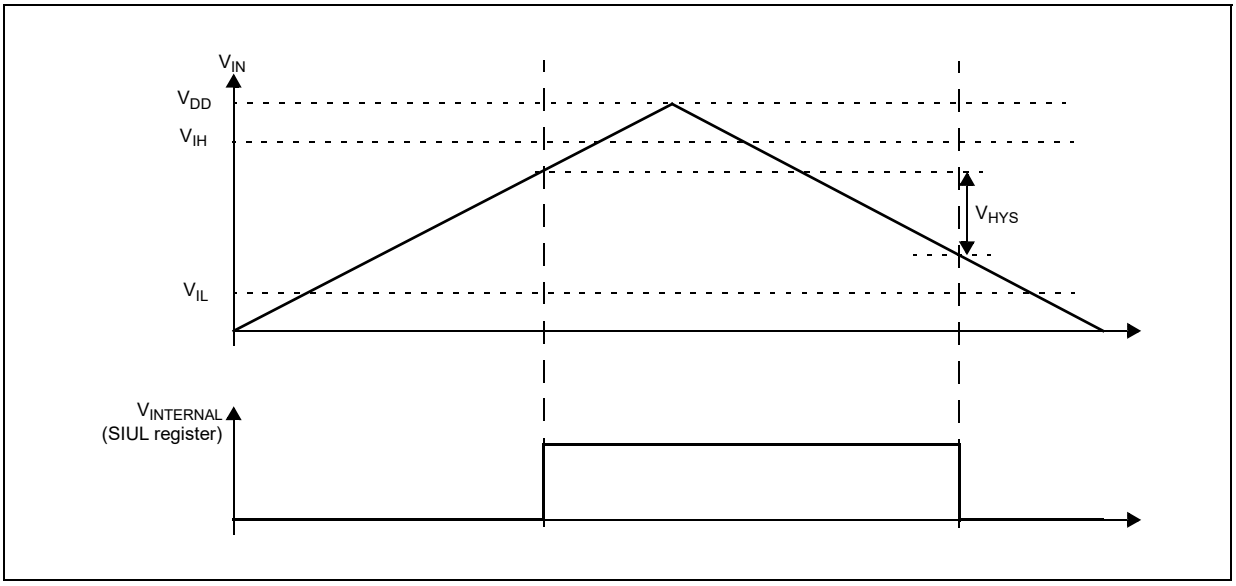
Pad type	Description
Weak configuration	Provides a good compromise between transition time and low electromagnetic emission.
Medium configuration	Provides transition fast enough for the serial communication channels with controlled current to reduce electromagnetic emission.
Strong configuration	Provides fast transition speed; used for fast interface.
Very strong configuration	Provides maximum speed and controlled symmetric behavior for rise and fall transition. Used for fast interface including Ethernet and FlexRay interfaces requiring fine control of rising/falling edge jitter.
Differential configuration	A few pads provide differential capability providing very fast interface together with good EMC performances.
Input only pads	These low input leakage pads are associated with the ADC channels.

Note: Each I/O pin on the device supports specific drive configurations. See the signal description table in the device reference manual for the available drive configurations for each I/O pin. PMC_DIG_VSIO register has to be configured to select the voltage level (3.3 V or 5.0 V) for each IO segment.

3.8.1 I/O input DC characteristics

The following table provides input DC electrical characteristics, as described in *Figure 3*.

Figure 3. I/O input electrical characteristics



In the following table, in case of current injection pulses on one pad under the conditions and limits described in I_{INJ2} parameter in *Section 3.3: Operating conditions*, other pads of

the same supply segment will have a drift of 4 % above the maximum V_{il} and 4 % below the minimum V_{ih} limits. Similarly V_{hys} parameter will be decreased of 4 %.

Table 11. I/O input electrical characteristics

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
TTL								
V_{ihttl}	SR	P	Input high level TTL	—	2	—	$V_{DD\_HV\_IO}$ + 0.3	V
V_{ilttl}	SR	P	Input low level TTL	—	–0.3	—	0.8	V
V_{hysttl}	CC	C	Input hysteresis TTL	—	0.3	—	—	V
AUTOMOTIVE								
V_{ihaut}(1)	SR	P	Input high level AUTO	$V_{DD\_HV\_IO}$ = 5.0 V ± 10%	3.8	—	$V_{DD\_HV\_IO}$ + 0.3	V
V_{ilaut}(2)	SR	P	Input low level AUTO	$V_{DD\_HV\_IO}$ = 5.0 V ± 10%	–0.3	—	2.2	V
V_{hysaut}(3)	CC	C	Input hysteresis AUTO	$V_{DD\_HV\_IO}$ = 5.0 V ± 10%	0.5	—	—	V
CMOS								
V_{ihcmos}	SR	P	Input high level CMOS(1)	—	0.65 * V_{DD}	—	$V_{DD\_HV\_IO}$ + 0.3	V
V_{ihcmos} BD	SR	T	Input high level CMOS	Buddy Device, hysteresis on	0.65 * $V_{DD\_HV\_IO}$	—	$V_{DD\_HV\_IO}$ + 0.3	V
				Buddy Device, hysteresis off	0.60 * $V_{DD\_HV\_IO}$	—	$V_{DD\_HV\_IO}$ + 0.3	V
V_{ilcmos}	SR	P	Input low level CMOS	—	–0.3	—	0.35 * V_{DD}	V
$V_{hyscmos}$	CC	C	Input hysteresis CMOS	—	0.10 * V_{DD}	—	—	V
COMMON								
I_{LKG}	CC	P	Pad input leakage	INPUT-ONLY pads T_J = 150 °C	—	—	200	nA
I_{LKG}	CC	C	Pad input leakage	INPUT-ONLY pads T_J = 165 °C	—	—	270	nA
I_{LKG}	CC	P	Pad input leakage	MEDIUM pads T_J = 150 °C	—	—	360	nA
I_{LKG}	CC	C	Pad input leakage	MEDIUM pads T_J = 165 °C	—	—	500	nA
I_{LKG}	CC	P	Pad input leakage	STRONG pads T_J = 150 °C	—	—	1,000	nA

Table 11. I/O input electrical characteristics (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
I_{LKG}	CC	C	Pad input leakage	STRONG pads T_J = 165 °C	—	—	1,500	nA
I_{LKG}	CC	P	Pad input leakage	VERY STRONG pads, T_J = 150 °C	—	—	1,000	nA
I_{LKG}	CC	C	Pad input leakage	VERY STRONG pads, T_J = 165 °C	—	—	2,000	nA
C_{P1}	CC	D	Pad capacitance	—	—	—	10	pF
V_{drift}	CC	D	Input V_{il}/V_{ih} temperature drift	In a 1 ms period, with a temperature variation <30 °C	—	—	100	mV
W_{FI}	SR	C	Wakeup input filtered pulse(4)	—	—	—	20	ns
W_{NFI}	SR	C	Wakeup input not filtered pulse(4)	—	400	—	—	ns

1. Good approximation of the variation of the minimum value with supply is given by formula: 5 V range: $V_{IHAUT} = 0.69 \times V_{DD\_HV\_IO}$; 3.3 V range: $V_{IHAUT} = 0.75 \times V_{DD\_HV\_IO}$
2. Good approximation of the variation of the maximum value with supply is given by formula: 5 V range: $V_{ILAUT} = 0.49 \times V_{DD\_HV\_IO}$; 3.3 V range: $V_{ILAUT} = 0.35 \times V_{DD\_HV\_IO}$
3. Good approximation of the variation of the minimum value with supply is given by formula: 5 V and 3.3 V range: $V_{HYSAUT} = 0.11 \times V_{DD\_HV\_IO}$
4. In the range from W_{FI} (max) to W_{NFI} (min), pulses can be filtered or not filtered, according to operating temperature and voltage. Refer to the device pinout IO definition excel file for the list of pins supporting the wakeup filter feature.

Table 12. I/O pull-up/pull-down electrical characteristics

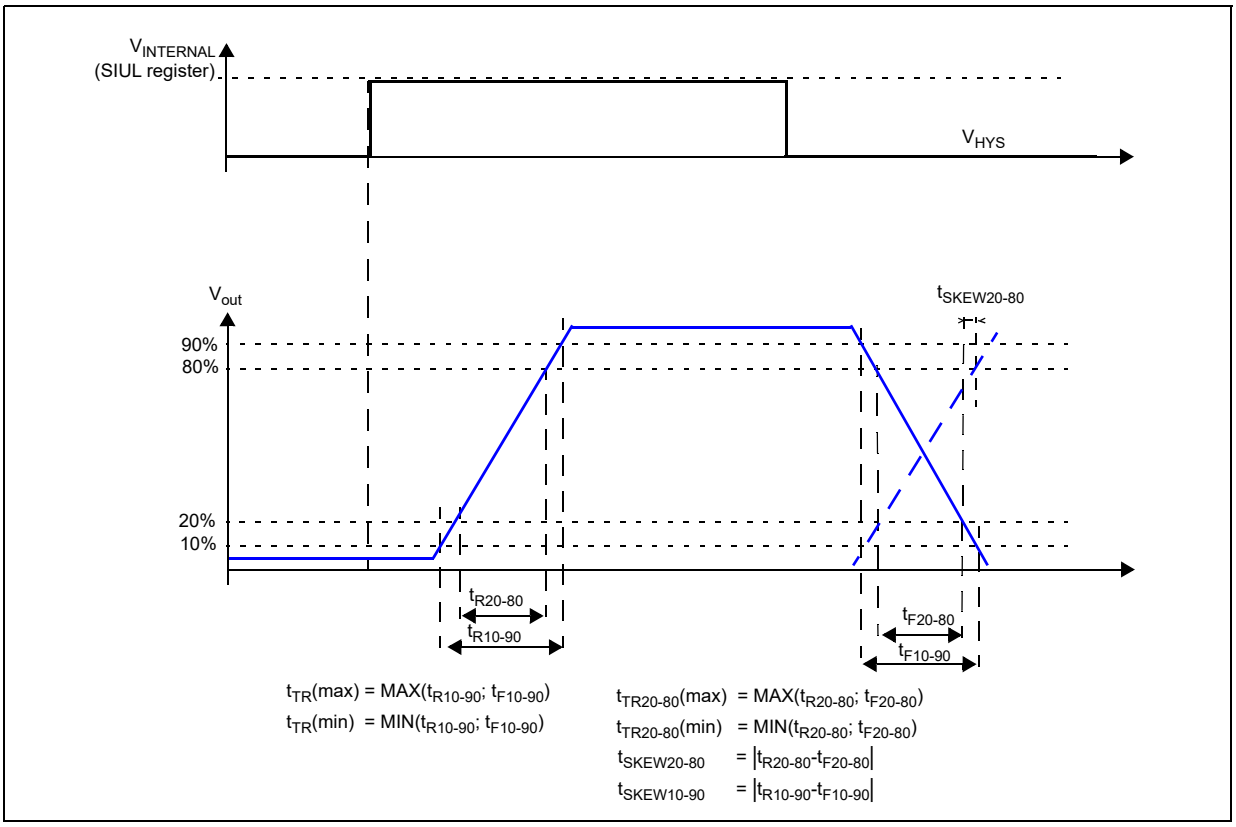
Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
I_{WPU}	CC	T	Weak pull-up current absolute value	V_{IN} = 1.1 V(1)	—	—	130	µA
		P		V_{IN} = 0.69 * $V_{DD\_HV\_IO}$(2)	15	—	—	
R_{WPU}	CC	D	Weak Pull-up resistance	$V_{DD\_HV\_IO}$ = 5.0 V ± 10%	33	—	93	KΩ
I_{WPD}	CC	T	Weak pull-down current absolute value	V_{IN} = 0.69 * $V_{DD\_HV\_IO}$(1)	—	—	130	µA
		P		V_{IN} = 0.9 V(2)	15	—	—	
R_{WPD}	CC	D	Weak Pull-down resistance	$V_{DD\_HV\_IO}$ = 5.0 V ± 10%	29	—	60	KΩ

1. Maximum current when forcing a change in the pin level opposite to the pull configuration.
2. Minimum current when keeping the same pin level state than the pull configuration.

3.8.2 I/O output DC characteristics

Figure 4 provides description of output DC electrical characteristics.

Figure 4. I/O output DC electrical characteristics definition



The following tables provide DC characteristics for bidirectional pads:

- *Table 13* provides output driver characteristics for I/O pads when in WEAK/SLOW configuration.
- *Table 14* provides output driver characteristics for I/O pads when in MEDIUM configuration.
- *Table 15* provides output driver characteristics for I/O pads when in STRONG/FAST configuration.
- *Table 16* provides output driver characteristics for I/O pads when in VERY STRONG/VERY FAST configuration.

Note: 10%/90% is the default condition for any parameter if not explicitly mentioned differently.

Table 13. WEAK/SLOW I/O output characteristics

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
V_{ol_W}	CC	D	Output low voltage for Weak type PADs	I_{ol} = 0.5 mA V_{DD} = 5.0 V ± 10% V_{DD} = 3.3 V ± 10%	—	—	0.1*V_{DD}	V
V_{oh_W}	CC	D	Output high voltage for Weak type PADs	Ioh = 0.5 mA V_{DD} = 5.0 V ± 10% V_{DD} = 3.3 V ± 10%	0.9*V_{DD}	—	—	V
$R_{\_W}$	CC	P	Output impedance for Weak type PADs	V_{DD} = 5.0 V ± 10%	380	—	1040	Ω
				V_{DD} = 3.3 V ± 10%	250	—	700	
F_{max_W}	CC	T	Maximum output frequency for Weak type PADs	CL = 25 pF V_{DD} = 5.0 V ± 10% V_{DD} = 3.3 V ± 10%	—	—	2	MHz
				CL = 50 pF V_{DD} = 5.0 V ± 10% V_{DD} = 3.3 V ± 10%	—	—	1	MHz
t_{TR_W}	CC	T	Transition time output pin weak configuration, 10%-90%	CL = 25 pF V_{DD} = 5.0 V + 10% V_{DD} = 3.3 V + 10%	25	—	120	ns
				CL = 50 pF V_{DD} = 5.0 V ± 10 % V_{DD} = 3.3 V ± 10 %	50	—	240	ns
$\lvert t_{SKEW\_W} \rvert$	CC	T	Difference between rise and fall time, 90%-10%	—	—	—	25	%
I_{DCMAX_W}	CC	D	Maximum DC current	V_{DD} = 5.0 V ± 10% V_{DD} = 3.3 V ± 10%	—	—	0.5	mA

Table 14. MEDIUM I/O output characteristics

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
V_{ol_M}	CC	D	Output low voltage for Medium type PADs	I_{ol} = 2.0 mA V_{DD} =5.0 V ± 10 % V_{DD} =3.3 V ± 10 %	—	—	0.1*V_{DD}	V
V_{oh_M}	CC	D	Output high voltage for Medium type PADs	I_{oh}=2.0 mA V_{DD} = 5.0 V ± 10% V_{DD} = 3.3 V ± 10%	0.9*V_{DD}	—	—	V

Table 14. MEDIUM I/O output characteristics (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
$R_{\_M}$	CC	P	Output impedance for Medium type PADs	V_{DD} = 5.0 V ± 10%	90	—	260	Ω
				V_{DD} = 3.3 V ± 10%	60	—	170	
F_{max_M}	CC	T	Maximum output frequency for Medium type PADs	CL = 25 pF V_{DD} = 5.0 V ± 10% V_{DD} = 3.3 V ± 10%	—	—	12	MHz
				CL = 50 pF V_{DD} = 5.0 V ± 10 % V_{DD} = 3.3 V ± 10 %	—	—	6	MHz
t_{TR_M}	CC	T	Transition time output pin MEDIUM configuration, 10%-90%	CL = 25 pF V_{DD} = 5.0 V ± 10% V_{DD} = 3.3 V ± 10%	8	—	30	ns
				CL = 50 pF V_{DD} = 5.0 V ± 10% V_{DD} = 3.3 V ± 10%	12	—	60	ns
$\lvert t_{SKEW\_M} \rvert$	CC	T	Difference between rise and fall time, 90%-10%	—	—	—	25	%
I_{DCMAX_M}	CC	D	Maximum DC current	V_{DD} = 5.0 V ± 10% V_{DD} = 3.3 V ± 10%	—	—	2	mA

Table 15. STRONG/FAST I/O output characteristics

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
V_{ol_S}	CC	D	Output low voltage for Strong type PADs	I_{ol} = 8.0 mA V_{DD} = 5.0 V ± 10%	—	—	$0.1*V_{DD}$	V
				I_{ol} = 5.5 mA V_{DD} =3 .3 V ± 10%	—	—	$0.15*V_{DD}$	V
V_{oh_S}	CC	D	Output high voltage for Strong type PADs	I_{oh} = 8.0 mA V_{DD} = 5.0 V ± 10%	$0.9*V_{DD}$	—	—	V
				I_{oh} = 5.5 mA V_{DD} = 3.3 V ± 10%	$0.85*V_{DD}$	—	—	V
$R_{\_S}$	CC	P	Output impedance for Strong type PADs	V_{DD} = 5.0 V ± 10%	20	—	65	Ω
				V_{DD} = 3.3 V ± 10%	28	—	90	

Table 15. STRONG/FAST I/O output characteristics (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
F_{max_S}	CC	T	Maximum output frequency for Strong type PADs	CL = 25 pF V_{DD}=5.0 V ± 10%	—	—	50	MHz
				CL = 50 pF V_{DD}=5.0 V ± 10%	—	—	25	MHz
				CL = 25 pF V_{DD} = 3.3 V ± 10%	—	—	25	MHz
				CL = 50 pF V_{DD} = 3.3 V ± 10%	—	—	12.5	MHz
t_{TR_S}	CC	T	Transition time output pin STRONG configuration, 10%-90%	CL = 25 pF V_{DD} = 5.0 V ± 10%	3	—	10	ns
				CL = 50 pF V_{DD} = 5.0 V ± 10%	5	—	16	
				CL = 25 pF V_{DD} = 3.3 V ± 10%	1.5	—	15	
				CL = 50 pF V_{DD} = 3.3 V ± 10%	2.5	—	26	
I_{DCMAX_S}	CC	D	Maximum DC current	V_{DD} = 5 V ± 10%	—	—	8	mA
				V_{DD} = 3.3 V ± 10%	—	—	5.5	
$\lvert t_{SKEW\_S} \rvert$	CC	T	Difference between rise and fall time, 90%-10%	—	—	—	25	%

Table 16. VERY STRONG/VERY FAST I/O output characteristics

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
V_{ol_V}	CC	D	Output low voltage for Very Strong type PADs	I_{ol} = 9.0 mA V_{DD} =5.0 V ± 10%	—	—	0.1*V_{DD}	V
				I_{ol} = 9.0 mA V_{DD} =3.3 V ± 10%	—	—	0.15*V_{DD}	V
V_{oh_V}	CC	D	Output high voltage for Very Strong type PADs	I_{oh} = 9.0 mA V_{DD} = 5.0 V ± 10%	0.9*V_{DD}	—	—	V
				I_{oh} = 9.0 mA V_{DD} = 3.3 V ± 10%	0.85*V_{DD}	—	—	V
$R_{\_V}$	CC	P	Output impedance for Very Strong type PADs	V_{DD} = 5.0 V ± 10%	20	—	60	Ω
				V_{DD} = 3.3 V ± 10%	18	—	50	

Table 16. VERY STRONG/VERY FAST I/O output characteristics (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
F_{max_V}	CC	T	Maximum output frequency for Very Strong type PADs	CL = 25 pF V_{DD} = 5.0 V ± 10%	—	—	50	MHz
				CL = 50 pF V_{DD} = 5.0 V ± 10%	—	—	25	MHz
				CL = 25 pF V_{DD} = 3.3 V ± 10%	—	—	50	MHz
				CL = 50 pF V_{DD} = 3.3 V ± 10%	—	—	25	MHz
t_{TR_V}	CC	T	10–90% threshold transition time output pin VERY STRONG configuration	CL = 25 pF V_{DD} = 5.0 V ± 10%	1	—	6	ns
				CL = 50 pF V_{DD} = 5.0 V ± 10%	3	—	12	
				CL = 25 pF V_{DD} = 3.3 V ± 10%	1.5	—	6	
				CL = 50 pF V_{DD} = 3.3 V ± 10%	3	—	11	
$t_{TR20\text{-}80\_V}$	CC	T	20–80% threshold transition time output pin VERY STRONG configuration (Flexray Standard)	CL = 25 pF V_{DD} = 5.0 V ± 10%	0.8	—	4.5	ns
				CL = 15 pF V_{DD} = 3.3 V ± 10%	1	—	4.5	
t_{TRTTL_V}	CC	T	TTL threshold transition time for output pin in VERY STRONG configuration (Ethernet standard)	CL = 25 pF V_{DD} = 3.3 V ± 10%	0.88	—	5	ns
$\Sigma t_{TR20\text{-}80\_V}$	CC	T	Sum of transition time 20–80% output pin VERY STRONG configuration	CL = 25 pF V_{DD} = 5.0 V ± 10%	—	—	9	ns
				CL = 15 pF V_{DD} = 3.3 V ± 10%	—	—	9	
$\lvert t_{SKEW\_V} \rvert$	CC	T	Difference between rise and fall delay	CL = 25 pF V_{DD} = 5.0 V ± 10%	0	—	1.2	ns
I_{DCMAX_V}	CC	D	Maximum DC current	V_{DD} = 5.0 V±10% V_{DD} = 3.3 V ± 10%	—	—	9	mA

3.8.3 I/O pad current specifications

The I/O pads are distributed across the I/O supply segment. Each I/O supply segment is associated to a V_{DD}/V_{SS} supply pair as described in the device pinout Microsoft Excel file attached to the IO_Definition document.

Table 17 provides I/O consumption figures.

In order to ensure device reliability, the average current of the I/O on a single segment should remain below the I_{RMSSEG} maximum value.

In order to ensure device functionality, the sum of the dynamic and static current of the I/O on a single segment should remain below the I_{DYNSEG} maximum value.

Pad mapping on each segment can be optimized using the pad usage information provided on the I/O Signal Description table.

Note: In order to ensure the correct functionality for SENT, the sum of all pad usage ratio within the SENT segment should remain below 10%.

Table 17. I/O consumption

Symbol		C	Parameter	Conditions	Value(1)			Unit
					Min	Typ	Max	
Average consumption(2)								
I_{RMSSEG}	SR	D	Sum of all the DC I/O current within a supply segment	—	—	—	80	mA
I_{RMS_W}	CC	D	RMS I/O current for WEAK configuration	C_L = 25 pF, 2 MHz, V_{DD} = 5.0 V ± 10 %	—	—	1.1	mA
				C_L = 50 pF, 1 MHz, V_{DD} = 5.0 V ± 10 %	—	—	1.1	
				C_L = 25 pF, 2 MHz, V_{DD} = 3.3 V ± 10 %	—	—	1.0	
				C_L = 25 pF, 1 MHz, V_{DD} = 3.3 V ± 10%	—	—	1.0	
I_{RMS_M}	CC	D	RMS I/O current for MEDIUM configuration	C_L = 25 pF, 12 MHz, V_{DD} = 5.0 V ± 10%	—	—	5.5	mA
				C_L = 50 pF, 6 MHz, V_{DD} = 5.0 V ± 10%	—	—	5.5	
				C_L = 25 pF, 12 MHz, V_{DD} = 3.3 V ± 10%	—	—	4.2	
				C_L = 25 pF, 6 MHz, V_{DD} = 3.3 V ± 10%	—	—	4.2	

Table 17. I/O consumption (continued)

Symbol		C	Parameter	Conditions	Value(1)			Unit
					Min	Typ	Max	
I_{RMS_S}	CC	D	RMS I/O current for STRONG configuration	C_L = 25 pF, 50 MHz, V_{DD} = 5.0 V ± 10%	—	—	21	mA
				C_L = 50 pF, 25 MHz, V_{DD} = 5.0 V ± 10%	—	—	21	
				C_L = 25 pF, 25 MHz, V_{DD} = 3.3 V ± 10%	—	—	10	
				C_L = 25 pF, 12.5 MHz, V_{DD} = 3.3 V ± 10%	—	—	10	
I_{RMS_V}	CC	D	RMS I/O current for VERY STRONG configuration	C_L = 25 pF, 50 MHz, V_{DD} = 5.0 V ± 10%	—	—	23	mA
				C_L = 50 pF, 25 MHz, V_{DD} = 5.0 V ± 10%	—	—	23	
				C_L = 25 pF, 50 MHz, V_{DD} = 3.3 V ± 10%	—	—	16	
				C_L = 25 pF, 25 MHz, V_{DD} = 3.3 V ± 10%	—	—	16	
Dynamic consumption(3)								
I_{DYN_SEG}	SR	D	Sum of all the dynamic and DC I/O current within a supply segment	V_{DD} = 5.0 V ± 10%	—	—	195	mA
				V_{DD} = 3.3 V ± 10%	—	—	150	
I_{DYN_W}	CC	D	Dynamic I/O current for WEAK configuration	C_L = 25 pF, V_{DD} = 5.0 V ± 10%	—	—	16.7	mA
				C_L = 50 pF, V_{DD} = 5.0 V ± 10%	—	—	16.8	
				C_L = 25 pF, V_{DD} = 3.3 V ± 10%	—	—	12.9	
				C_L = 50 pF, V_{DD} = 3.3 V ± 10%	—	—	12.9	
I_{DYN_M}	CC	D	Dynamic I/O current for MEDIUM configuration	C_L = 25 pF, V_{DD} = 5.0 V ± 10%	—	—	18.2	mA
				C_L = 50 pF, V_{DD} = 5.0 V ± 10%	—	—	18.4	
				C_L = 25 pF, V_{DD} = 3.3 V ± 10%	—	—	14.3	
				C_L = 50 pF, V_{DD} = 3.3 V ± 10%	—	—	16.4	

Table 17. I/O consumption (continued)

Symbol		C	Parameter	Conditions	Value[1]			Unit
					Min	Typ	Max	
I_{DYN_S}	CC	D	Dynamic I/O current for STRONG configuration	C_L = 25 pF, V_{DD} = 5.0 V ± 10%	—	—	57	mA
				C_L = 50 pF, V_{DD} = 5.0 V ± 10%	—	—	63.5	
				C_L = 25 pF, V_{DD} = 3.3 V ± 10%	—	—	31	
				C_L = 50 pF, V_{DD} = 3.3 V ± 10%	—	—	33.5	
I_{DYN_V}	CC	D	Dynamic I/O current for VERY STRONG configuration	C_L = 25 pF, V_{DD} = 5.0 V ± 10%	—	—	62	mA
				C_L = 50 pF, V_{DD} = 5.0 V ± 10%	—	—	70	
				C_L = 25 pF, V_{DD} = 3.3 V ± 10%	—	—	52	
				C_L = 50 pF, V_{DD} = 3.3 V ± 10%	—	—	55	

1. I/O current consumption specifications for the 4.5 V $\leq V_{DD\_HV\_IO} \leq$ 5.5 V range are valid for VSIO_[VSIO_xx] = 1, and VSIO[VSIO_xx] = 0 for 3.0 V $\leq V_{DD\_HV\_IO} \leq$ 3.6 V.
2. Average consumption in one pad toggling cycle.
3. Stated maximum values represent peak consumption that lasts only a few ns during I/O transition. When possible (timed output) it is recommended to delay transition between pads by few cycles to reduce noise and consumption.

3.9 Reset pad (PORST, ESR0) electrical characteristics

The device implements dedicated bidirectional reset pins as below specified. $\overline{\text{PORST}}$ pin does not require active control. It is possible to implement an external pull-up to ensure correct reset exit sequence. Recommended value is 4.7 KΩ.

Figure 5. Startup Reset requirements

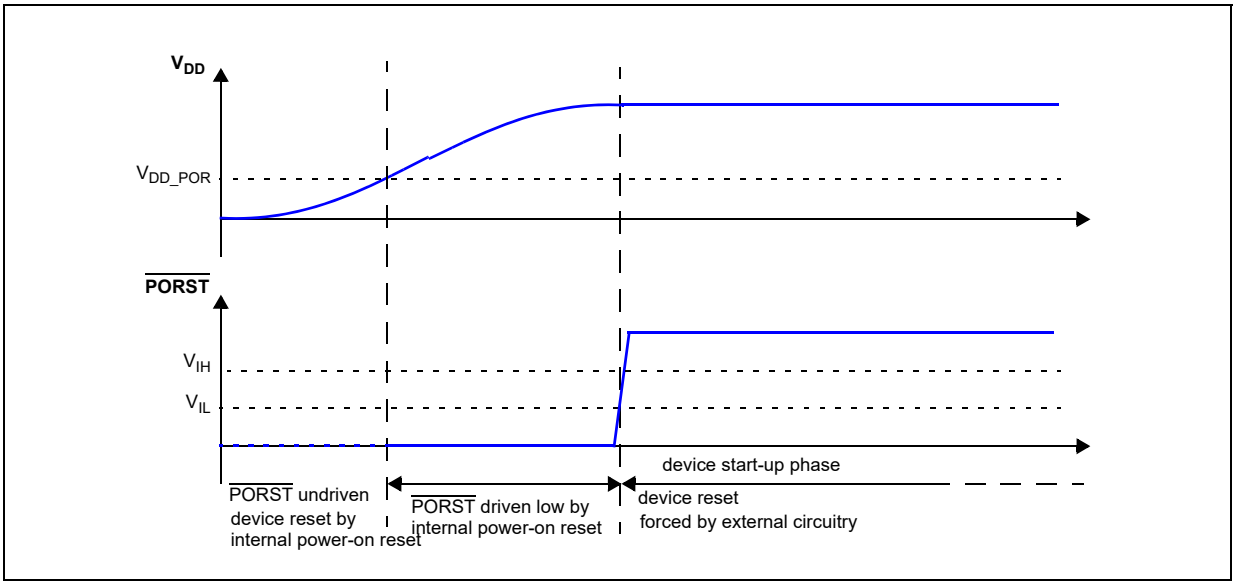


Figure 6 describes the device behavior depending on the supply signal on PORST:

1. $\overline{\text{PORST}}$ low pulse has too low amplitude: it is filtered by input buffer hysteresis. Device remains in current state.
2. $\overline{\text{PORST}}$ low pulse has too short duration: it is filtered by low pass filter. Device remains in current state.
3. $\overline{\text{PORST}}$ low pulse is generating a reset:
   a) $\overline{\text{PORST}}$ low but initially filtered during at least WFRST. Device remains initially in current state.
   b) $\overline{\text{PORST}}$ potentially filtered until WNFRST. Device state is unknown. It may either be reset or remains in current state depending on extra condition (temperature, voltage, device).
   c) $\overline{\text{PORST}}$ asserted for longer than WNFRST. Device is under reset.

Figure 6. Noise filtering on reset signal

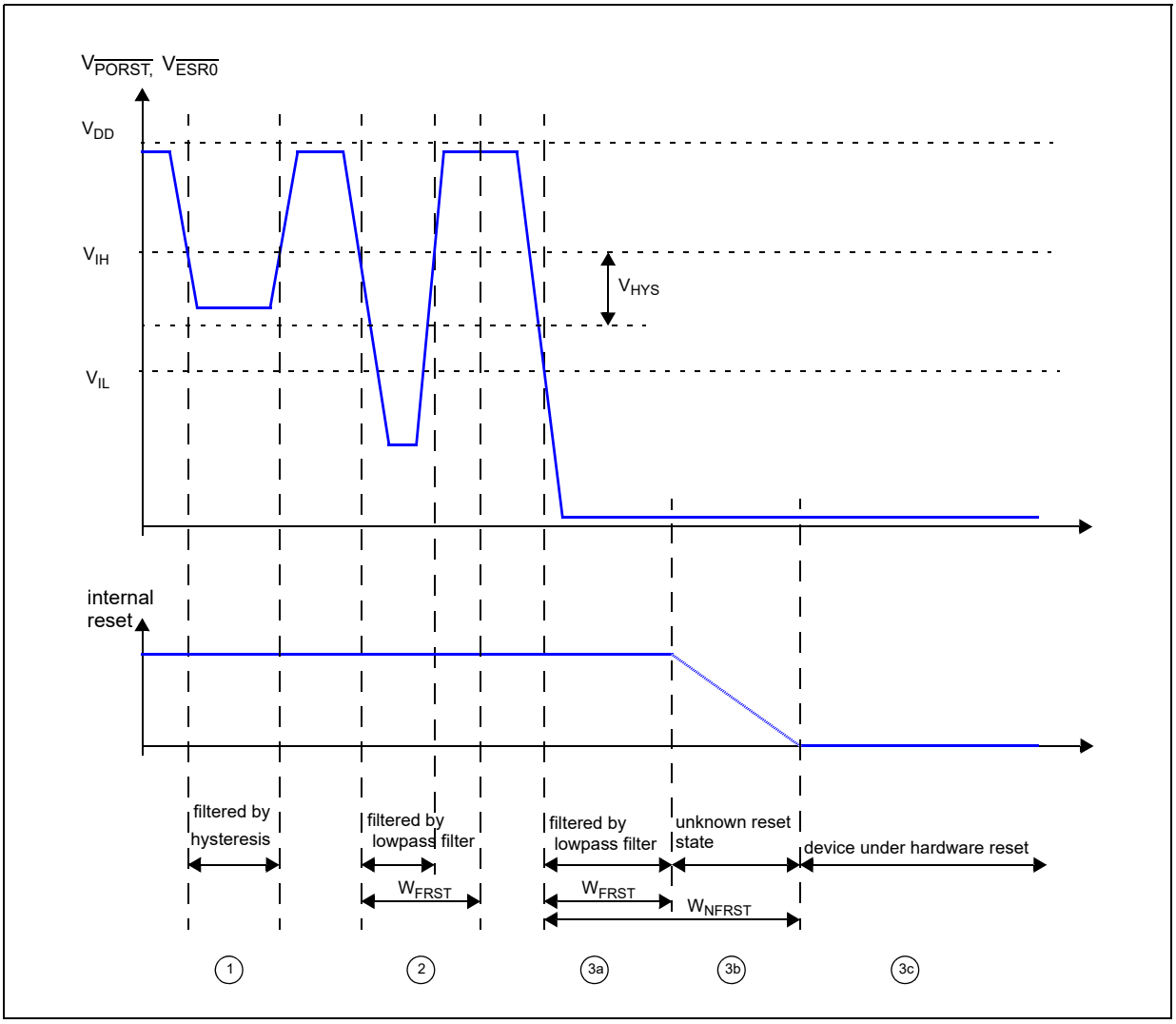


Table 18. Reset PAD electrical characteristics

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
V_{IHRES}	SR	P	Input high level TTL	V_{DD_HV} = 5.0 V ± 10%	2	—	$V_{DD\_HV\_IO}$ +0.3	V
V_{ILRES}	SR	P	Input low level TTL	V_{DD_HV} = 5.0 V ± 10%	-0.3	—	0.8	V
V_{HYSRES}	CC	C	Input hysteresis TTL	V_{DD_HV} = 5.0 V ± 10%	0.3	—	—	V
V_{DD_POR}	CC	D	Minimum supply for strong pull-down activation	V_{DD_HV} = 5.0 V ± 10%	—	—	1.6	V
I_{OL_R}	CC	P	Strong pull-down current (1)	V_{DD_HV} = 5.0 V ± 10%	12	—	—	mA

Table 18. Reset PAD electrical characteristics (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
I_{WPU}	CC	P	Weak pull-up current absolute value	V_{IN} = 1.1 V(2) V_{DD_HV} = 5.0 V ± 10%	—	—	130	µA
		P		V_{IN} = 0.69 * $V_{DD\_HV\_IO}$(3) V_{DD_HV} = 5.0 V ± 10%	15	—	—	
I_{WPD}	CC	P	Weak pull-down current absolute value	V_{IN} = 0.69 * $V_{DD\_HV\_IO}$(2) V_{DD_HV} = 5.0 V ± 10%	—	—	130	µA
		P		V_{IN} = 0.9 V V_{DD_HV} = 5.0 V ± 10%	15	—	—	
W_{FRST}	CC	P	Input filtered pulse	V_{DD_HV} = 5.0 V ± 10%	—	—	500	ns
W_{NFRST}	CC	P	Input not filtered pulse	V_{DD_HV} = 5.0 V ± 10%	2000	—	—	ns

1. I_{ol_r} applies to PORST: Strong Pull-down is active on PHASE0 for PORST. Refer to the device pinout IO definition excel file for details regarding pin usage.
2. Maximum current when forcing a change in the pin level opposite to the pull configuration.
3. Minimum current when keeping the same pin level state than the pull configuration.

Table 19. Reset Pad state during power-up and reset

PAD	POWER-UP State	RESET state	DEFAULT state(1)
PORST	Strong pull-down	Weak pull-down	Weak pull-down
ESR0	Strong pull-down	Strong pull-down	Weak pull-up

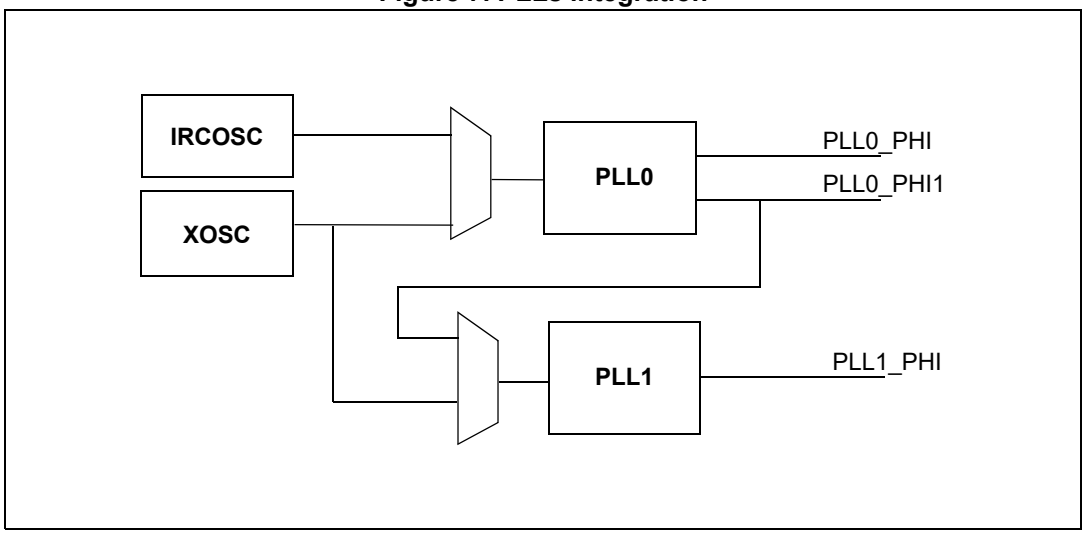
1. Before SW Configuration. Please refer to the Device Reference Manual, Reset Generation Module (MC_RGM) Functional Description chapter for the details of the power-up phases.

3.10 PLLs

Two phase-locked loop (PLL) modules are implemented to generate system and auxiliary clocks on the device.

Figure 7 depicts the integration of the two PLLs. Refer to the device Reference Manual for more detailed schematic.

Figure 7. PLLs integration



3.10.1 PLL0

Table 20. PLL0 electrical characteristics

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
f_{PLL0IN}	SR	—	PLL0 input clock[1]	—	8	—	44	MHz
Δ_{PLL0IN}	SR	—	PLL0 input clock duty cycle[1]	—	40	—	60	%
f_{INFIN}	SR	—	PLL0 PFD (Phase Frequency Detector) input clock frequency	—	8	—	20	MHz
$f_{PLL0VCO}$	CC	P	PLL0 VCO frequency	—	600	—	1400	MHz
$f_{PLL0PHI0}$	CC	D	PLL0 output frequency	—	4.762	—	400	MHz
$f_{PLL0PHI1}$	CC	D	PLL0 output clock PHI1	—	20	—	175[2]	MHz
$t_{PLL0LOCK}$	CC	P	PLL0 lock time	—	—	—	100	µs
$\lvert\Delta_{PLL0PHI0SPJ}\rvert$[3]	CC	T	PLL0_PHI0 single period jitter f_{PLL0IN} = 20 MHz (resonator)	$f_{PLL0PHI0}$ = 400 MHz, 6-sigma pk-pk	—	—	200	ps

Table 20. PLL0 electrical characteristics (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
$\lvert\Delta_{PLL0PHI1SPJ}\rvert$(3)	CC	D	PLL0_PHI1 single period jitter f_{PLL0IN} = 20 MHz (resonator)	$f_{PLL0PHI1}$ = 40 MHz, 6-sigma pk-pk	—	—	300(4)	ps
$\Delta_{PLL0LTJ}$(3)	CC	D	PLL0 output long term jitter(4) f_{PLL0IN} = 20 MHz (resonator), VCO frequency = 800 MHz	10 periods accumulated jitter (80 MHz equivalent frequency), 6-sigma pk-pk	—	—	±250	ps
				16 periods accumulated jitter (50 MHz equivalent frequency), 6-sigma pk-pk	—	—	±300	ps
				long term jitter (< 1 MHz equivalent frequency), 6-sigma pk-pk)	—	—	±500	ps
I_{PLL0}	CC	D	PLL0 consumption	FINE LOCK state	—	—	6	mA

1. PLL0IN clock retrieved directly from either internal RCOSC or external FXOSC clock. Input characteristics are granted when using internal RCOSC or external oscillator is used in functional mode.
2. If the PLL0_PHI1 is used as an input for PLL1, then the PLL0_PHI1 frequency shall obey the maximum input frequency limit set for PLL1 (87.5 MHz, according to *Table 21*).
3. Jitter values reported in this table refer to the internal jitter, and do not include the contribution of the divider and the path to the output CLKOUT pin.
4. V_{DD_LV} noise due to application in the range V_{DD_LV} = 1.20 V±5%, with frequency below PLL bandwidth (40 kHz) will be filtered.

3.10.2 PLL1

PLL1 is a frequency modulated PLL with Spread Spectrum Clock Generation (SSCG) support.

Table 21. PLL1 electrical characteristics

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
f_{PLL1IN}	SR	—	PLL1 input clock(1)	—	37.5	—	87.5	MHz
Δ_{PLL1IN}	SR	—	PLL1 input clock duty cycle(1)	—	35	—	65	%
f_{INFIN}	SR	—	PLL1 PFD (Phase Frequency Detector) input clock frequency	—	37.5		87.5	MHz
$f_{PLL1VCO}$	CC	P	PLL1 VCO frequency	—	600	—	1400	MHz
$f_{PLL1PHI0}$	CC	D	PLL1 output clock PHI0	—	4.762	—	F_{SYS}(2)	MHz
$t_{PLL1LOCK}$	CC	P	PLL1 lock time	—	—	—	50	µs
$f_{PLL1MOD}$	CC	T	PLL1 modulation frequency	—	—	—	250	kHz
$\lvert\delta_{PLL1MOD}\rvert$	CC	T	PLL1 modulation depth (when enabled)	Center spread(3)	0.25	—	2	%
				Down spread	0.5	—	4	%
$\lvert\Delta_{PLL1PHI0SPJ}\rvert$ (4)	CC	T	PLL1_PHI0 single period peak to peak jitter	$f_{PLL1PHI0}$ = 200 MHz, 6-sigma	—	—	500(5)	ps
I_{PLL1}	CC	D	PLL1 consumption	FINE LOCK state	—	—	5	mA

1. PLL1IN clock retrieved directly from either internal PLL0 or external FXOSC clock. Input characteristics are granted when using internal PPL0 or external oscillator is used in functional mode.
2. Refer to *Section 3.3: Operating conditions* for the maximum operating frequency.
3. The device maximum operating frequency F_{SYS} (max) includes the frequency modulation. If center modulation is selected, the FSYS must be below the maximum by MD (Modulation Depth Percentage), such that FSYS(max)=FSYS(1+MD%). Refer to the Reference Manual for the PLL programming details.
4. Jitter values reported in this table refer to the internal jitter, and do not include the contribution of the divider and the path to the output CLKOUT pin.
5. 1.25 V±5%, application noise below 40 kHz at V_{DD_LV} pin - no frequency modulation.

3.11 Oscillators

3.11.1 Crystal oscillator 40 MHz

Table 22. External 40 MHz oscillator electrical specifications

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
f_{XTAL}	CC	D	Crystal Frequency Range[1]	—	4[2]	8	MHz
					>8	20	
					>20	40	
t_{cst}	CC	T	Crystal start-up time [3],[4]	T_J = 150 °C	—	5	ms
				T_J = 165 °C	—	6	
t_{rec}	CC	D	Crystal recovery time[5]	—	—	0.5	ms
V_{IHEXT}	CC	D	EXTAL input high voltage[6] (External Reference)	V_{REF} = 0.29 * $V_{DD\_HV\_OSC}$	V_{REF} + 0.75	—	V
V_{ILEXT}	CC	D	EXTAL input low voltage[6] (External Reference)	V_{REF} = 0.29 * $V_{DD\_HV\_OSC}$	—	V_{REF} - 0.75	V
C_{S_EXTAL}	CC	D	Total on-chip stray capacitance on EXTAL pin[7]	—	3	7	pF
C_{S_XTAL}	CC	D	Total on-chip stray capacitance on XTAL pin[7]	—	3	7	pF
g_m	CC	P	Oscillator Transconductance	f_{XTAL} = 4 – 8 MHz freq_sel[2:0] = 000	3.9	13.6	mA/V
		D		f_{XTAL} = 5 - 10 MHz freq_sel[2:0] = 001	5	17.5	
		D		f_{XTAL} = 10 – 15 MHz freq_sel[2:0] = 010	8.6	29.3	
		P		f_{XTAL} = 15 - 20 MHz freq_sel[2:0] = 011	14.4	48	
		D		f_{XTAL} = 20 - 25 MHz freq_sel[2:0] = 100	21.2	69	
		D		f_{XTAL} = 25 – 30 MHz freq_sel[2:0] = 101	27	86	
		D		f_{XTAL} = 30 - 35 MHz freq_sel[2:0] = 110	33.5	115	
		P		f_{XTAL} = 35 - 40 MHz freq_sel[2:0] = 111	33.5	115	
V_{EXTAL}	CC	D	Oscillation Amplitude on the EXTAL pin after startup[8]	T_J = –40 °C to 150 °C	0.5	1.8	V
				T_J = 150 °C to 165 °C	0.5	1.9	

Table 22. External 40 MHz oscillator electrical specifications (continued)

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
V_{HYS}	CC	D	Comparator Hysteresis	T_J = –40 °C to 150 °C	0.1	1.0	V
				T_J = 150 °C to 165 °C	0.1	1.1	
I_{XTAL}	CC	D	XTAL current(8),(9)	T_J = –40 °C to 150 °C	—	14	mA
				T_J = 150 °C to 165 °C	—	15	

1. The range is selectable by UTEST miscellaneous DCF client XOSC_FREQ_SEL.
2. The XTAL frequency, if used to feed the PPL0 (or PLL1), shall obey the minimum input frequency limit set for PLL0 (or PLL1).
3. This value is determined by the crystal manufacturer and board design, and it can potentially be higher than the maximum provided.
4. Proper PC board layout procedures must be followed to achieve specifications.
5. Crystal recovery time is the time for the oscillator to settle to the correct frequency after adjustment of the integrated load capacitor value.
6. Applies to an external clock input and not to crystal mode.
7. See crystal manufacturer's specification for recommended load capacitor (C_L) values. The external oscillator requires external load capacitors when operating from 8 MHz to 16 MHz. Account for on-chip stray capacitance (C_{S_EXTAL}/C_{S_XTAL}) and PCB capacitance when selecting a load capacitor value. When operating at 20 MHz/40 MHz, the integrated load capacitor value is selected via S/W to match the crystal manufacturer's specification, while accounting for on-chip and PCB capacitance.
8. Amplitude on the EXTAL pin after startup is determined by the ALC block, that is the Automatic Level Control Circuit. The function of the ALC is to provide high drive current during oscillator startup, but reduce current after oscillation in order to reduce power, distortion, and RFI, and to avoid over driving the crystal. The operating point of the ALC is dependent on the crystal value and loading conditions.
9. I_{XTAL} is the oscillator bias current out of the XTAL pin with both EXTAL and XTAL pins grounded. This is the maximum current during startup of the oscillator.

3.11.2 RC oscillator 16 MHz

Table 23. Internal RC oscillator electrical specifications

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
f_{Target}	CC	D	IRC target frequency	—	—	16	—	MHz
δf_{var_noT}	CC	P	IRC frequency variation without temperature compensation	T < 150 °C	–5	—	5	%
		T		T < 165 °C	–7	—	7	
δf_{var_T}	CC	T	IRC frequency variation with temperature compensation	T < 150 °C	–3	—	3	%
				T < 165 °C	–4	—	4	
δf_{var_SW}		T	IRC software trimming accuracy	Trimming temperature	–0.5	±0.3	0.5	%
T_{start_noT}	CC	T	Startup time to reach within f_{var_noT}	Factory trimming already applied	—	—	5	µs

Table 23. Internal RC oscillator electrical specifications (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
T_{start_T}	CC	T	Startup time to reach within f_{var_T}	Factory trimming already applied	—	—	120	µs
I_{FIRC}	CC	T	Current consumption on HV power supply(1)	After T_{start_T}	—	—	1200	µA

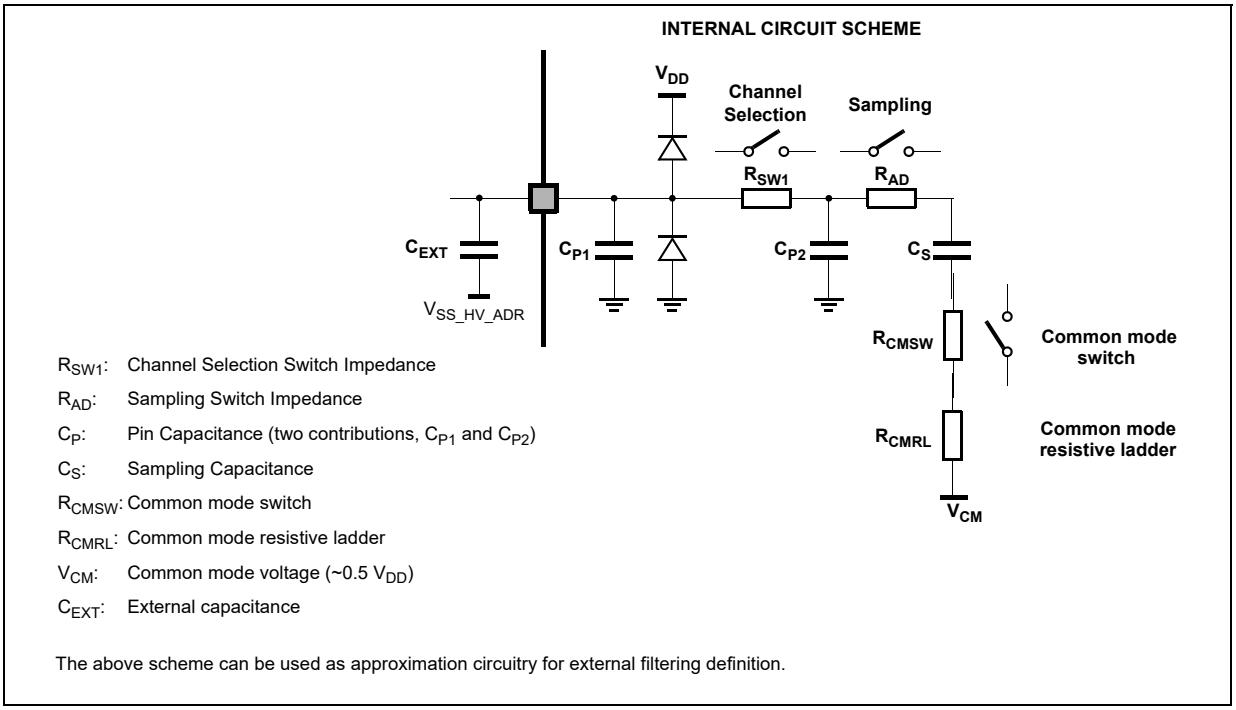
1. The consumption reported considers the sum of the RC oscillator 16 MHz IP, and the core logic clocked by the IP.

3.12 ADC system

3.12.1 ADC input description

Figure 8 shows the input equivalent circuit for SARn and SARB channels.

Figure 8. Input equivalent circuit (Fast SARn and SARB channels)



All specifications in the following table are valid for the full input voltage range for the analog inputs.

Table 24. ADC pin specification

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
$R_{20K\Omega}$	CC	D	Internal voltage reference source impedance.	—	16	30	KΩ
I_{LKG}	CC	—	Input leakage current, two ADC channels on input-only pin.	See IO chapter *Table 11: I/O input electrical characteristics*, parameter I_{LKG}.			
$I_{INJ1,2}$	SR	—	Injection current on analog input preserving functionality at full or degraded performances.	See Operating Conditions chapter *Table 5: Operating conditions*, I_{INJ1} and I_{INJ2} parameters.			
C_{HV_ADC}	SR	D	$V_{DD\_HV\_ADV}$ external capacitance.	See Power Management chapter *Table 38: External components integration*, C_{ADC} parameter.			
C_{P1}	CC	D	Pad capacitance	See IO chapter *Table 11: I/O input electrical characteristics*, parameter C_{P1}.			

Table 24. ADC pin specification (continued)

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
C_{P2}	CC	D	Internal routing capacitance	SARB channels	—	2	pF
				SARn 10bit channels	—	0.5	
				SARn 12bit channels	—	1	
C_S	CC	D	SAR ADC sampling capacitance	SARn 12bit	—	5	pF
				SARn 10bit	—	2	
R_{SWn}	CC	D	Analog switches resistance	SARB channels	0	1.8	kΩ
				SARn 10bit channels	0	0.8	
				SARn 12bit channels	0	1.8	
R_{AD}	CC	D	ADC input analog switches resistance	SARn 12bit	—	0.8	kΩ
				SARn 10bit	—	3.2	
R_{CMSW}	CC	D	Common mode switch resistance	Sum of the two resistances	—	9	kΩ
R_{CMRL}	CC	D	Common mode resistive ladder				kΩ
R_{SAFEPD}(1)	CC	D	Discharge resistance for ADC input-only pins (strong pull-down for safety)	$V_{DD\_HV\_IO}$ = 5.0 V ± 10%	—	300	Ω
				$V_{DD\_HV\_IO}$ = 3.3 V ± 10%	—	500	Ω
A_{BGAP}	CC	D	ADC digital bandgap accuracy		-1.5	+1.5	%
C_{EXT}	SR	—	External capacitance at the pad input pin	To preserve the accuracy of the ADC, it is necessary that analog input pins have low AC impedance. Placing a capacitor with good high frequency characteristics at the input pin of the device can be effective: the capacitor should be as large as possible. This capacitor contributes to attenuating the noise present on the input pin. The impedance relative to the signal source can limit the ADC's sample rate.			

1. It enables discharge of up to 100 nF from 5 V every 300 ms. Refer to the device pinout Microsoft Excel file attached to the IO_Definition document for the pads supporting it.

3.12.2 SAR ADC 12 bit electrical specification

The SARn ADCs are 12-bit Successive Approximation Register analog-to-digital converters with full capacitive DAC. The SARn architecture allows input channel multiplexing.

Note: The functional operating conditions are given in the DC electrical specifications. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the listed maximum may affect device reliability or cause permanent damage to the device.

Table 25. SARn ADC electrical specification

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
f_{ADCK}	SR	P	Clock frequency	Standard frequency mode	7.5	13.33	MHz
		T		High frequency mode	>13.33	16.0	
$t_{ADCINIT}$	SR	—	ADC initialization time	—	1.5	—	µs
$t_{ADCBIASINIT}$	SR	—	ADC BIAS initialization time	—	5	—	µs
$t_{ADCPRECH}$	SR	T	ADC decharge time	Fast SAR	$1/f_{ADCK}$	—	µs
				Slow SAR (SARADC_B)	$2/f_{ADCK}$	—	
ΔV_{PRECH}	SR	D	Decharge voltage precision	T_J < 150 °C	0	0.25	V
				T_J < 165 °C	0	0.3	
$R_{20K\Omega}$	CC	D	Internal voltage reference source impedance	—	16	30	KΩ
ΔV_{INTREF}	CC	P	Internal reference voltage precision	Applies to all internal reference points ($V_{SS\_HV\_ADR}$, 1/3 * $V_{DD\_HV\_ADR}$, 2/3 * $V_{DD\_HV\_ADR}$, $V_{DD\_HV\_ADR}$)	–0.20	0.20	V

Table 25. SARn ADC electrical specification (continued)

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
$t_{ADCSAMPLE}$	SR	P	ADC sample time(1)	Fast SAR – 12-bit configuration	$6/f_{ADCK}$	—	µs
		D		Fast SAR – 10-bit configuration mode 1(2) (Standard frequency mode only)	$6/f_{ADCK}$		
				Fast SAR – 10-bit configuration mode 2(3) (Standard frequency mode only)	$5/f_{ADCK}$		
				Fast SAR – 10-bit configuration mode 3(4) (High frequency mode only)	$6/f_{ADCK}$		
				Slow SAR (SARADC_B) – 12-bit configuration	$12/f_{ADCK}$		
				Slow SAR (SARADC_B) – 10-bit configuration mode 1(2) (Standard frequency mode only)	$12/f_{ADCK}$		
				Slow SAR (SARADC_B) – 10-bit configuration mode 2(3) (Standard frequency mode only)	$10/f_{ADCK}$		
				Slow SAR (SARADC_B) – 10-bit configuration mode 3(4) (High frequency mode only)	$12/f_{ADCK}$		
				Conversion of BIAS test channels through 20 kΩ input.	$40/f_{ADCK}$		
$t_{ADCEVAL}$	SR	P	ADC evaluation time	12-bit configuration	$12/f_{ADCK}$	—	µs
		D		10-bit configuration	$10/f_{ADCK}$	—	

Table 25. SARn ADC electrical specification (continued)

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
$I_{ADCREFH}$(5),(6)	CC	T	ADC high reference current	Run mode (average across all codes) T_j = -40°C to 150°C	—	7	µA
				Run mode (average across all codes) T_j = 150°C to 165°C	—	14	
				Power Down mode T_j = -40°C to 150°C	—	1	
				Power Down mode T_j = 150°C to 165°C	—	2	
$I_{ADCREFL}$(6)	CC	D	ADC low reference current	Run mode $V_{DD\_HV\_ADR\_S} \leq 5.5$ V T_j = -40°C to 150°C	—	15	µA
				Run mode $V_{DD\_HV\_ADR\_S} \leq 5.5$ V T_j = 150°C to 165°C	—	30	
				Power Down mode $V_{DD\_HV\_ADR\_S} \leq 5.5$ V T_j = -40°C to 150°C	—	1	
				Power Down mode $V_{DD\_HV\_ADR\_S} \leq 5.5$ V T_j = 150°C to 165°C	—	2	
I_{ADV_S}(6)	CC	P	$V_{DD\_HV\_ADV}$ power supply current	Run mode	—	4.0	mA
		D		Power Down mode T_j = -40°C to 150°C	—	0.04	
		D		Power Down mode T_j = 150°C to 165°C	—	0.08	

Table 25. SARn ADC electrical specification (continued)

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
TUE_{12}	CC	T	Total unadjusted error in 12-bit configuration(7)	T_J < 150 °C, $V_{DD\_HV\_ADV}$ > 3 V, $V_{DD\_HV\_ADR\_S}$ > 3 V	–4	4	LSB (12b)
		P		T_J < 150 °C, $V_{DD\_HV\_ADV}$ > 3 V, $V_{DD\_HV\_ADR\_S}$ > 3 V	–6	6	
		T		T_J < 150 °C, $V_{DD\_HV\_ADV}$ > 3 V, 3 V > $V_{DD\_HV\_ADR\_S}$ > 2 V	–6	6	
		T		T_J < 165 °C, $V_{DD\_HV\_ADV}$ > 3 V, $V_{DD\_HV\_ADR\_S}$ > 3 V	–9	9	
		T		T_J < 165 °C, $V_{DD\_HV\_ADV}$ > 3 V, 3 V > $V_{DD\_HV\_ADR\_S}$ > 2 V	–11	11	
		D		High frequency mode, T_J < 150 °C, $V_{DD\_HV\_ADV}$ > 3 V, $V_{DD\_HV\_ADR\_S}$ > 3 V	–12	12	
TUE_{10}	CC	D	Total unadjusted error in 10-bit configuration(7)	Mode 1, T_J < 150 °C, $V_{DD\_HV\_ADV}$ > 3 V $V_{DD\_HV\_ADR\_S}$ > 3 V	–1.5	1.5	LSB (10b)
		D		Mode 1, T_J < 150 °C, $V_{DD\_HV\_ADV}$ > 3 V, 3 V > $V_{DD\_HV\_ADR\_S}$ > 2 V	–2.0	2.0	
		D		Mode 1, T_J < 165 °C, $V_{DD\_HV\_ADV}$ > 3 V, $V_{DD\_HV\_ADR\_S}$ > 3 V	–2.5	2.5	
		D		Mode 1, T_J < 165 °C, $V_{DD\_HV\_ADV}$ > 3 V, 3 V > $V_{DD\_HV\_ADR\_S}$ > 2 V	–3.5	3.5	
		C		Mode 2, T_J < 150 °C, $V_{DD\_HV\_ADV}$ > 3 V $V_{DD\_HV\_ADR\_S}$ > 3 V	–3.0	3.0	
		C		Mode 3, T_J < 150 °C, $V_{DD\_HV\_ADV}$ > 3 V $V_{DD\_HV\_ADR\_S}$ > 3 V	–4.0	4.0	

Table 25. SARn ADC electrical specification (continued)

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
ΔTUE_{12}	CC	D	TUE degradation due to $V_{DD\_HV\_ADR}$ offset with respect to $V_{DD\_HV\_ADV}$	$V_{IN} < V_{DD\_HV\_ADV}$ $V_{DD\_HV\_ADR} - V_{DD\_HV\_ADV} \in$ [0:25 mV]	–1	1	LSB (12b)
				$V_{IN} < V_{DD\_HV\_ADV}$ $V_{DD\_HV\_ADR} - V_{DD\_HV\_ADV} \in$ [25:50 mV]	–2	2	
				$V_{IN} < V_{DD\_HV\_ADV}$ $V_{DD\_HV\_ADR} - V_{DD\_HV\_ADV} \in$ [50:75 mV]	–4	4	
				$V_{IN} < V_{DD\_HV\_ADV}$ $V_{DD\_HV\_ADR} - V_{DD\_HV\_ADV} \in$ [75:100 mV]	–6	6	
				$V_{DD\_HV\_ADV} < V_{IN} < V_{DD\_HV\_ADR}$ $V_{DD\_HV\_ADR} - V_{DD\_HV\_ADV} \in$ [0:25 mV]	–2.5	2.5	
				$V_{DD\_HV\_ADV} < V_{IN} < V_{DD\_HV\_ADR}$ $V_{DD\_HV\_ADR} - V_{DD\_HV\_ADV} \in$ [25:50 mV]	–4	4	
				$V_{DD\_HV\_ADV} < V_{IN} < V_{DD\_HV\_ADR}$ $V_{DD\_HV\_ADR} - V_{DD\_HV\_ADV} \in$ [50:75 mV]	–7	7	
				$V_{DD\_HV\_ADV} < V_{IN} < V_{DD\_HV\_ADR}$ $V_{DD\_HV\_ADR} - V_{DD\_HV\_ADV} \in$ [75:100 mV]	–12	12	
TUE_{INJ2}	CC	T	TUE degradation addition, due to current injection in I_{INJ2} range.(8)	See Operating Conditions chapter *Table 5*, I_{INJ2} parameter.	+8		LSB
DNL(9)	CC	P	Differential non-linearity	Standard frequency mode, $V_{DD\_HV\_ADV} > 4$ V $V_{DD\_HV\_ADR\_S} > 4$ V	–1	2	LSB (12b)
		T		High frequency mode, $V_{DD\_HV\_ADV} > 4$ V $V_{DD\_HV\_ADR\_S} > 4$ V	–1	2	

1. Minimum ADC sample times are dependent on adequate charge transfer from the external driving circuit to the internal sample capacitor. The time constant of the entire circuit must allow the sampling capacitor to charge within 1/2 LSB within the sampling window. Refer to *Figure 8* for models of the internal ADC circuit, and the values to use in external RC sizing and calculating the sampling window duration.
2. Mode1: 6 sampling cycles + 10 conversion cycles at 13.33 MHz.
3. Mode2: 5 sampling cycles + 10 conversion cycles at 13.33 MHz.

4. Mode3: 6 sampling cycles + 10 conversion cycles at 16 MHz.
5. $I_{ADCREFH}$ and $I_{ADCREFL}$ are independent from ADC clock frequency. It depends on conversion rate: consumption is driven by the transfer of charge between internal capacitances during the conversion.
6. Current parameter values are for a single ADC.
7. TUE is granted with injection current within the range defined in *Table 24*, for parameters classified as T and D.
8. All channels of all SAR-ADC12bit and SAR-ADC10bit are impacted with same degradation, independently from the ADC and the channel subject to current injection.
9. DNL is granted with injection current within the range defined in *Table 24*, for parameters classified as T and D.

3.12.3 SAR ADC 10 bit electrical specification

The ADC comparators are 10-bit Successive Approximation Register analog-to-digital converters with full capacitive DAC. The SARn architecture allows input channel multiplexing.

Note: The functional operating conditions are given in the DC electrical specifications. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the listed maximum may affect device reliability or cause permanent damage to the device.

Table 26. ADC-Comparator electrical specification

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
f_{ADCK}	SR	P	Clock frequency	Standard frequency mode	7.5	13.33	MHz
		T		High frequency mode	>13.33	16.0	
$t_{ADCINIT}$	SR	—	ADC initialization time	—	1.5	—	µs
$t_{ADCBIASINIT}$	SR	—	ADC BIAS initialization time	—	5	—	µs
$t_{ADCPRECH}$	SR	T	ADC precharge time	—	$1/f_{ADCK}$	—	µs
ΔV_{PRECH}	SR	D	Precharge voltage precision	T_J < 150 °C	0	0.25	V
				T_J < 165 °C	0	0.3	
$t_{ADCSAMPLE}$	SR	P	ADC sample time(1)	10-bit ADC mode	$5/f_{ADCK}$	—	µs
				ADC comparator mode	$2/f_{ADCK}$	—	µs
$t_{ADCEVAL}$	SR	P	ADC evaluation time	10-bit ADC mode	$10/f_{ADCK}$	—	µs
		D		ADC comparator mode	$2/f_{ADCK}$	—	

Table 26. ADC-Comparator electrical specification (continued)

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
$I_{ADCREFH}$[2],[3]	CC	T	ADC high reference current	Run mode (average across all codes) T_j = -40°C to 150°C	—	7	µA
				Run mode (average across all codes) T_j = 150°C to 165°C	—	14	
				Power Down mode T_j = -40°C to 150°C	—	1	
				Power Down mode T_j = 150°C to 165°C	—	2	
				ADC comparator mode T_j = -40°C to 150°C	—	19.5	
				ADC comparator mode T_j = 150°C to 165°C	—	38	
$I_{ADCREFL}$[4]	CC	D	ADC low reference current	Run mode $V_{DD\_HV\_ADR\_S} \leq 5.5$ V T_j = -40°C to 150°C	—	15	µA
				Run mode $V_{DD\_HV\_ADR\_S} \leq 5.5$ V T_j = 150°C to 165°C	—	30	
				Power Down mode $V_{DD\_HV\_ADR\_S} \leq 5.5$ V T_j = -40°C to 150°C	—	1	
				Power Down mode $V_{DD\_HV\_ADR\_S} \leq 5.5$ V T_j = 150°C to 165°C	—	2	
				ADC comparator mode T_j = -40°C to 150°C	—	20.5	
				ADC comparator mode T_j = 150°C to 165°C	—	40	
I_{ADV_S}[4]	CC	P	$V_{DD\_HV\_ADV}$ power supply current	Run mode	—	4	mA
		D		Power Down mode T_j = -40°C to 150°C	—	0.04	
		D		Power Down mode T_j = 150°C to 165°C	—	0.08	

Table 26. ADC-Comparator electrical specification (continued)

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
TUE_{10}	CC	T	Total unadjusted error in 10-bit configuration(5)	T_J < 150 °C, $V_{DD\_HV\_ADV}$ > 3 V, $V_{DD\_HV\_ADR\_S}$ > 3 V	–2	2	LSB (10b)
		P		T_J < 150 °C, $V_{DD\_HV\_ADV}$ > 3 V, $V_{DD\_HV\_ADR\_S}$ > 3 V	–3	3	
		T		T_J < 150 °C, $V_{DD\_HV\_ADV}$ > 3 V, 3 V > $V_{DD\_HV\_ADR\_S}$ > 2 V	–3	3	
		T		T_J < 165 °C, $V_{DD\_HV\_ADV}$ > 3 V, $V_{DD\_HV\_ADR\_S}$ > 3 V	–3	3	
		T		T_J < 165 °C, $V_{DD\_HV\_ADV}$ > 3 V, 3 V > $V_{DD\_HV\_ADR\_S}$ > 2 V	–4	4	
		D		High frequency mode, T_J < 150 °C, $V_{DD\_HV\_ADV}$ > 3 V, $V_{DD\_HV\_ADR\_S}$ > 3 V	–3	3	

Table 26. ADC-Comparator electrical specification (continued)

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
ΔTUE_{10}	CC	D	TUE degradation due to $V_{DD\_HV\_ADR}$ offset with respect to $V_{DD\_HV\_ADV}$	$V_{IN} < V_{DD\_HV\_ADV}$ $V_{DD\_HV\_ADR} - V_{DD\_HV\_ADV} \in$ [0:25 mV]	–1.0	1.0	LSB (10b)
				$V_{IN} < V_{DD\_HV\_ADV}$ $V_{DD\_HV\_ADR} - V_{DD\_HV\_ADV} \in$ [25:50 mV]	–2.0	2.0	
				$V_{IN} < V_{DD\_HV\_ADV}$ $V_{DD\_HV\_ADR} - V_{DD\_HV\_ADV} \in$ [50:75 mV]	–3.5	3.5	
				$V_{IN} < V_{DD\_HV\_ADV}$ $V_{DD\_HV\_ADR} - V_{DD\_HV\_ADV} \in$ [75:100 mV]	–6.0	6.0	
				$V_{DD\_HV\_ADV} < V_{IN} < V_{DD\_HV\_ADR}$ $V_{DD\_HV\_ADR} - V_{DD\_HV\_ADV} \in$ [0:25 mV]	–2.5	2.5	
				$V_{DD\_HV\_ADV} < V_{IN} < V_{DD\_HV\_ADR}$ $V_{DD\_HV\_ADR} - V_{DD\_HV\_ADV} \in$ [25:50 mV]	–4.0	4.0	
				$V_{DD\_HV\_ADV} < V_{IN} < V_{DD\_HV\_ADR}$ $V_{DD\_HV\_ADR} - V_{DD\_HV\_ADV} \in$ [50:75 mV]	–7.0	7.0	
				$V_{DD\_HV\_ADV} < V_{IN} < V_{DD\_HV\_ADR}$ $V_{DD\_HV\_ADR} - V_{DD\_HV\_ADV} \in$ [75:100 mV]	–12.0	12.0	
TUE_{INJ2}	CC	T	TUE degradation addition, due to current injection in I_{INJ2} range.(4)	See Operating Conditions chapter *Table 5*, I_{INJ2} parameter.	3		LSB
DNL(6)	CC	P	Differential non-linearity std. mode	Standard frequency mode, $V_{DD\_HV\_ADV}$ > 4 V $V_{DD\_HV\_ADR\_S}$ > 4 V	–1	2	LSB (10b)
		T		High frequency mode, $V_{DD\_HV\_ADV}$ > 4 V $V_{DD\_HV\_ADR\_S}$ > 4 V	–1	2	

1. Minimum ADC sample times are dependent on adequate charge transfer from the external driving circuit to the internal sample capacitor. The time constant of the entire circuit must allow the sampling capacitor to charge within 1/2 LSB within the sampling window. Refer to *Figure 8* for models of the internal ADC circuit, and the values to use in external RC sizing and calculating the sampling window duration.
2. $I_{ADCREFH}$ and $I_{ADCREFL}$ are independent from ADC clock frequency. It depends on conversion rate: consumption is driven by the transfer of charge between internal capacitances during the conversion.
3. Current parameter values are for a single ADC.

4. All channels of all SAR-ADC12bit and SAR-ADC10bit are impacted with same degradation, independently from the ADC and the channel subject to current injection.
5. TUE is granted with injection current within the range defined in *Table 24*, for parameters classified as T and D.
6. DNL is granted with injection current within the range defined in *Table 24*, for parameters classified as T and D.

3.12.4 S/D ADC electrical specification

The SDn ADCs are Sigma Delta 16-bit analog-to-digital converters with 333666 Ksps maximum output rate.

Note: The functional operating conditions are given in the DC electrical specifications. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the listed maximum may affect device reliability or cause permanent damage to the device.

S/D ADC is functional in the range 3.0 V < VDD_HV_ADV < 4.0 V and 3.0 V < VDD_HV_ADR_D < 4.0 V, but precision of conversion is not guaranteed.

Table 27. SDn ADC electrical specification

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
V_{IN_PK2PK}(1)	SR	D	Input range peak to peak $V_{IN\_PK2PK} = V_{INP}$(2) $- V_{INM}$(3)	Single ended $V_{INM} = V_{SS\_HV\_ADR\_D}$	$V_{DD\_HV\_ADR\_D}$/GAIN			V
		D		Single ended $V_{INM} = 0.5*V_{DD\_HV\_ADR\_D}$ GAIN = 1	±0.5*$V_{DD\_HV\_ADR\_D}$			
		D		Single ended $V_{INM} = 0.5*V_{DD\_HV\_ADR\_D}$ GAIN = 2,4,8,16	±$V_{DD\_HV\_ADR\_D}$/GAIN			
		D		Differential, $0 < V_{IN} < V_{DD\_HV\_IO\_MAIN}$	±$V_{DD\_HV\_ADR\_D}$/GAIN			
f_{ADCD_M}	SR	P	S/D modulator input Clock 3	T_J < 150 °C	4	14.4	16	MHz
f_{IN}	SR	P	Input signal frequency	—	0.01	—	75(4)	kHz
f_{ADCD_S}	SR	D	Output conversion rate	Default Filter Mode effective OSR = 24(5)	—	—	333	ksps
				Modified Filter Mode effective OSR = 12(5)	—	—	666	
				Bypass FIR Mode effective OSR = 24(5)	—	—	333	
				External Filter Mode effective OSR = 6(5)	—	—	1333	

Table 27. SDn ADC electrical specification (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
—	CC	D	Oversampling ratio	Internal modulator	24	—	1024	—
				External modulator	—	—	256	—
RESOLUTION	CC	D	S/D register resolution(6)	2's complement notation	16			bit
GAIN	SR	D	ADC gain	Defined via ADC_SD[PGA] register. Only integer powers of 2 are valid gain values.	1	—	16	—
$\lvert\delta_{GAIN}\rvert$(7)	CC	C	Absolute value of the ADC gain error .(8)(9)	Before calibration (applies to gain setting = 1)	—	—	1	%
		D		After calibration, $\Delta V_{DD\_HV\_ADR\_D} < 5\%$ $\Delta V_{DD\_HV\_ADV\_D} < 10\%$ $\Delta T_J < 50$ °C	—	—	5	mV
				After calibration, $\Delta V_{DD\_HV\_ADR\_D} < 5\%$ $\Delta V_{DD\_HV\_ADV\_D} < 10\%$ $\Delta T_J < 100$ °C	—	—	7.5	
				After calibration, $\Delta V_{DD\_HV\_ADR\_D} < 5\%$ $\Delta V_{DD\_HV\_ADV\_D} < 10\%$ $\Delta T_J < 150$ °C	—	—	10	
				After calibration, $\Delta V_{DD\_HV\_ADR\_D} < 5\%$ $\Delta V_{DD\_HV\_ADV\_D} < 10\%$ $\Delta T_J < 165$ °C	—	—	12.5	
V_{OFFSET}	CC	P	Conversion offset(8),(9),(10)	Before calibration (applies to all gain settings – 1, 2, 4, 8, 16)	—	10* (1+1/gain)	65	mV
		D		After calibration, $\Delta V_{DD\_HV\_ADR\_D} < 10\%$ $\Delta T_J < 50$ °C	—	—	5	mV
				After calibration, $\Delta V_{DD\_HV\_ADR\_D} < 10\%$ $\Delta T_J < 100$ °C	—	—	7.5	
				After calibration, $\Delta V_{DD\_HV\_ADR\_D} < 10\%$ $\Delta T_J < 150$ °C	0.5	—	19	

Table 27. SDn ADC electrical specification (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
$SNR_{DIFF150}$[11]	CC	P	Signal to noise ratio in differential mode 150 ksps output rate[12]	4.0 < $V_{DD\_HV\_ADV}$ < 5.5 $V_{DD\_HV\_ADR\_D}$ = $V_{DD\_HV\_ADV}$ GAIN = 1 T_J < 150 °C	80	—	—	dBFS
		C		4.0 < $V_{DD\_HV\_ADV}$ < 5.5 $V_{DD\_HV\_ADR\_D}$ = $V_{DD\_HV\_ADV}$ GAIN = 2 T_J < 150 °C	77	—	—	
		C		4.0 < $V_{DD\_HV\_ADV}$ < 5.5 $V_{DD\_HV\_ADR\_D}$ = $V_{DD\_HV\_ADV}$ GAIN = 4 T_J < 150 °C	74	—	—	
		C		4.0 < $V_{DD\_HV\_ADV}$ < 5.5 $V_{DD\_HV\_ADR\_D}$ = $V_{DD\_HV\_ADV}$ GAIN = 8 T_J < 150 °C	71	—	—	
		D		4.0 < $V_{DD\_HV\_ADV}$ < 5.5 $V_{DD\_HV\_ADR\_D}$ = $V_{DD\_HV\_ADV}$ GAIN = 16 T_J < 150 °C	68	—	—	

Table 27. SDn ADC electrical specification (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
$SNR_{DIFF333}$[11]	CC	P	Signal to noise ratio in differential mode 333 ksps output rate[12]	4.0 < $V_{DD\_HV\_ADV}$ < 5.5 $V_{DD\_HV\_ADR\_D}$ = $V_{DD\_HV\_ADV}$ GAIN = 1 T_J < 150 °C	71	—	—	dBFS
		C		4.0 < $V_{DD\_HV\_ADV}$ < 5.5 $V_{DD\_HV\_ADR\_D}$ = $V_{DD\_HV\_ADV}$ GAIN = 2 T_J < 150 °C	68	—	—	
		C		4.0 < $V_{DD\_HV\_ADV}$ < 5.5 $V_{DD\_HV\_ADR\_D}$ = $V_{DD\_HV\_ADV}$ GAIN = 4 T_J < 150 °C	65	—	—	
		C		4.0 < $V_{DD\_HV\_ADV}$ < 5.5 $V_{DD\_HV\_ADR\_D}$ = $V_{DD\_HV\_ADV}$ GAIN = 8 T_J < 150 °C	62	—	—	
		D		4.0 < $V_{DD\_HV\_ADV}$ < 5.5 $V_{DD\_HV\_ADR\_D}$ = $V_{DD\_HV\_ADV}$ GAIN = 16 T_J < 150 °C	60	—	—	

Table 27. SDn ADC electrical specification (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
SNR_{SE150}[11]	CC	P	Signal to noise ratio in single ended mode 150 ksps output rate[12]	4.0 < $V_{DD\_HV\_ADV}$ < 5.5 $V_{DD\_HV\_ADR\_D}$ = $V_{DD\_HV\_ADV}$ GAIN = 1 T_J < 150 °C	74	—	—	dBFS
		T		4.0 < $V_{DD\_HV\_ADV}$ < 5.5 $V_{DD\_HV\_ADR\_D}$ = $V_{DD\_HV\_ADV}$ GAIN = 2 T_J < 150 °C	71	—	—	
				4.0 < $V_{DD\_HV\_ADV}$ < 5.5 $V_{DD\_HV\_ADR\_D}$ = $V_{DD\_HV\_ADV}$ GAIN = 4 T_J < 150 °C	68	—	—	
				4.0 < $V_{DD\_HV\_ADV}$ < 5.5 $V_{DD\_HV\_ADR\_D}$ = $V_{DD\_HV\_ADV}$ GAIN = 8 T_J < 150 °C	65	—	—	
		D		4.0 < $V_{DD\_HV\_ADV}$ < 5.5 $V_{DD\_HV\_ADR\_D}$ = $V_{DD\_HV\_ADV}$ GAIN = 16 T_J < 150 °C	62	—	—	
$\Delta_{SNR165C}$	CC	C	165 °C Signal to noise ratio impact	Any GAIN 150 °C < T_J < 165 °C	–9	—	—	dBFS
$\Delta_{SNRINJ2}$	CC	T	TUE degradation addition, due to current injection in I_{INJ2} range.	See Operating Conditions chapter *Table 5*, I_{INJ2} parameter[13]	—	—	–9	dBFS
SFDR	CC	P	Spurious free dynamic range	GAIN = 1	60	—	—	dBc
		C		GAIN = 2	60	—	—	
		C		GAIN = 4	60	—	—	
		C		GAIN = 8	60	—	—	
		D		GAIN = 16	60	—	—	
Z_{DIFF}	CC	D	Differential input impedance (f_{ADCD_M} = 16 MHz)	GAIN = 1	900	1125	1350	kΩ
		D		GAIN = 2	550	700	900	
		D		GAIN = 4	250	350	450	
		D		GAIN = 8	180	225	270	
		D		GAIN = 16	180	225	270	

Table 27. SDn ADC electrical specification (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
Z_{CM}	CC	D	Common mode input impedance (f_{ADCD_M} = 16 MHz)	GAIN = 1	1250	1600	2000	kΩ
		D		GAIN = 2	900	1150	1450	
		D		GAIN = 4	620	850	1050	
		D		GAIN = 8	450	580	720	
		D		GAIN = 16	450	580	720	
R_{BIAS}	CC	D	Bias resistance	—	120	160	200	kΩ
V_{BIAS}	CC	D	Bias voltage	—	—	$V_{DD\_HV\_ADR\_D}/2$	—	V
ΔV_{INTCM}	CC	D	common mode input reference voltage	—	–12	$(V_{DD\_HV\_ADV} + V_{SS\_HV\_ADV})/2$	+12	%
δV_{BIAS}	CC	D	Bias voltage accuracy	—	–2.5	—	+2.5	%
V_{cmrr}	CC	T	Common mode rejection ratio	—	50	—	—	dB
R_{Caaf}	SR	D	Anti-aliasing filter	External series resistance	—	—	20	kΩ
	CC	D		Filter capacitances	180	—	—	pF
$f_{PASSBAND}$	CC	D	Pass band[14]	Default filter mode Bypass FIR mode	0.01	—	0.333 * f_{ADCD_S}	kHz
				Modified bandwidth mode		—	0.166 * f_{ADCD_S}	
				External filter mode (OSR = 75)		—	0.066 * f_{ADCD_S}	
				External filter mode (All OSR, expect 75)		—	0.083 * f_{ADCD_S}	
δ_{RIPPLE}	CC	D	Pass band ripple[15]	$f_{PASSBAND}$ range	–1	—	1	%
$F_{rolloff}$	CC	D	Stop band attenuation Default filter mode[16]	[0.5 * f_{ADCD_S}, 1.0 * f_{ADCD_S}]	40	—	—	dB
				[1.0 * f_{ADCD_S}, 1.5 * f_{ADCD_S}]	54	—	—	
				[1.5 * f_{ADCD_S}, 2.0 * f_{ADCD_S}]	84	—	—	
				[2.0 * f_{ADCD_S}, 2.5 * f_{ADCD_S}]	100	—	—	
				[2.5 * f_{ADCD_S}, $f_{ADCD\_M}/2$]	78	—	—	

Table 27. SDn ADC electrical specification (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
$F_{rolloff}$	CC	D	Stop band attenuation Modified bandwidth mode(16)	[0.25 * f_{ADCD_S}, 0.5 * f_{ADCD_S}]	40	—	—	dB
				[0.5 * f_{ADCD_S}, 0.75 * f_{ADCD_S}]	54	—	—	
				[0.75 * f_{ADCD_S}, 1.0 * f_{ADCD_S}]	78	—	—	
				[1.0 * f_{ADCD_S}, 1.25 * f_{ADCD_S}]	100	—	—	
				[1.25 * f_{ADCD_S}, 1.0 * f_{ADCD_M}/2]	67	—	—	
$F_{rolloff}$	CC	D	Stop band attenuation External Filter mode(16)	[0.5 * f_{ADCD_S}, 1.0 * f_{ADCD_S}]	3	—	—	dB
				[1.0 * f_{ADCD_S}, 1.5 * f_{ADCD_S}]	15	—	—	
				[1.5 * f_{ADCD_S}, 2.0 * f_{ADCD_S}]	41	—	—	
				[2.0 * f_{ADCD_S}, 2.5 * f_{ADCD_S}]	58	—	—	
				[2.5 * f_{ADCD_S}, f_{ADCD_M}/2]	52	—	—	
$F_{rolloff}$	CC	D	Stop band attenuation Bypass FIR mode(16)	[0.5 * f_{ADCD_S}, 1.0 * f_{ADCD_S}]	15	—	—	dB
				[1.0 * f_{ADCD_S}, 1.5 * f_{ADCD_S}]	52	—	—	
				[1.5 * f_{ADCD_S}, 2.0 * f_{ADCD_S}]	53	—	—	
				[2.0 * f_{ADCD_S}, 2.5 * f_{ADCD_S}]	70	—	—	
				[2.5 * f_{ADCD_S}, f_{ADCD_M}/2]	70	—	—	

Table 27. SDn ADC electrical specification (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
δ_{GROUP}	CC	D	Group delay Default filter mode[16]	Within pass band – Tclk is f_{ADCD_M} / 2	—	—	—	—
				OSR = 24	—	—	191.5	Tclk
				OSR = 28	—	—	223	
				OSR = 32	—	—	254.5	
				OSR = 36	—	—	286	
				OSR = 40	—	—	317.5	
				OSR = 44	—	—	349	
				OSR = 48	—	—	380.5	
				OSR = 56	—	—	443.5	
				OSR = 64	—	—	506.5	
				OSR = 72	—	—	569.5	
				OSR = 75	—	—	550	
				OSR = 80	—	—	632.5	
				OSR = 88	—	—	695.5	
				OSR = 96	—	—	758.5	
				OSR = 112	—	—	884.5	
				OSR = 128	—	—	1010.5	
				OSR = 144	—	—	1136.5	
				OSR = 160	—	—	1262.5	
				OSR = 176	—	—	1388.5	
				OSR = 192	—	—	1514.5	
				OSR = 224	—	—	1766.5	
				OSR = 256	—	—	2018.5	
				OSR = 512	—	—	4034.5	
				OSR = 1024	—	—	8066.5	

Table 27. SDn ADC electrical specification (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
δ_{GROUP}	CC	D	Group delay Modified bandwidth mode(16)	Within pass band – Tclk is f_{ADCD_M} / 2	—	—	—	—
				OSR = 24	—	—	203.5	Tclk
				OSR = 28	—	—	237	
				OSR = 32	—	—	270.5	
				OSR = 36	—	—	304	
				OSR = 40	—	—	337.5	
				OSR = 44	—	—	371	
				OSR = 48	—	—	404.5	
				OSR = 56	—	—	471.5	
				OSR = 64	—	—	538.5	
				OSR = 72	—	—	605.5	
				OSR = 75	—	—	580	
				OSR = 80	—	—	672.5	
				OSR = 88	—	—	739.5	
				OSR = 96	—	—	806.5	
				OSR = 112	—	—	940.5	
				OSR = 128	—	—	1074.5	
				OSR = 144	—	—	1208.5	
				OSR = 160	—	—	1342.5	
				OSR = 176	—	—	1476.5	
				OSR = 192	—	—	1610.5	
				OSR = 224	—	—	1878.5	
				OSR = 256	—	—	2146.5	
				OSR = 512	—	—	4290.5	
				OSR = 1024	—	—	8578.5	

Table 27. SDn ADC electrical specification (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
δ_{GROUP}	CC	D	Group delay Bypass FIR mode(16)	Within pass band – Tclk is f_{ADCD_M} / 2	—	—	—	—
				OSR = 24	—	—	62.5	Tclk
				OSR = 28	—	—	72.5	
				OSR = 32	—	—	82.5	
				OSR = 36	—	—	92.5	
				OSR = 40	—	—	102.5	
				OSR = 44	—	—	112.5	
				OSR = 48	—	—	122.5	
				OSR = 56	—	—	142.5	
				OSR = 64	—	—	162.5	
				OSR = 72	—	—	182.5	
				OSR = 75	—	—	190	
				OSR = 80	—	—	202.5	
				OSR = 88	—	—	222.5	
				OSR = 96	—	—	242.5	
				OSR = 112	—	—	282.5	
				OSR = 128	—	—	322.5	
				OSR = 144	—	—	362.5	
				OSR = 160	—	—	402.5	
				OSR = 176	—	—	442.5	
				OSR = 192	—	—	482.5	
				OSR = 224	—	—	562.5	
				OSR = 256	—	—	642.5	
				OSR = 512	—	—	1282.5	
				OSR = 1024	—	—	2562.5	

Table 27. SDn ADC electrical specification (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
δ_{GROUP}	CC	D	Group delay External filter mode(16)	Within pass band – Tclk is f_{ADCD_M} / 2	—	—	—	—
				OSR = 24	—	—	29.5	Tclk
				OSR = 28	—	—	34	
				OSR = 32	—	—	38.5	
				OSR = 36	—	—	43	
				OSR = 40	—	—	47.5	
				OSR = 44	—	—	52	
				OSR = 48	—	—	56.5	
				OSR = 56	—	—	65.5	
				OSR = 64	—	—	74.5	
				OSR = 72	—	—	83.5	
				OSR = 75	—	—	86.875	
				OSR = 80	—	—	92.5	
				OSR = 88	—	—	101.5	
				OSR = 96	—	—	110.5	
				OSR = 112	—	—	128.5	
				OSR = 128	—	—	146.5	
				OSR = 144	—	—	164.5	
				OSR = 160	—	—	182.5	
				OSR = 176	—	—	200.5	
				OSR = 192	—	—	218.5	
				OSR = 224	—	—	254.5	
				OSR = 256	—	—	290.5	
				OSR = 512	—	—	578.5	
				OSR = 1024	—	—	1154.5	
f_{HIGH}	CC	D	High pass filter 3dB frequency	Enabled	—	10e-5* f_{ADCD_S}	—	—
$t_{STARTUP}$	CC	D	Start-up time from power down state	—	—	—	100	µs
$t_{LATENCY}$	CC	D	Latency between input data and converted data (input mux not changed)(17)	HPF = ON	—	—	δ_{GROUP} + f_{ADCD_S}	—
				HPF = OFF	—	—	δ_{GROUP}	—

Table 27. SDn ADC electrical specification (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
$t_{SETTLING}$	CC	D	Settling time after mux change	Analog inputs are muxed HPF = ON	—	—	$2*\delta_{GROUP} + 3*f_{ADCD\_S}$	—
				HPF = OFF	—	—	$2*\delta_{GROUP} + 2*f_{ADCD\_S}$	—
$t_{ODRECOVERY}$	CC	D	Overdrive recovery time	After input comes within range from saturation HPF = ON	—	—	$2*\delta_{GROUP} + f_{ADCD\_S}$	—
				HPF = OFF	—	—	$2*\delta_{GROUP}$	—
C_{S_D}	CC	D	S/D ADC sampling capacitance after sampling switch(18)	GAIN = 1, 2, 4, 8	—	—	75*GAIN	fF
				GAIN = 16	—	—	600	fF
IBIAS	CC	D	Bias consumption	At least 1 ADCD enabled	—	—	5	mA
I_{ADV_D}	CC	C	$V_{DD\_HV\_ADV}$ power supply current (each ADC)	ADCD enabled	—	—	3.5	mA
ΣI_{ADR_D}	CC	C	Sum of all ADC reference consumption(19)	ADCD enabled T_j = -40°C to 150°C	—	—	80	µA
				ADCD enabled T_j = 150°C to 165°C	—	—	160	µA

1. For input voltage above the maximum and below the clamp voltage of the input pad, there is no latch-up concern, and the signal will only be ‘clipped’.
2. V_{INP} is the input voltage applied to the positive terminal of the SDADC.
3. V_{INM} is the input voltage applied to the negative terminal of the SDADC.
4. Maximum input of 166.67 KHz supported with reduced accuracy. See SNR specifications.
5. Configured oversampling rate: SDADC_MCR[PDR] = 24.
6. When using a GAIN setting of 16, the conversion result will always have a value of zero in the least significant bit. This gives an effective resolution of 15 bits.
7. The absolute value of the ADC gain error (|δGAIN|) after calibration is applicable in differential mode only. In single-ended mode after calibration, this value should be considered as 25mV.
8. Offset and gain error due to temperature drift can occur in either direction (+/-) for each of the SDADCs on the device.
9. Calibration of gain is possible when gain = 1. Offset Calibration should be done with respect to 0.5*VDD_HV_ADR_D for "differential mode" and "single ended mode with negative input=0.5*VDD_HV_ADR_D". Offset Calibration should be done with respect to 0 for "single ended mode with negative input=0". Both offset and Gain Calibration are guaranteed for ±5% variation of VDD_HV_ADR_D, ±10% variation of VDD_HV_ADV, and ± 50 °C temperature variation.
10. Conversion offset error must be divided by the applied gain factor (1, 2, 4, 8, or 16) to obtain the actual input referred offset error.
11. This parameter is guaranteed by bench validation with a small sample of devices across process variations, and tested in production to a value of 3 dB less.
12. S/D ADC is functional in the range 3.6 V < $V_{DD\_HV\_ADV}$ < 4.0 V and, SNR parameter degrades by 12 dB. Degraded SNR value based on simulation and granted by design.
13. All channels of all SD-ADCs are impacted with same degradation, independently from the ADC and the channel subject to current injection.

14. SNR value guaranteed only if external noise on the ADC input pin is attenuated by the required SNR value in the frequency range of $f_{ADCD\_M} - f_{ADCD\_S}$ to $f_{ADCD\_M} + f_{ADCD\_S}$, where f_{ADCD_M} is the input sampling frequency, and f_{ADCD_S} is the output sample frequency. A proper external input filter should be used to remove any interfering signals in this frequency range.
15. The ±1% passband ripple specification is equivalent to $20 * \log_{10}(0.99) = 0.087$ dB.
16. For details, refer to *Section 3.12.5: SD ADC filter modes*.
17. Propagation of the information from the pin to the register CDR[CDATA] and flags SFR[DFEF], SFR[DFFF] is given by the different modules that need to be crossed: delta/sigma filters, high pass filter, fifo module, clock domain synchronizers. The time elapsed between data availability at pin and internal S/D module registers is given by the below formula: REGISTER LATENCY = $t_{LATENCY} + 0.5/f_{ADCD\_S} + 2\ (\sim+1)/f_{ADCD\_M} + 2(\sim+1)f_{PBRIDGEx\_CLK}$ where f_{ADCD_S} is the frequency of the sampling clock, f_{ADCD_M} is the frequency of the modulator, and $f_{PBRIDGEx\_CLK}$ is the frequency of the peripheral bridge clock feeds to the ADC S/D module. The (~+1) symbol refers to the number of clock cycles uncertainty (from 0 to 1 clock cycle) to be added due to resynchronization of the signal during clock domain crossing. Some further latency may be added by the target module (core, DMA, interrupt) controller to process the data received from the ADC S/D module.
18. This capacitance does not include pin capacitance, that can be considered together with external capacitance, before sampling switch.
19. Consumption is given after power-up, when steady state is reached. Extra consumption up to 2 mA may be required during internal circuitry set-up.

3.12.5 SD ADC filter modes

Table 28 describes the 4 SD ADC filter modes which are controlled by bits BANDSEL, FSEL and EXTFILTER of the Module Configuration Register (MCR). For details, refer to the SPC58xNx Reference Manual.

Table 28. Filter modes

BANDSEL	FSEL	EXTFILTER	Filter Mode
0	0	0	Normal/Default mode
1	0	0	Modified bandwidth mode
X	1	0	Bypass FIR mode
X	X	1	External filter mode

In normal/default mode, modified bandwidth mode and bypass FIR mode, the output values are not normalized by hardware. To apply normalization by software *Table 29* lists the digital output codes in these modes when input signal is full range.

Table 29. Digital output codes in full scale

OSR	MCR[FSEL] = 1 MCR[GECEN] = 1	MCR[FSEL] = 0 MCR[BANDSEL] = 0 MCR[GECEN] = 1	MCR[FSEL] = 0 MCR[BANDSEL] = 1 MCR[GECEN] = 1
24	29160	31081	31095
28	29157	31077	31092
32	29158	31079	31093
36	29155	31075	31090
40	29109	31026	31042
44	29121	31040	31054
48	29160	31081	31095
56	29157	31077	31092

Table 29. Digital output codes in full scale (continued)

OSR	MCR[FSEL] = 1 MCR[GECEN] = 1	MCR[FSEL] = 0 MCR[BANDSEL] = 0 MCR[GECEN] = 1	MCR[FSEL] = 0 MCR[BANDSEL] = 1 MCR[GECEN] = 1
64	29158	31079	31093
72	29155	31075	31090
75	29064	31128	31143
80	29109	31026	31042
88	29121	31040	31054
96	29160	31081	31095
112	29157	31078	31092
128	29158	31079	31093
144	29155	31076	31089
160	29109	31026	31042
176	29121	31040	31054
192	29160	31081	31095
224	29157	31078	31092
256	29158	31079	31093
512	29158	31079	31093
1024	29158	31079	31093

3.13 Temperature Sensor

The following table describes the temperature sensor electrical characteristics.

Table 30. Temperature sensor electrical characteristics

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
—	CC	—	Temperature monitoring range	—	–40	—	165	°C
T_{SENS}	CC	T	Sensitivity	—	—	5.18	—	mV/°C
T_{ACC}	CC	P	Accuracy	T_J < 150 C	–3	—	3	°C
		C		T_J < 165 °C	–7	—	7	

3.14 LFAST pad electrical characteristics

The LFAST(LVDS Fast Asynchronous Serial Transmission) pad electrical characteristics apply to both the SIPI and high-speed debug serial interfaces on the device. The same LVDS pad is used for the Microsecond Channel (MSC) and DSPI LVDS interfaces, with different characteristics given in the following tables.

3.14.1 LFAST interface timing diagrams

Figure 9. LFAST and MSC/DSPI LVDS timing definition

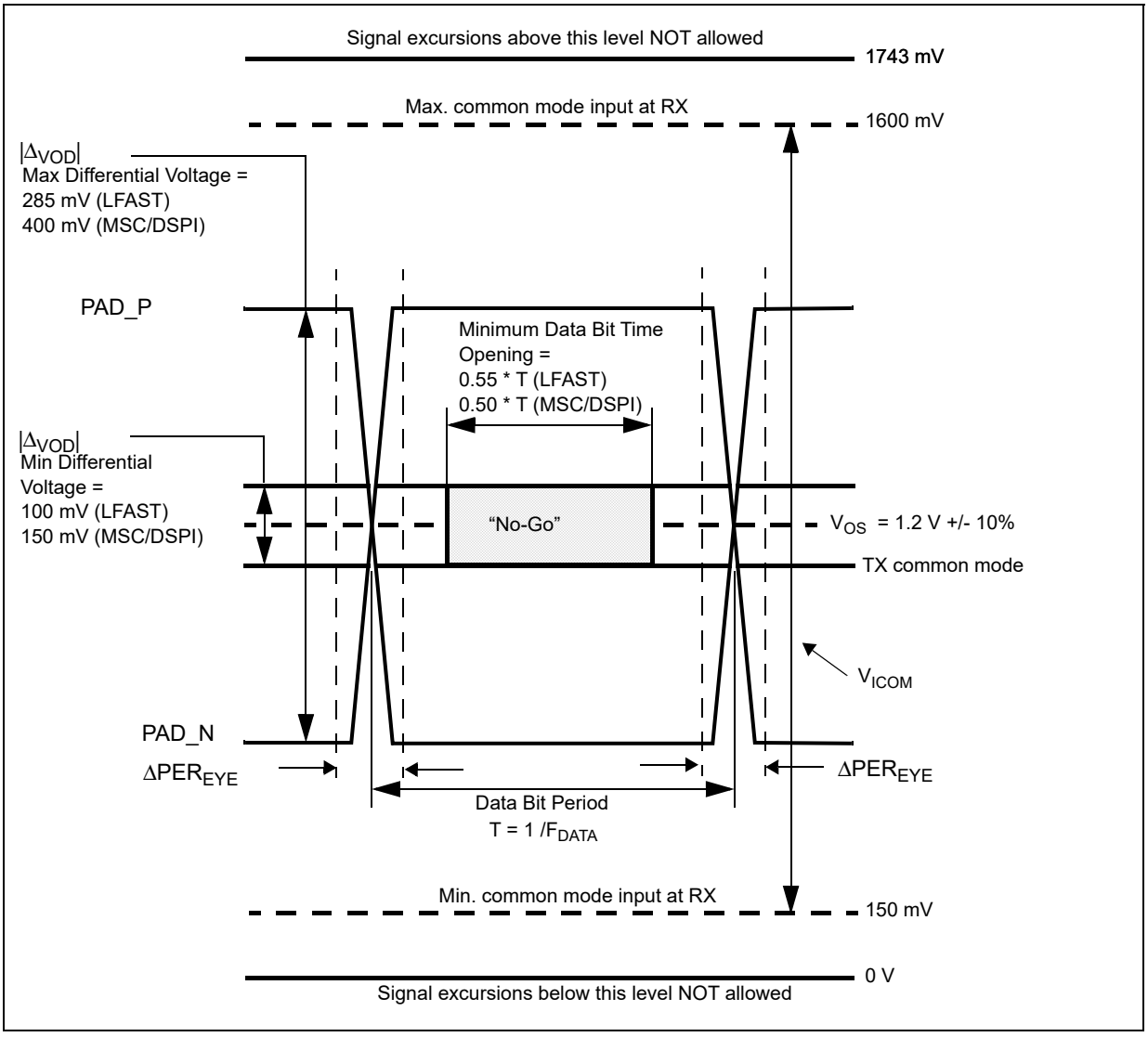


Figure 10. Power-down exit time

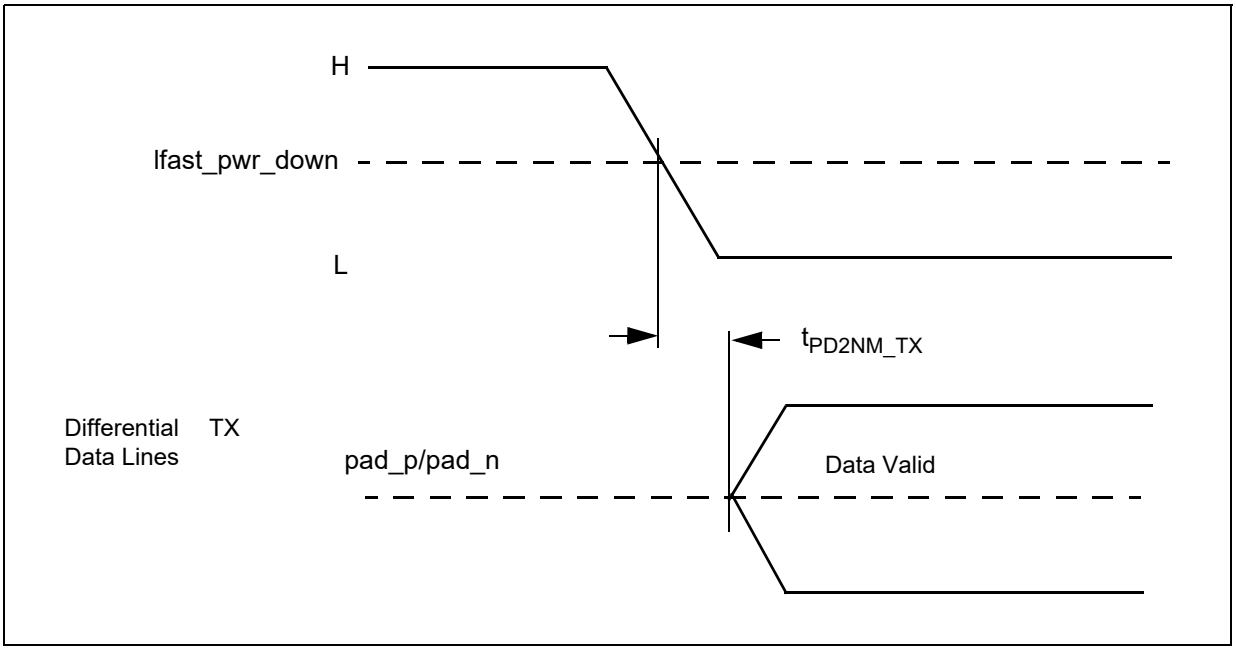
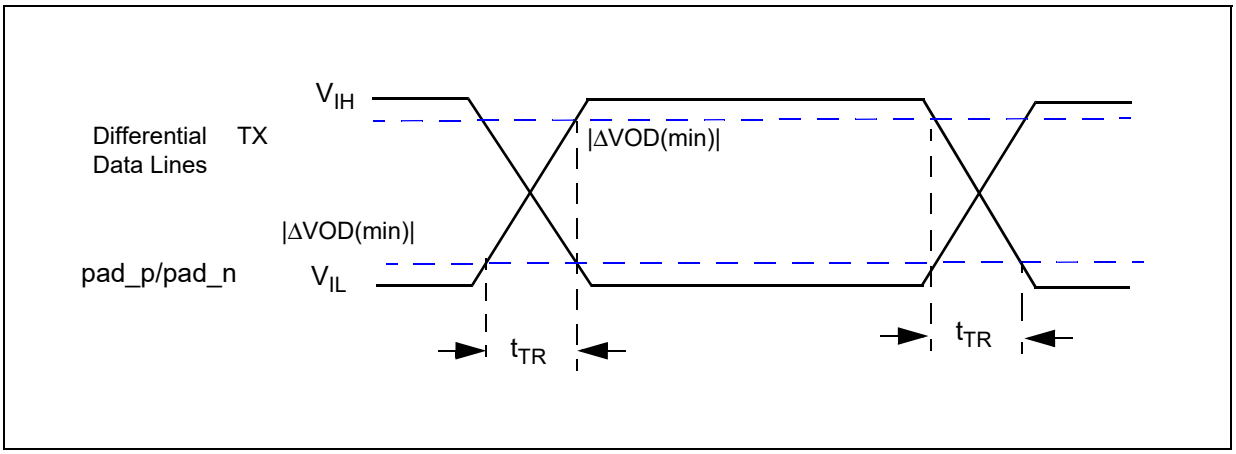


Figure 11. Rise/fall time



3.14.2 LFAST and MSC/DSPI LVDS interface electrical characteristics

The following table contains the electrical characteristics for the LFAST interface.

Table 31. LVDS pad startup and receiver electrical characteristics(1),(2)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
STARTUP(3),(4)								
t_{STRT_BIAS}	CC	T	Bias current reference startup time(5)	—	—	0.5	4	µs
t_{PD2NM_TX}	CC	T	Transmitter startup time (power down to normal mode)(6)	—	—	0.4	2.75	µs

Table 31. LVDS pad startup and receiver electrical characteristics[1],[2] (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
t_{SM2NM_TX}	CC	T	Transmitter startup time (sleep mode to normal mode)[7]	Not applicable to the MSC/DSPI LVDS pad	—	0.4	0.6	µs
t_{PD2NM_RX}	CC	T	Receiver startup time (power down to normal mode)[8]	—	—	20	40	ns
t_{PD2SM_RX}	CC	T	Receiver startup time (power down to sleep mode)[9]	Not applicable to the MSC/DSPI LVDS pad	—	20	50	ns
I_{LVDS_BIAS}	CC	D	LVDS bias current consumption	Tx or Rx enabled	—	—	0.95	mA
TRANSMISSION LINE CHARACTERISTICS (PCB Track)								
Z_0	SR	D	Transmission line characteristic impedance	—	47.5	50	52.5	Ω
Z_{DIFF}	SR	D	Transmission line differential impedance	—	95	100	105	Ω
RECEIVER								
V_{ICOM}	SR	T	Common mode voltage	—	0.15 [10]	—	1.6[11]	V
$\|\Delta_{VI}\|$	SR	T	Differential input voltage[12]	—	100	—	—	mV
V_{HYS}	CC	T	Input hysteresis	—	25	—	—	mV
R_{IN}	CC	D	Terminating resistance	$V_{DD\_HV\_IO}$ = 5.0 V ± 10% -40 °C < T_J< 150 °C	80	—	120	Ω
				$V_{DD\_HV\_IO}$ = 3.3 V ± 10% -40 °C < T_J< 150 °C				
				$V_{DD\_HV\_IO}$ = 5.0 V ± 10% -40 °C<Tj<165 °C				
				$V_{DD\_HV\_IO}$ = 3.3 V ± 10% -40 °C<Tj<165 °C			160	
C_{IN}	CC	D	Differential input capacitance[13]	—	—	3.5	6.0	pF
I_{LVDS_RX}	CC	C	Receiver DC current consumption	Enabled	—	—	1.6	mA
I_{PIN_RX}	CC	D	Maximum consumption on receiver input pin	Δ_{VI} = 400 mV, R_{IN} = 80 Ω	—	—	5	mA

1. The LVDS pad startup and receiver electrical characteristics in this table apply to both the LFAST & High-speed Debug (HSD) LVDS pad, and the MSC/DSPI LVDS pad except where noted in the conditions.
2. All LVDS pad electrical characteristics are valid from -40 °C to 150 °C.
3. All startup times are defined after a 2 peripheral bridge clock delay from writing to the corresponding enable bit in the LVDS control registers (LCR) of the LFAST and High-speed Debug modules. The value of the LCR bits for the LFAST/HSD modules don't take effect until the corresponding SIUL2 MSCR ODC bits are set to LFAST LVDS mode. Startup times for MSC/DSPI LVDS are defined after 2 peripheral bridge clock delay after selecting MSC/DSPI LVDS in the corresponding SIUL2 MSCR ODC field.

4. Startup times are valid for the maximum external loads CL defined in both the LFAST/HSD and MSC/DSPI transmitter electrical characteristic tables.
5. Bias startup time is defined as the time taken by the current reference block to reach the settling bias current after being enabled.
6. Total transmitter startup time from power down to normal mode is t_{STRT_BIAS} + t_{PD2NM_TX} + 2 peripheral bridge clock periods.
7. Total transmitter startup time from sleep mode to normal mode is t_{SM2NM_TX} + 2 peripheral bridge clock periods. Bias block remains enabled in sleep mode.
8. Total receiver startup time from power down to normal mode is t_{STRT_BIAS} + t_{PD2NM_RX} + 2 peripheral bridge clock periods.
9. Total receiver startup time from power down to sleep mode is t_{PD2SM_RX} + 2 peripheral bridge clock periods. Bias block remains enabled in sleep mode.
10. Absolute min = 0.15 V – (285 mV/2) = 0 V
11. Absolute max = 1.6 V + (285 mV/2) = 1.743 V
12. Value valid for LFAST mode and SPI mode. In LFAST mode the LXRXOP_BR bit in the LFAST LVDS Control Register (LCR) must be set to one to ensure proper LFAST receive timing.
13. Total internal capacitance including receiver and termination, co-bonded GPIO pads, and package contributions.

Table 32. LFAST transmitter electrical characteristics(1),(2),(3)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
f_{DATA}	SR	D	Data rate	—	—	—	320	Mbps
V_{OS}	CC	P	Common mode voltage	—	1.08	—	1.32	V
$\|\Delta_{VOD}\|$	CC	P	Differential output voltage swing (terminated)(4),(5)	—	110	—	285	mV
t_{TR}	CC	T	Rise time from -|ΔVOD(min)| to +|ΔVOD(min)|. Fall time from +|ΔVOD(min)| to -|ΔVOD(min)|	—	0.26	—	1.25	ns
C_L	SR	D	External lumped differential load capacitance(4)	$V_{DD\_HV\_IO}$ = 4.5 V	—	—	6.0	pF
				$V_{DD\_HV\_IO}$ = 3.0 V	—	—	4.0	
I_{LVDS_TX}	CC	C	Transmitter DC current consumption	Enabled	—	—	3.6	mA
I_{PIN_TX}	CC	D	Transmitter DC current sourced through output pin	—	1.1		2.85	mA

1. This table is applicable to LFAST LVDS pads used in LFAST configuration (SIUL2_MSCR_IO_n.ODC=101).
2. The LFAST and High-Speed Debug LFAST pad electrical characteristics are based on worst case internal capacitance values shown in *Figure 12*.
3. All LFAST and High-Speed Debug LVDS pad electrical characteristics are valid from -40 °C to 165 °C.
4. Valid for maximum data rate f_{DATA}. Value given is the capacitance on each terminal of the differential pair, as shown in *Figure 12*.
5. Valid for maximum external load C_L.

Table 33. MSC/DSPI LVDS transmitter electrical characteristics (1),(2),(3)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
f_{DATA}	SR	D	Data rate	—	—	—	80	Mbps
V_{OS}	CC	P	Common mode voltage	—	1.08	—	1.32	V
$\lvert\Delta_{VOD}\rvert$	CC	P	Differential output voltage swing (terminated)(4),(5)	—	150	—	400	mV
t_{TR}	CC	T	Rise time from -|ΔVOD(min)| to +|ΔVOD(min)|. Fall time from +|ΔVOD(min)| to -|ΔVOD(min)|(6)	—	0.8	—	5.8	ns
C_L	SR	D	External lumped differential load capacitance(4)	$V_{DD\_HV\_IO}$ = 4.5 V	—	—	50	pF
				$V_{DD\_HV\_IO}$ = 3.0 V	—	—	39	
I_{LVDS_TX}	CC	C	Transmitter DC current consumption	Enabled	—	—	5.0	mA
I_{PIN_TX}	CC	D	Transmitter DC current sourced through output pin	—	1.5	—	4.0	mA

1. This table is applicable to MSC/DSPI LVDS pads used in MSC configuration (SIUL2_MSCR_IO_n.ODC=100).
2. The MSC and DSPI LVDS pad electrical characteristics are based on the application circuit and typical worst case internal capacitance values given in *Figure 12*.
3. All MSC and DSPI LVDS pad electrical characteristics are valid from -40 °C to 165 °C.
4. Valid for maximum data rate f_{DATA}. Value given is the capacitance on each terminal of the differential pair, as shown in *Figure 12*.
5. Valid for maximum external load C_L.
6. The transition time is measured from 10% to 90% of the voltage transition from -|ΔVOD|(min) to +|ΔVOD|(min).

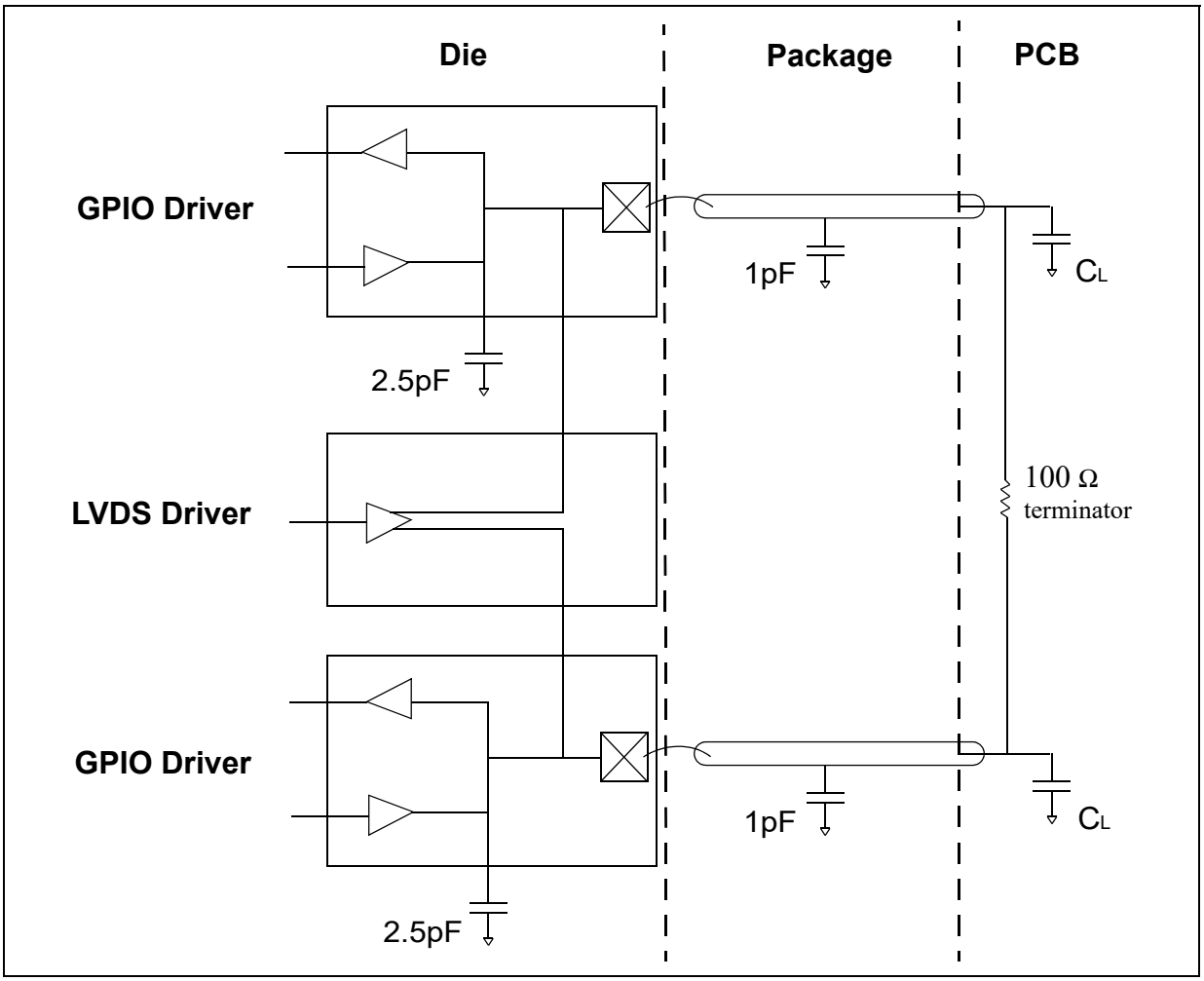
Table 34. MSC LVDS transmitter electrical characteristics for LFAST pads. (1),(2),(3)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
f_{DATA}	SR	D	Data rate	—	—	—	320	Mbps
V_{OS}	CC	P	Common mode voltage	—	1.08	—	1.32	V
$\lvert\Delta_{VOD}\rvert$	CC	P	Differential output voltage swing (terminated)(4),(5)	—	120	—	400	mV
t_{TR}	CC	T	Rise time from -|ΔVOD(min)| to +|ΔVOD(min)|. Fall time from +|ΔVOD(min)| to -|ΔVOD(min)|(6)	—	0.26	—	1.4	ns
C_L	SR	D	External lumped differential load capacitance(4)	$V_{DD\_HV\_IO}$ = 4.5 V	—	—	12.0	pF
				$V_{DD\_HV\_IO}$ = 3.0 V	—	—	8.5	
I_{LVDS_TX}	CC	C	Transmitter DC current consumption	Enabled	—	—	5.0	mA
I_{PIN_TX}	CC	D	Transmitter DC current sourced through output pin	—	1.5		4.0	mA

1. This table is applicable to LFAST LVDS pads used in MSC configuration (SIUL2_MSCR_IO_n.ODC=100).
2. The MSC and DSPI LVDS pad electrical characteristics are based on the application circuit and typical worst case internal capacitance values given in *Figure 12*.

3. All MSC and DSPI LVDS pad electrical characteristics are valid from -40 °C to 165 °C.
4. Valid for maximum data rate f_{DATA}. Value given is the capacitance on each terminal of the differential pair, as shown in *Figure 12*.
5. Valid for maximum external load C_L.
6. The transition time is measured from 10% to 90% of the voltage transition from -|ΔVOD|(min) to +|ΔVOD|(min).

Figure 12. LVDS pad external load diagram



3.14.3 LFAST PLL electrical characteristics

The following table contains the electrical characteristics for the LFAST PLL.

Table 35. LFAST PLL electrical characteristics(1)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
f_{RF_REF}	SR	D	PLL reference clock frequency (CLKIN)	—	10(2)	—	30	MHz
ERR_{REF}	CC	D	PLL reference clock frequency error	—	-1	—	1	%

Table 35. LFAST PLL electrical characteristics(1) (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
DC_{REF}	CC	D	PLL reference clock duty cycle (CLKIN)	—	30	—	70	%
PN	CC	D	Integrated phase noise (single side band)	f_{RF_REF} = 20 MHz	—	—	-58	dBc
f_{VCO}	CC	P	PLL VCO frequency	—	312	—	320(3)	MHz
t_{LOCK}	CC	D	PLL phase lock	—	—	—	150(4)	µs
ΔPER_{REF}	SR	T	Input reference clock jitter (peak to peak)	Single period, f_{RF_REF} = 20 MHz	—	—	350	ps
		T		Long term, f_{RF_REF} = 20 MHz	-500	—	500	ps
ΔPER_{EYE}	CC	T	Output Eye Jitter (peak to peak)(5)	—	—	—	400	ps

1. The specifications in this table apply to both the interprocessor bus and debug LFAST interfaces.
2. If the input frequency is lower than 20 MHz, it is required to set a input division factor of 1.
3. The 320 MHz frequency is achieved with a 20 MHz reference clock.
4. The total lock time is the sum of the coarse lock time plus the programmable lock delay time 2 clock cycles of the peripheral bridge clock that is connected to the PLL on the device (to set the PLL enable bit).
5. Measured at the transmitter output across a 100 Ω termination resistor on a device evaluation board. See *Figure 12*.

3.15 Aurora LVDS electrical characteristics

The following table describes the Aurora LVDS electrical characteristics.

Note: The Aurora interface is AC coupled, so there is no common-mode voltage specification

Table 36. Aurora LVDS electrical characteristics(1),(2)

Symbol	C		Parameter	Conditions	Value			Unit
					Min	Typ	Max	
Transmitter								
F_{TX}	CC	D	Transmit Data Rate	—	—	—	1.25	Gbps
$\|\Delta V_{OD\_LVDS}\|$	CC	T	Differential output voltage swing (terminated)(3)	—	±400	±600	±800	mV
t_{TR_LVDS}	CC	T	Rise/Fall time (10%–90% of swing)	—	60	—	—	ps
$R_{V\_L\_Tx}$	SR	D	Differential Terminating resistance	—	81	100	120	W
T_{Loss}	CC	D	Transmission Line Loss due to loading effects	—	—	—	6(4)	dB
Transmission line characteristics (PCB track)								
L_{LINE}	SR	D	Transmission line length	—	—	—	20	cm
Z_{LINE}	SR	D	Transmission line characteristic impedance	—	45	50	55	W
C_{AC_CLK}	SR	D	Clock Receive Pin External AC Coupling Capacitance	Values are nominal, valid for +/-50% tolerance	100	—	270	pF
C_{AC_TX}	SR	D	Transmit Lane External AC Coupling Capacitance	Values are nominal, valid for +/-50% tolerance	250	—	2000	pF
Receiver								
F_{RX}	CC	D	Receive Clock Rate	T_J = 150 °C	—	—	1.25	Gbps
		D		T_J = 165 °C	—	—	1	
$\|\Delta V_{I\_L}\|$	SR	T	Differential input voltage (peak to peak)	—	200	—	1000	mV
$R_{V\_L\_Rx}$	CC	D	Differential Terminating resistance	—	81	100	120	W

1. All Aurora electrical characteristics are valid from –40 °C to 150 °C, except where noted.
2. All specifications valid for maximum transmit data rate F_{TX}.
3. The minimum value of 400 mV is only valid for differential terminating resistance (R_{V_L}) = 99 ohm to 101 ohm. The differential output voltage swing tracks with the value of R_{V_L}.
4. Transmission line loss maximum value is specified for the maximum drive level of the Aurora transmit pad.

3.16 Power management

The power management module monitors the different power supplies as well as it generates the required internal supplies. The device can operate in the following configurations:

Table 37. Power management regulators

Device	External regulator(1)	Internal SMPS regulator (2)	Internal linear regulator external ballast	Internal linear regulator internal ballast	Auxiliary regulator(3)	Clamp regulator(3)	Internal standby regulator
SPC58NN84x	X	X	—	—	X	X	—

1. The application can select between the internal or external regulator mode, by controlling the EXTREG_SEL pin of the device. If EXTREG_SEL is connected to VDD_HV_IO_MAIN, the external regulator mode is selected.
2. Parts with SMPS enabled can only be used in this mode and EXTREG_SEL has to be set to V_{SS}.
3. In external regulator mode, the auxiliary and clamp regulators can be optionally enabled, to support the compensation of overshoots and undershoots in the supply. In internal regulator mode, the auxiliary and clamp regulators are always active. In SMPS regulator mode, the auxiliary and clamp regulators cannot be enabled.

3.16.1 Power management integration

Use the integration schemes provided below to ensure the proper device function, according to the selected regulator configuration.

The internal regulators are supplied by $V_{DD\_HV\_IO\_MAIN}$ supply and are used to generate V_{DD_LV} supply.

Place capacitances on the board as near as possible to the associated pins and limit the serial inductance of the board to less than 5 nH.

It is recommended to use the internal regulators only to supply the device itself.

Figure 13. External regulator mode

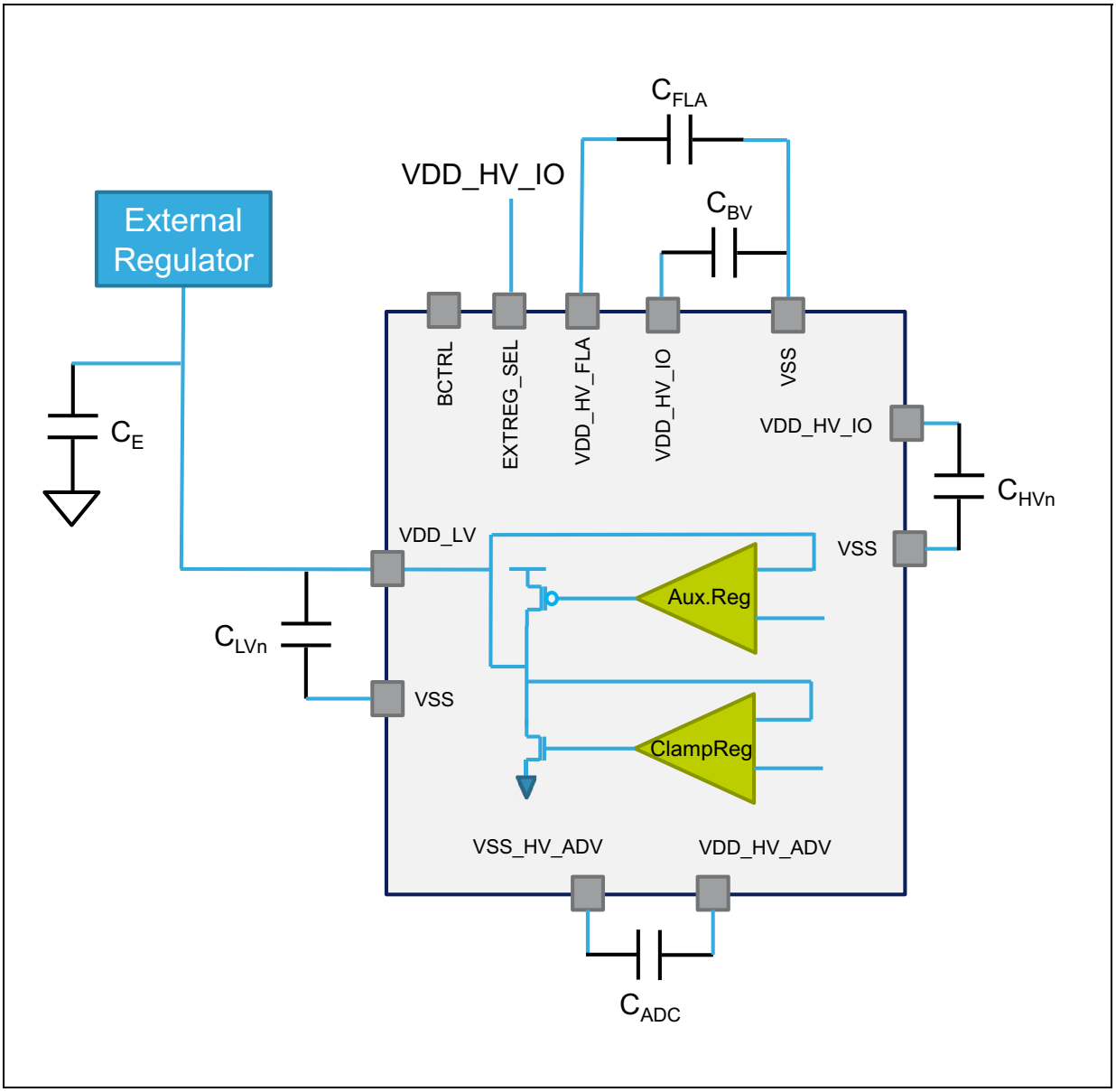
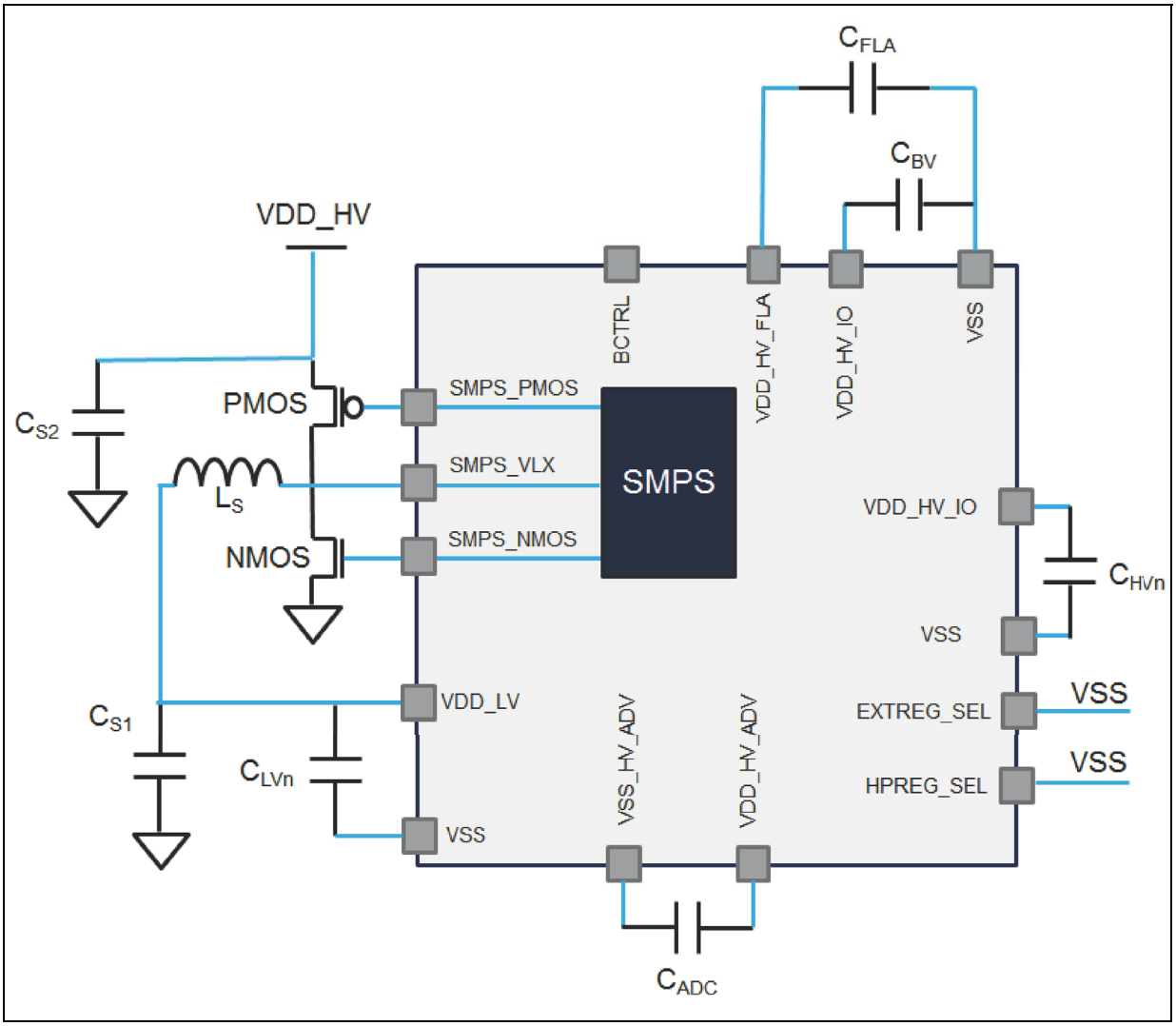


Figure 14. SMPS Regulator Mode



Note: Refer to the device pinout IO definition excel file for the list of available PMU control pins for each device and package.

Table 38. External components integration

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
Common Components								
C_E	SR	D	Internal voltage regulator stability external capacitance.[2] [3]		—	2× 2.2	—	µF
R_E	SR	D	Stability capacitor equivalent serial resistance	Total resistance including board track	5	—	50	mΩ
C_{LVn}	SR	D	Internal voltage regulator decoupling external capacitance[2] [4] [5]	Each V_{DD_LV}/V_{SS} pair	—	100	—	nF

Table 38. External components integration (continued)

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
R_{LVn}	SR	D	Stability capacitor equivalent serial resistance	—	—	—	50	mΩ
C_{BV}	SR	D	Bulk capacitance for HV supply[2]	on one $V_{DD\_HV\_IO\_MAIN}$/ V_{SS} pair	—	4.7	—	µF
C_{HVn}	SR	D	Decoupling capacitance for ballast and IOs[2]	on all $V_{DD\_HV\_IO}$/V_{SS} and $V_{DD\_HV\_ADR}$/V_{SS} pairs	—	100	—	nF
C_{FLA}	SR	D	Decoupling capacitance for Flash supply[2][6]	—	—	10	—	nF
C_{ADC}	SR	D	ADC supply external capacitance[2] [6]	$V_{DD\_HV\_ADV}$/$V_{SS\_HV\_ADV}$ pair.	—	2.2	—	µF
SMPS Regulator Mode								
Common Configuration[7]								
PMOS	SR	D	Recommended PMOS transistor for SMPS mode	PMPB100XPEA				
NMOS	SR	D	Recommended NMOS transistor for SMPS mode	PMPB55XNEA				
C_{S2}	SR	D	SMPS External capacitance on HV supply[2]	—	-50%	47[8]	+35%	µF
Option A								
C_{S1_A}	SR	D	SMPS External capacitance on LV supply[2]	—	-50%	2×10	+35%	µF
L_{S_A}	SR	D	SMPS External inductance	—	-30%	10	+30%	µH
Option B								
C_{S1_B}	SR	D	SMPS External capacitance on LV supply[9]	—	-35%	3×10	+35%	µF
L_{S_B}	SR	D	SMPS External inductance	—	-30%	4.7	+30%	µH

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_J = –40 / 165 °C, unless otherwise specified.
2. Recommended X7R or X5R ceramic –50% / +35% variation across process, temperature, voltage and after aging.
3. CE capacitance is required both in internal and external regulator mode.
4. For noise filtering, add a high frequency bypass capacitance of 10 nF.
5. For BGA applications it is recommended to implement at least 5 C_{LV} capacitances.
6. Recommended X7R capacitors. For noise filtering, add a high frequency bypass capacitance of 100 nF.
7. The application has to implement one of the two recommended combinations of external components for the SMPS regulator:
   PMOS, NMOS and CS2 (common), plus CS1_A and LS_A (option A), or
   PMOS, NMOS and CS2 (common), plus CS1_B and LS_B (option B).
8. The value of the capacitance on the HV supply reported in the datasheet is a general recommendation. The application can select a different number, based on the external regulator and emc requirements.
9. Recommended X7R or X5R ceramic –35% / +35% variation across process, temperature, voltage and after aging.

3.16.2 Voltage regulators

Table 39. Auxiliary regulator specifications

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
V_{AUX}	CC	P	Aux regulator output voltage	After trimming, internal regulator mode	1.08	1.18	1.21	V
	CC	P		After trimming, external regulator mode	1.03	1.12	1.16	
IDD_{AUX}	CC	T	Aux regulator current provided to V_{DD_LV} domain	—	—	—	250	mA
ΔIDD_{AUX}	CC	T	Aux regulator current variation	20 µs observation window	-100	—	100	mA
I_{AUXINT}	CC	D	Aux regulator current consumption	I_{MREG} = max	—	—	1.1	mA
		D		I_{MREG} = 0 mA	—	—	1.1	

Table 40. Clamp regulator specifications

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
V_{CLAMP}	CC	P	Clamp regulator output voltage	After trimming, internal regulator mode	1.17	1.21	1.32	V
	CC	P		After trimming, external regulator mode	1.24	1.28	1.39	
ΔIDD_{CLAMP}	CC	T	Clamp regulator current variation	20 µs observation window	-100	—	100	mA
$I_{CLAMPINT}$	CC	D	Clamp regulator current consumption	I_{MREG} = 0 mA	—	—	0.7	mA

Table 41. SMPS Regulator specifications

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
$V_{DD\_HV\_IO}$	SR	P	SMPS Regulator Supply Voltage[1]	—	4.5	—	5.5	V
V_{SMPS}	CC	P	SMPS regulator output voltage	After trimming, max load	1.14	1.20	1.26	V
δV_{SMPS}	CC	T	SMPS regulator output voltage tolerance	after trimming, < 20 µs observation window	-5%	—	+5%	—
F_{SMPS}	CC	T	SMPS regulator switching frequency	—	-5%	727	+5%	kHz
IDD_{SMPS}	CC	T	SMPS regulator current provided to V_{DD_LV} domain	—	—	—	1000	mA

Table 41. SMPS Regulator specifications (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
IDD_{CLAMP}	CC	D	SMPS regulator rush current sinked from VDD_HV_IO_MAIN domain during VDD_LV domain loading	Power-up condition	—	—	400	mA
ΔIDD_{SMPS} (2)	CC	T	SMPS regulator current variation	20 µs observation window	-200	—	200	mA

1. SMPS regulator is functional in the range 2.85 V < $V_{DD\_HV\_IO}$ < 4.5 V, but at a reduced efficiency.
2. Internal schemes must be used by the application (for example, frequency ramping feature enable) to ensure that incremental demands are made on the external power supply within the maximum value. Mbist/Lbist must be configured to avoid exceeding the maximum value.

3.16.3 Voltage monitors

The monitors and their associated levels for the device are given in *Table 42*. *Figure 15* illustrates the workings of voltage monitoring threshold.

Figure 15. Voltage monitor threshold definition

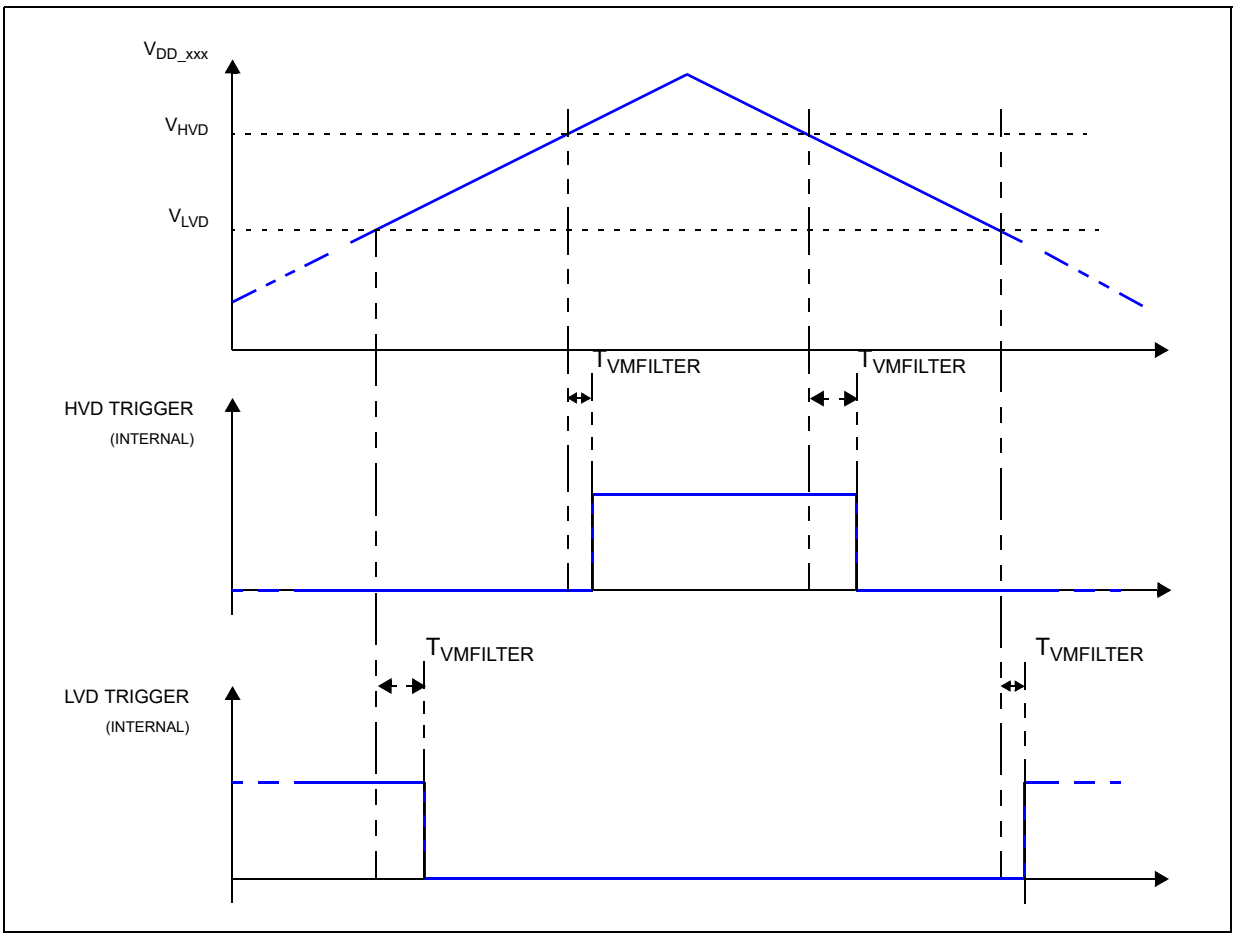


Table 42. Voltage monitor electrical characteristics

Symbol	C		Supply/Parameter[1]	Conditions	Value[2]			Unit
					Min	Typ	Max	
PowerOn Reset HV								
V_{POR200_C}	CC	P	$V_{DD\_HV\_IO\_MAIN}$	—	1.80	2.18	2.40	V
Minimum Voltage Detectors HV								
V_{MVD270_C}	CC	P	$V_{DD\_HV\_IO\_MAIN}$	—	2.71	2.76	2.80	V
V_{MVD270_F}	CC	P	$V_{DD\_HV\_FLA}$	—	2.71	2.76	2.80	V
Low Voltage Detectors HV								
V_{LVD290_C}	CC	P	$V_{DD\_HV\_IO\_MAIN}$	—	2.89	2.94	2.99	V
V_{LVD290_F}	CC	P	$V_{DD\_HV\_FLA}$	—	2.89	2.94	2.99	V
V_{LVD290_AD}	CC	P	$V_{DD\_HV\_ADV}$ (ADCSD pad)	—	2.89	2.94	2.99	V
V_{LVD290_AS}	CC	P	$V_{DD\_HV\_ADV}$ (ADCSAR pad)	—	2.89	2.94	2.99	V
V_{LVD290_IJ}	CC	P	$V_{DD\_HV\_IO\_JTAG}$	—	2.89	2.94	2.99	V
V_{LVD290_IF}	CC	P	$V_{DD\_HV\_IO\_FLEX}$	—	2.89	2.94	2.99	V
V_{LVD400_AD}	CC	P	$V_{DD\_HV\_ADV}$ (ADCSD pad)	—	4.15	4.23	4.31	V
V_{LVD400_AS}	CC	P	$V_{DD\_HV\_ADV}$ (ADCSAR pad)	—	4.15	4.23	4.31	V
V_{LVD400_IM}	CC	P	$V_{DD\_HV\_IO\_MAIN}$	—	4.15	4.23	4.31	V
V_{LVD400_IJ}	CC	P	$V_{DD\_HV\_IO\_JTAG}$		4.15	4.23	4.31	V
V_{LVD400_IF}	CC	P	$V_{DD\_HV\_IO\_FLEX}$	—	4.15	4.23	4.31	V
High Voltage Detectors HV								
V_{HVD400_C}	CC	P	$V_{DD\_HV\_IO\_MAIN}$		3.68	3.75	3.82	V
V_{HVD400_IJ}	CC	P	$V_{DD\_HV\_IO\_JTAG}$		3.68	3.75	3.82	V
V_{HVD400_IF}	CC	P	$V_{DD\_HV\_IO\_FLEX}$	—	3.68	3.75	3.82	V
Upper Voltage Detectors HV								
V_{UVD600_C}	CC	P	$V_{DD\_HV\_IO\_MAIN}$		5.72	5.82	5.92	V
V_{UVD600_F}	CC	P	$V_{DD\_HV\_FLA}$	—	5.72	5.82	5.92	V
V_{UVD600_IJ}	CC	P	$V_{DD\_HV\_IO\_JTAG}$	—	5.72	5.82	5.92	V
V_{UVD600_IF}	CC	P	$V_{DD\_HV\_IO\_FLEX}$	—	5.72	5.82	5.92	V
PowerOn Reset LV								
V_{POR031_C}	CC	P	V_{DD_LV}	—	0.29	0.60	0.97	V
Minimum Voltage Detectors LV								
V_{MVD082_C}	CC	P	V_{DD_LV}	—	0.85	0.88	0.91	V
V_{MVD082_B}	CC	P	$V_{DD\_LV\_BD}$	—	0.85	0.88	0.91	V
V_{MVD094_C}	CC	P	V_{DD_LV}	—	0.98	1.00	1.02	V
V_{MVD094_FA}	CC	P	V_{DD_LV} (Flash)	—	1.00	1.02	1.04	V

Table 42. Voltage monitor electrical characteristics (continued)

Symbol		C	Supply/Parameter[1]	Conditions	Value[2]			Unit
					Min	Typ	Max	
V_{MVD094_FB}	CC	P	V_{DD_LV} (Flash)	—	1.00	1.02	1.04	V
Low Voltage Detectors LV								
V_{LVD100_C}	CC	P	V_{DD_LV}	—	1.06	1.08	1.11	V
V_{LVD100_F}	CC	P	V_{DD_LV} (Flash)	—	1.08	1.10	1.12	V
High Voltage Detectors LV								
V_{HVD134_C}	CC	P	V_{DD_LV}	—	1.28	1.31	1.33	V
Upper Voltage Detectors LV								
V_{UVD140_C}	CC	P	V_{DD_LV}	—	1.34	1.37	1.39	V
V_{UVD140_F}	CC	P	V_{DD_LV} (Flash)	—	1.34	1.37	1.39	V
Common								
$T_{VMFILTER}$	CC	D	Voltage monitor filter[3]	—	5	—	25	µs

1. Even if LVD/HVD monitor reaction is configurable, the application ensures that the device remains in the operative condition range. If the internal LVDx monitors are disabled by the application, then an external voltage monitor with minimum threshold of VDD_LV (min) = 1.08 V (measured at the device pad) has to be implemented.
For HVDx, if the application disables them, then they need to grant that VDD_LV and VDD_HV voltage levels stay withing the limitations provided in *Section 3.2: Absolute maximum ratings*.
2. The values reported are Trimmed values, where applicable.
3. See *Figure 15*. Transitions shorter than minimum are filtered. Transitions longer than maximum are not filtered, and will be delayed by $T_{VMFILTER}$ time. Transitions between minimum and maximum can be filtered or not filtered, according to temperature, process and voltage variations.

3.17 Flash memory

The following table shows the Wait State configuration.

Table 43. Wait State configuration

APC	RWSC	Frequency range (MHz)
000(1)	0	f≤33
	1	f≤66
	2	f≤100
	3	f≤133
	4	f≤167
	5	f≤200
100(2)	0	f≤33
	1	f≤66
	2	f≤100
	3	f≤133
	4	f≤167
	5	f≤200
001(3)	2	55<f≤80
	3	55<f≤120
	4	55<f≤160
	5	55<f≤200

1. STD pipelined.
2. No pipeline.
3. Pipeline with 1 Tck address anticipation.

The following table shows the Program/Erase Characteristics.

Table 44. Flash memory program and erase specifications

Symbol	Characteristics(1)(2)	Value								Unit
		Typ(3)	C	Initial max			Typical end of life(4)	Lifetime max(5)	C	
				25 °C (6)	All temp (7)	C		< 1 K cycles / ≤ 250 K cycles		
$t_{dwprogram}$	Double Word (64 bits) program time EEPROM (partitions 2, 3, 4) [Packaged part]	55	C	130	—	—	140	650	C	µs
$t_{pprogram}$	Page (256 bits) program time	76	C	240	—	—	255	1000	C	µs

Table 44. Flash memory program and erase specifications (continued)

Symbol	Characteristics[1][2]	Value									Unit
		Typ[3]	C	Initial max			Typical end of life[4]	Lifetime max[5]		C	
				25 °C [6]	All temp [7]	C		< 1 K cycles	≤ 250 K cycles		
$t_{pprogrameep}$	Page (256 bits) program time EEPROM (partitions 2, 3, 4) [Packaged part]	90	C	300	—	—	315	1300		C	µs
$t_{qprogram}$	Quad Page (1024 bits) program time	220	C	840	1200	P	850	2000		C	µs
$t_{qprogrameep}$	Quad Page (1024 bits) program time EEPROM (partitions 2, 3, 4) [Packaged part]	306	C	1200	1800	P	1270	2600		C	µs
$t_{16kpperase}$	16 KB block pre-program and erase time	190	C	450	500	P	250	1000	—	C	ms
$t_{32kpperase}$	32 KB block pre-program and erase time	250	C	520	600	P	310	1200	—	C	ms
$t_{64kpperase}$	64 KB block pre-program and erase time	360	C	700	750	P	420	1600	—	C	ms
$t_{128kpperase}$	128 KB block pre-program and erase time	600	C	1300	1600	P	800	4000	—	C	ms
$t_{256kpperase}$	256 KB block pre-program and erase time	1050	C	1800	2400	P	1600	4000	—	C	ms
$t_{16kprogram}$	16 KB block program time	25	C	45	50	P	40	1000	—	C	ms
$t_{32kprogram}$	32 KB block program time	50	C	90	100	P	75	1200	—	C	ms
$t_{64kprogram}$	64 KB block program time	102	C	175	200	P	150	1600	—	C	ms
$t_{128kprogram}$	128 KB block program time	205	C	350	430	P	300	2000	—	C	ms
$t_{256kprogram}$	256 KB block program time	410	C	700	850	P	590	4000	—	C	ms
$t_{64kprogrameep}$	Program 64 KB EEPROM (partitions 2,3) [Packaged part]	120	C	200	300	P	330	2275		C	ms
$t_{64keraseeep}$	Erase 64 KB EEPROM (partition 2,3) [Packaged part]	530	C	910	1150	P	1040	4700		C	ms
$t_{16kprogrameep}$	Program 16 KB EEPROM (partition 4)	30	C	52	75	P	84	2275		C	ms
$t_{16keraseeep}$	Erase 16 KB EEPROM (partition 4)	225	C	645	715	P	520	4700		C	ms
t_{prr}	Program rate[8]	1.7	C	2.8	3.40	C	2.4	—		C	s/MB

Table 44. Flash memory program and erase specifications (continued)

Symbol	Characteristics[1][2]	Value									Unit
		Typ[3]	C	Initial max			Typical end of life[4]	Lifetime max[5]		C	
				25 °C [6]	All temp [7]	C		< 1 K cycles	≤ 250 K cycles		
t_{err}	Erase rate[8]	4.8	C	7.2	9.6	C	6.4	—		C	s/MB
t_{prfm}	Program rate Factory Mode[8]	1.12	C	1.4	1.6	C	—	—		C	s/MB
t_{erfm}	Erase rate Factory Mode[8]	4.0	C	5.2	5.8	C	—	—		C	s/MB
$t_{ffprogram}$	Full flash programming time[9]	12.0	C	17.8	22.0	P	15.4	—	—	C	s
$t_{fferase}$	Full flash erasing time[9]	25.0	C	40.0	50.0	P	40.0	—	—	C	s
t_{ESRT}	Erase suspend request rate[10]	200	T	—	—	—	—	—		—	µs
t_{PSRT}	Program suspend request rate[10]	30	T	—	—	—	—	—		—	µs
t_{AMRT}	Array Integrity Check - Margin Read suspend request rate	15	T	—	—	—	—	—		—	µs
t_{PSUS}	Program suspend latency[11]	—	—	—	—	—	—	12		T	µs
t_{ESUS}	Erase suspend latency[11]	—	—	—	—	—	—	22		T	µs
t_{AIC0S}	Array Integrity Check (6.0 MB, sequential)[12]	40	T	—	—	—	—	—	—	—	ms
$t_{AIC256KS}$	Array Integrity Check (256 KB, sequential)[12]	1.5	T	—	—	—	—	—	—	—	ms
t_{AIC0P}	Array Integrity Check (6.0 MB, proprietary)[12]	4.0	T	—	—	—	—	—	—	—	s
t_{MR0S}	Margin Read (6.0 MB, sequential)[12]	120	T	—	—	—	—	—	—	—	ms
$t_{MR256KS}$	Margin Read (256 KB, sequential)[12]	4.0	T	—	—	—	—	—	—	—	ms

1. Characteristics are valid both for Data Flash and Code Flash, unless specified in the characteristics column.
2. Actual hardware operation times; this does not include software overhead.
3. Typical program and erase times assume nominal supply values and operation at 25 °C.
4. Typical End of Life program and erase times represent the median performance and assume nominal supply values. Typical End of Life program and erase values may be used for throughput calculations. These values are characteristic, but not tested.
5. Lifetime maximum program & erase times apply across the voltages and temperatures and occur after the specified number of program/erase cycles. These maximum values are characterized but not tested or guaranteed.
6. Initial factory condition: < 100 program/erase cycles, 25 °C typical junction temperature and nominal (± 5%) supply voltages.
7. Initial maximum “All temp” program and erase times provide guidance for time-out limits used in the factory and apply for less than or equal to 100 program or erase cycles, –40 °C < TJ < 150 °C junction temperature and nominal (± 5%) supply voltages.

8. Rate computed based on 256 KB sectors.
9. Only code sectors, not including EEPROM, neither UTEST and BAF.
10. Time between suspend resume and next suspend. Value stated actually represents Min value specification.
11. Timings guaranteed by design.
12. AIC is done using system clock, thus all timing is dependent on system frequency and number of wait states. Timing in the table is calculated at max frequency.

All the Flash operations require the presence of the system clock for internal synchronization. About 50 synchronization cycles are needed: this means that the timings of the previous table can be longer if a low frequency system clock is used.

Table 45. Flash memory Life Specification

Symbol	Characteristics(1) (2)	Value				Unit
		Min	C	Typ	C	
N_{CER16K}	16 KB CODE Flash endurance	10	—	100	—	Kcycles
N_{CER32K}	32 KB CODE Flash endurance	10	—	100	—	Kcycles
N_{CER64K}	64 KB CODE Flash endurance	10	—	100	—	Kcycles
$N_{CER128K}$	128 KB CODE Flash endurance	1	—	100	—	Kcycles
$N_{CER256K}$	256 KB CODE Flash endurance	1	—	100	—	Kcycles
	256 KB CODE Flash endurance(3)	10	—	100	—	Kcycles
N_{DER64K}	64 KB DATA EEPROM Flash endurance	250	—	—	—	Kcycles
N_{DER16K}	16 KB HSM DATA EEPROM Flash endurance	100	—	—	—	Kcycles
t_{DR1k}	Minimum data retention Blocks with 0 - 1,000 P/E cycles	25	—	—	—	Years
t_{DR10k}	Minimum data retention Blocks with 1,001 - 10,000 P/E cycles	20	—	—	—	Years
t_{DR100k}	Minimum data retention Blocks with 10,001 - 100,000 P/E cycles	15	—	—	—	Years
t_{DR250k}	Minimum data retention Blocks with 100,001 - 250,000 P/E cycles	10	—	—	—	Years

1. Program and erase cycles supported across specified temperature specifications.
2. It is recommended that the application enables the core cache memory.
3. 10K cycles on 4-256 KB blocks is not intended for production. Reduced reliability and degraded erase time are possible.

3.18 AC Specifications

All AC timing specifications are valid up to 150 °C, except where explicitly noted.

3.18.1 Debug and calibration interface timing

3.18.1.1 JTAG interface timing

Table 46. JTAG pin AC electrical characteristics

#	Symbol		C	Characteristic	Value(1),(2)		Unit
					Min	Max	
1	t_{JCYC}	CC	D	TCK cycle time	100	—	ns
2	t_{JDC}	CC	T	TCK clock pulse width	40	60	%
3	$t_{TCKRISE}$	CC	D	TCK rise and fall times (40%–70%)	—	3	ns
4	t_{TMSS}, t_{TDIS}	CC	D	TMS, TDI data setup time	5	—	ns
5	t_{TMSH}, t_{TDIH}	CC	D	TMS, TDI data hold time	5	—	ns
6	t_{TDOV}	CC	D	TCK low to TDO data valid	—	15(3)	ns
7	t_{TDOI}	CC	D	TCK low to TDO data invalid	0	—	ns
8	t_{TDOHZ}	CC	D	TCK low to TDO high impedance	—	15	ns
9	t_{JCMPPW}	CC	D	JCOMP assertion time	100	—	ns
10	t_{JCMPS}	CC	D	JCOMP setup time to TCK low	40	—	ns
11	t_{BSDV}	CC	D	TCK falling edge to output valid	—	600(4)	ns
12	t_{BSDVZ}	CC	D	TCK falling edge to output valid out of high impedance	—	600	ns
13	t_{BSDHZ}	CC	D	TCK falling edge to output high impedance	—	600	ns
14	t_{BSDST}	CC	D	Boundary scan input valid to TCK rising edge	15	—	ns
15	t_{BSDHT}	CC	D	TCK rising edge to boundary scan input invalid	15	—	ns

1. These specifications apply to JTAG boundary scan only. See *Table 47* for functional specifications.
2. JTAG timing specified at $V_{DD\_HV\_IO\_JTAG}$ = 4.0 to 5.5 V and max. loading per pad type as specified in the I/O section of the datasheet.
3. Timing includes TCK pad delay, clock tree delay, logic delay and TDO output pad delay.
4. Applies to all pins, limited by pad slew rate. Refer to IO delay and transition specification and add 20 ns for JTAG delay.

Figure 16. JTAG test clock input timing

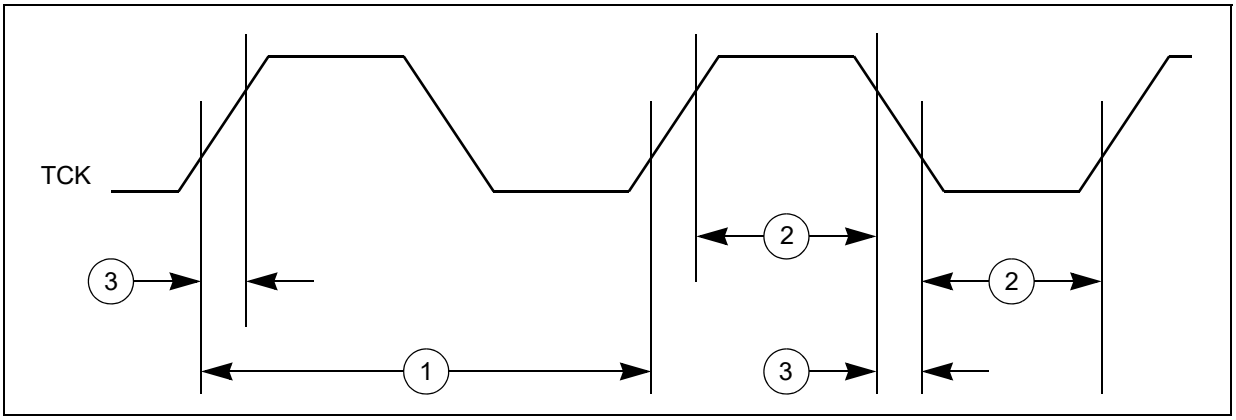


Figure 17. JTAG test access port timing

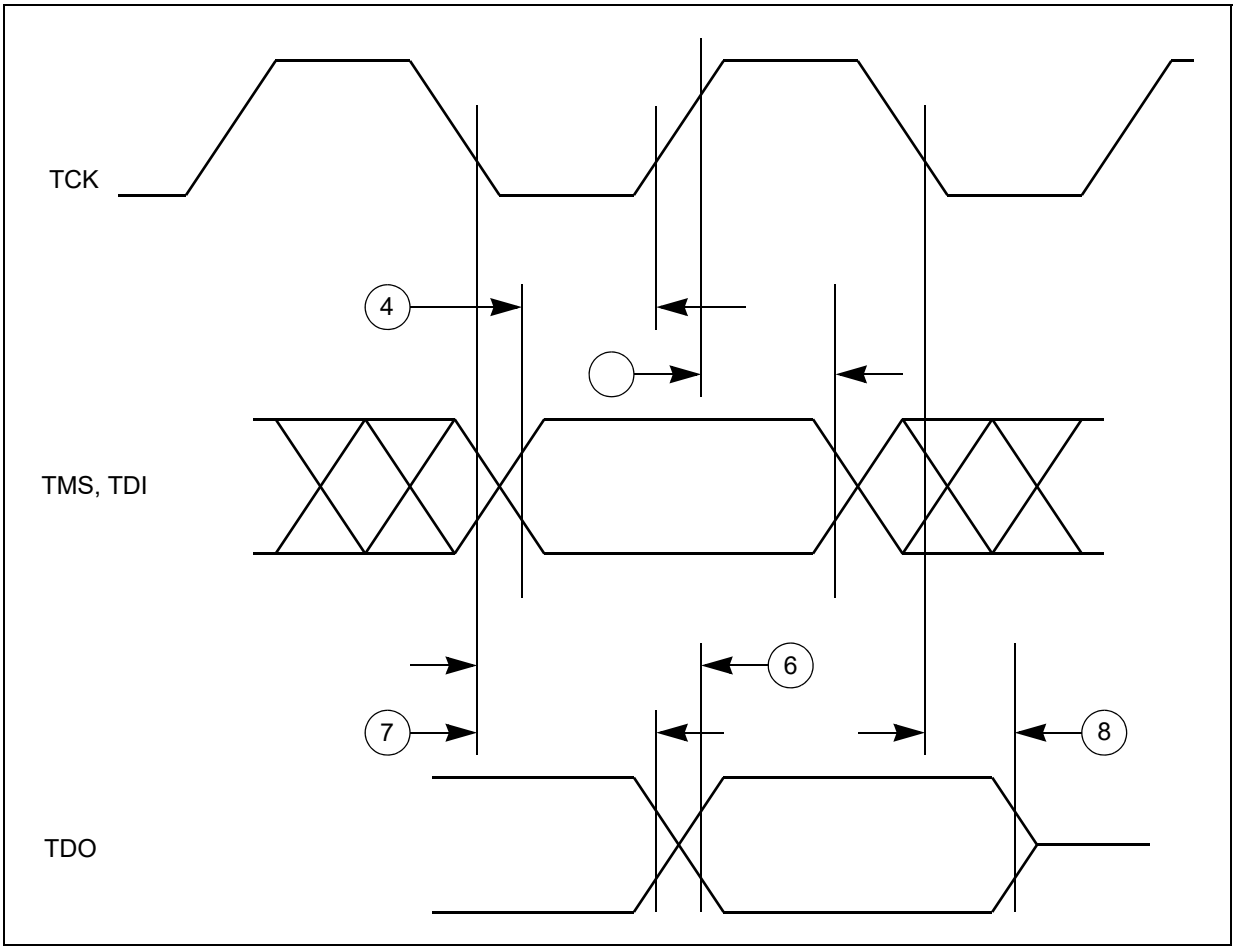


Figure 18. JTAG JCOMP timing

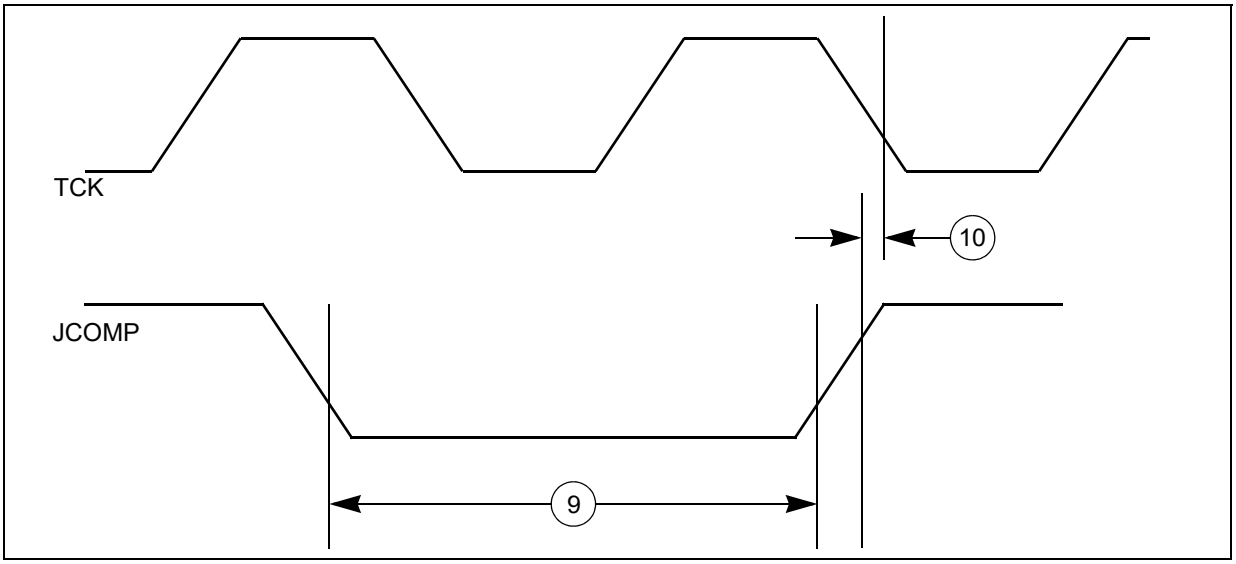
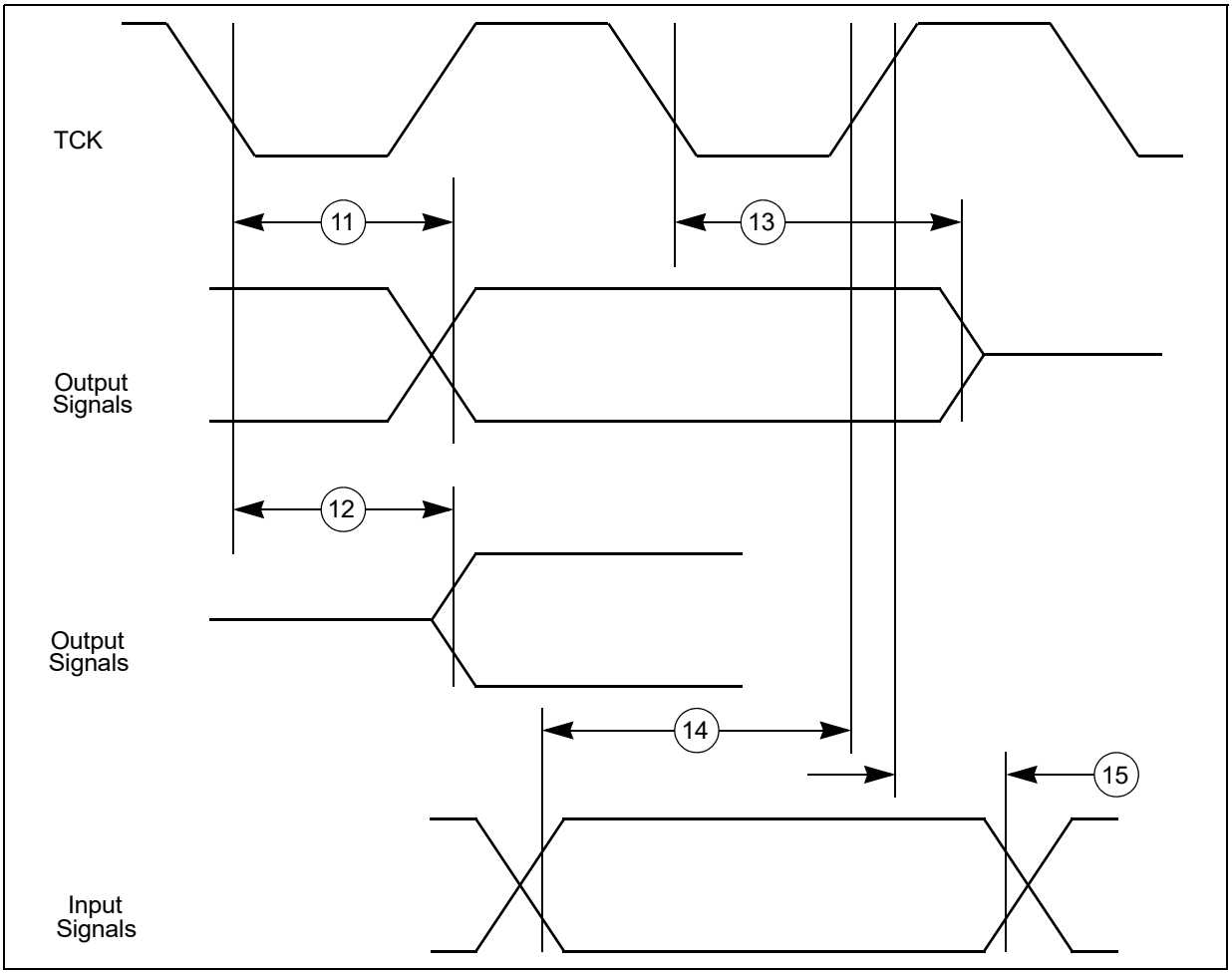


Figure 19. JTAG boundary scan timing



3.18.1.2 Nexus interface timing

Table 47. Nexus debug port timing

#	Symbol		C	Characteristic	Value(1)		Unit
					Min	Max	
7	t_{EVTIPW}	CC	D	$\overline{EVTI}$ pulse width	4	—	t_{CYC}(2)
8	t_{EVTOPW}	CC	D	$\overline{EVTO}$ pulse width	40	—	ns
9	t_{TCYC}	CC	D	TCK cycle time	2(3),(4)	—	t_{CYC}(2)
				Absolute minimum TCK cycle time(5) (TDO sampled on posedge of TCK)	50(6)	—	ns
				Absolute minimum TCK cycle time(7) (TDO sampled on negedge of TCK)	25(6)	—	
11	t_{NTDIS}	CC	D	TDI data setup time	5	—	ns
12	t_{NTDIH}	CC	D	TDI data hold time	5	—	ns
13	t_{NTMSS}	CC	D	TMS data setup time	5	—	ns
14	t_{NTMSH}	CC	D	TMS data hold time	5	—	ns
15	—	CC	D	TDO propagation delay from falling edge of TCK(8)	—	20	ns
16	—	CC	D	TDO hold time with respect to TCK falling edge (minimum TDO propagation delay)	2.25	—	ns

1. Nexus timing specified at $V_{DD\_HV\_IO\_JTAG}$ = 3.0 V to 5.5 V, and maximum loading per pad type as specified in the I/O section of the data sheet.
2. t_{CYC} is system clock period.
3. Achieving the absolute minimum TCK cycle time may require a maximum clock speed (system frequency / 8) that is less than the maximum functional capability of the design (system frequency / 4) depending on the actual peripheral frequency being used. To ensure proper operation TCK frequency should be set to the peripheral frequency divided by a number greater than or equal to that specified here.
4. This is a functionally allowable feature. However, it may be limited by the maximum frequency specified by the Absolute minimum TCK period specification.
5. This value is TDO propagation time 36 ns + 4 ns setup time to sampling edge.
6. This may require a maximum clock speed (system frequency / 8) that is less than the maximum functional capability of the design (system frequency / 4) depending on the actual system frequency being used.
7. This value is TDO propagation time 16 ns + 4 ns setup time to sampling edge.
8. Timing includes TCK pad delay, clock tree delay, logic delay and TDO output pad delay.

Figure 20. Nexus event trigger and test clock timings

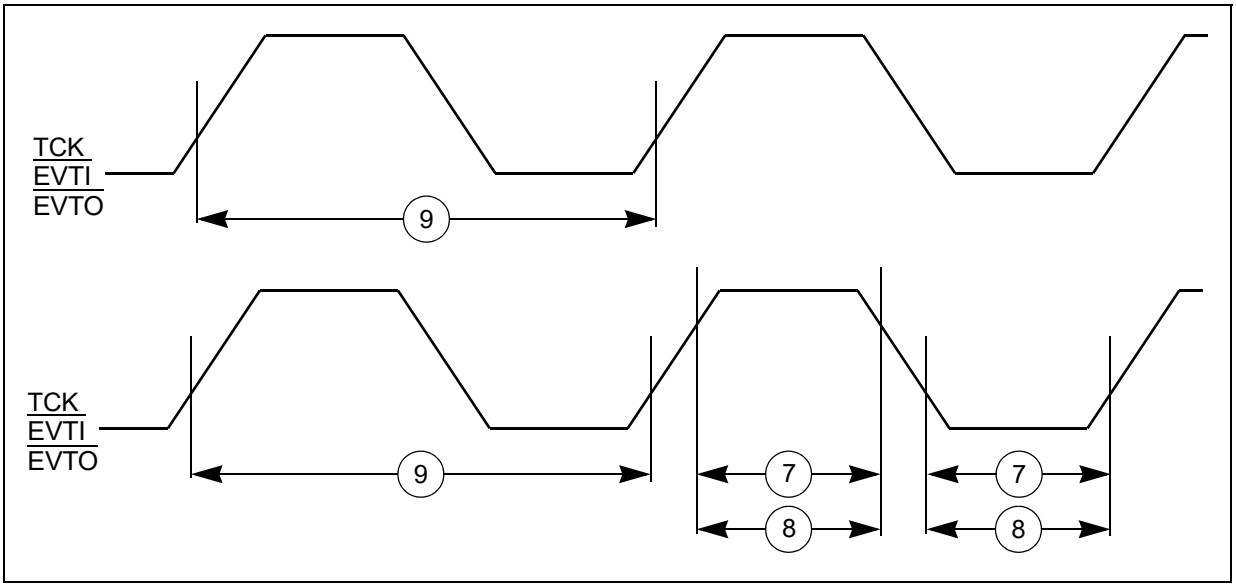
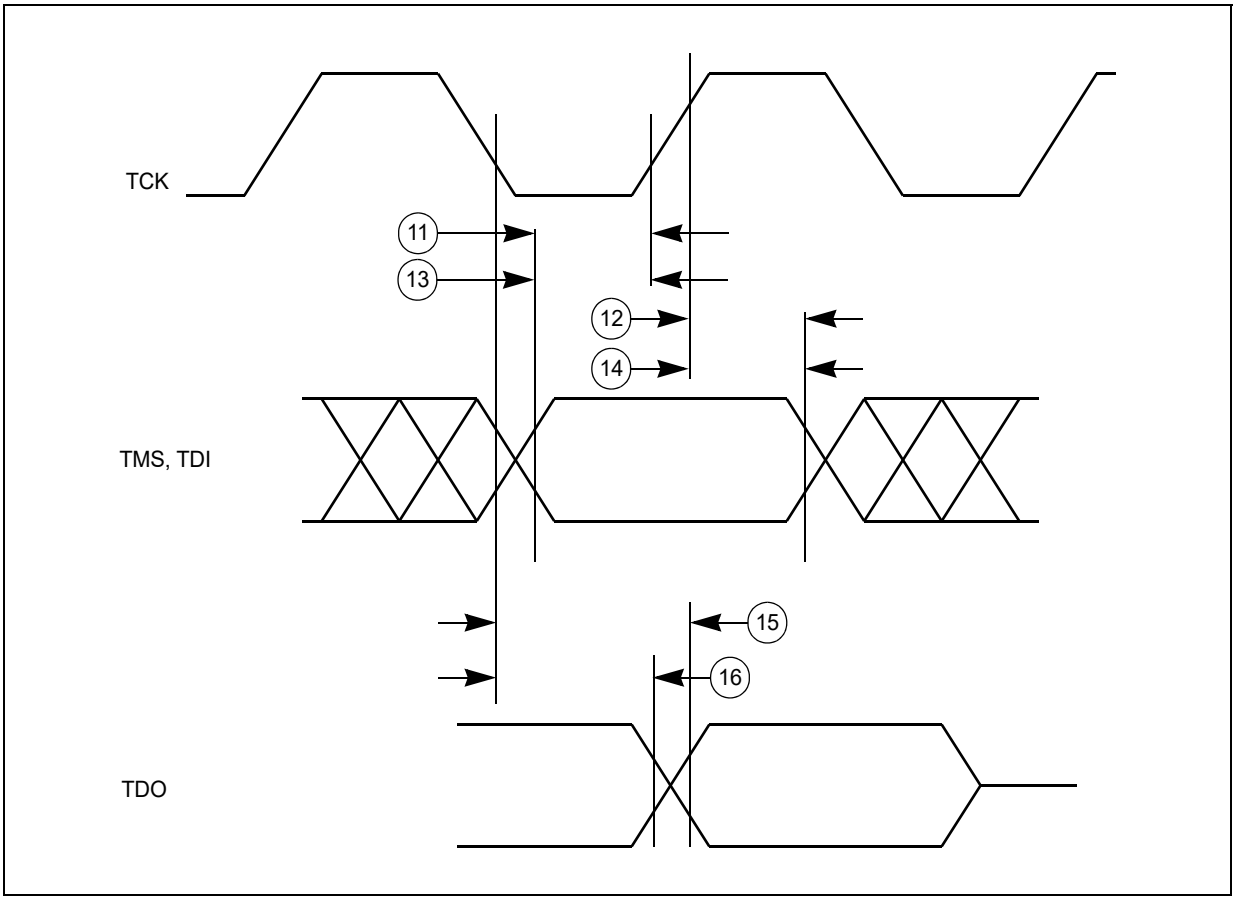


Figure 21. Nexus TDI, TMS, TDO timing



3.18.1.3 Aurora LVDS interface timing

Table 48. Aurora LVDS interface timing specifications

Symbol		C	Parameter	Value			Unit
				Min	Typ	Max	
Data Rate							
—	SR	T	Data rate	—	—	1250	Mbps
STARTUP							
t_{STRT_BIAS}	CC	T	Bias startup time(1)	—	—	5	µs
t_{STRT_TX}	CC	T	Transmitter startup time(2)	—	—	5	µs
t_{STRT_RX}	CC	T	Receiver startup time(3)	—	—	4	µs

1. Startup time is defined as the time taken by LVDS current reference block for settling bias current after its pwr_down (power down) has been deasserted. LVDS functionality is guaranteed only after the startup time.
2. Startup time is defined as the time taken by LVDS transmitter for settling after its pwr_down (power down) has been deasserted. Here it is assumed that current reference is already stable (see Bias start-up time). LVDS functionality is guaranteed only after the startup time.
3. Startup time is defined as the time taken by LVDS receiver for settling after its pwr_down (power down) has been deasserted. Here it is assumed that current reference is already stable (see Bias start-up time). LVDS functionality is guaranteed only after the startup time.

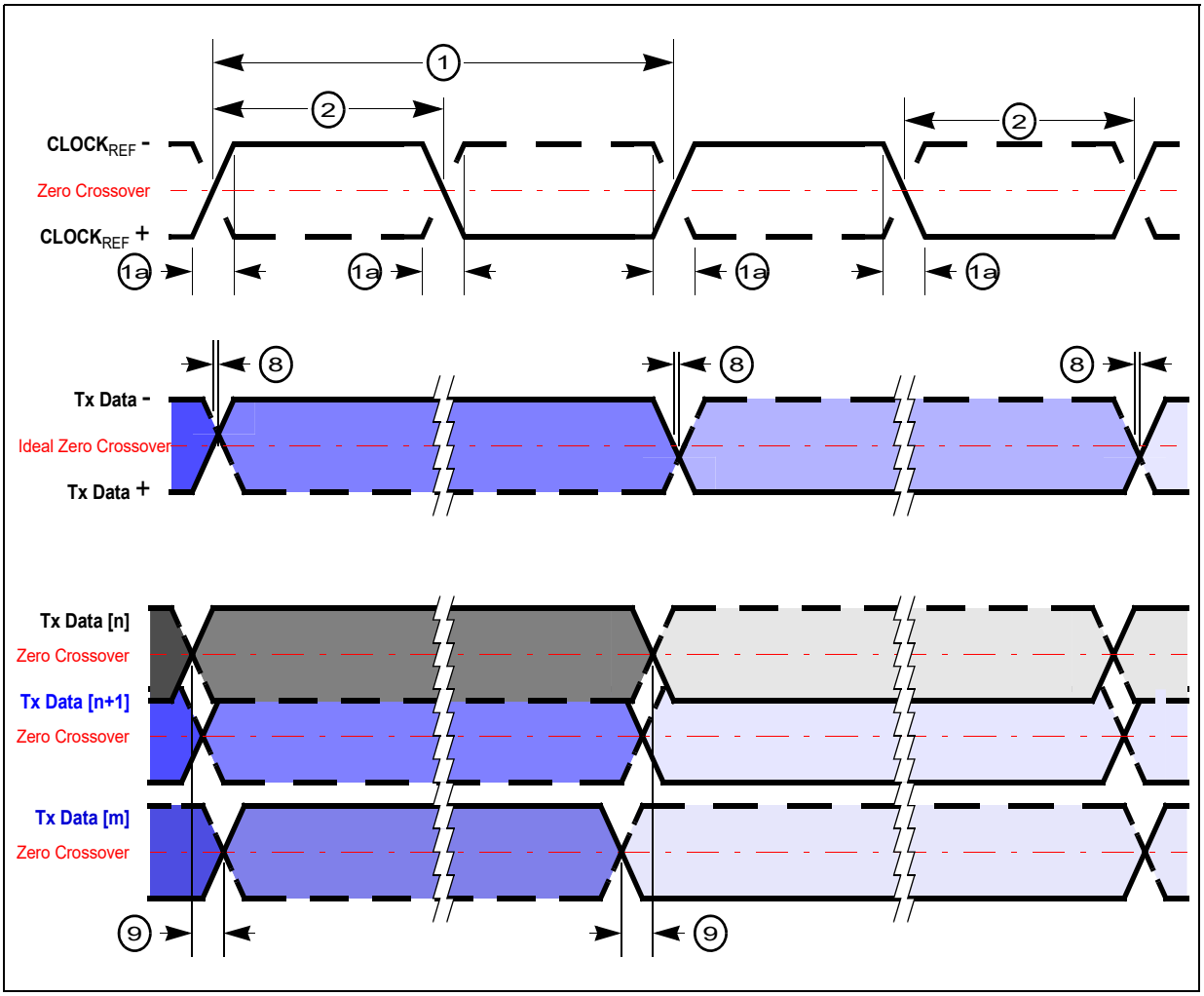
3.18.1.4 Aurora debug port timing

Table 49. Aurora debug port timing

#	Symbol		C	Characteristic		Value		Unit
						Min	Max	
1	t_{REFCLK}	CC	T	Reference clock frequency		625	1250	MHz
1a	t_{MCYC}	CC	T	Reference clock rise/fall time		—	400	ps
2	t_{RCDC}	CC	D	Reference clock duty cycle		45	55	%
3	J_{RC}	CC	D	Reference clock jitter		—	40	ps
4	$t_{STABILITY}$	CC	D	Reference clock stability		50	—	PPM
5	BER	CC	D	Bit error rate		—	10^{-12}	—
6	J_D	SR	D	Transmit lane deterministic jitter		—	0.17	OUI
7	J_T	SR	D	Transmit lane total jitter		—	0.35	OUI
8	S_O	CC	T	Differential output skew		—	20	ps
9	S_{MO}	CC	T	Lane to lane output skew		—	1000	ps
10	OUI	CC	D	Aurora lane unit interval(1)	625 Mbps	1600	1600	ps
			D		1.25 Gbps	800	800	

1. ± +/-100 PPM

Figure 22. Aurora timings



3.18.1.5 External interrupt timing (IRQ pin)

Table 50. External interrupt timing

Characteristic	Symbol	Min	Max	Unit
IRQ Pulse Width Low	t_{IPWL}	3	—	t_{cyc}
IRQ Pulse Width High	t_{IPWH}	3	—	t_{cyc}
IRQ Edge to Edge Time(1)	t_{ICYC}	6	—	t_{cyc}

1. Applies when IRQ pins are configured for rising edge or falling edge events, but not both.

Figure 23. External interrupt timing

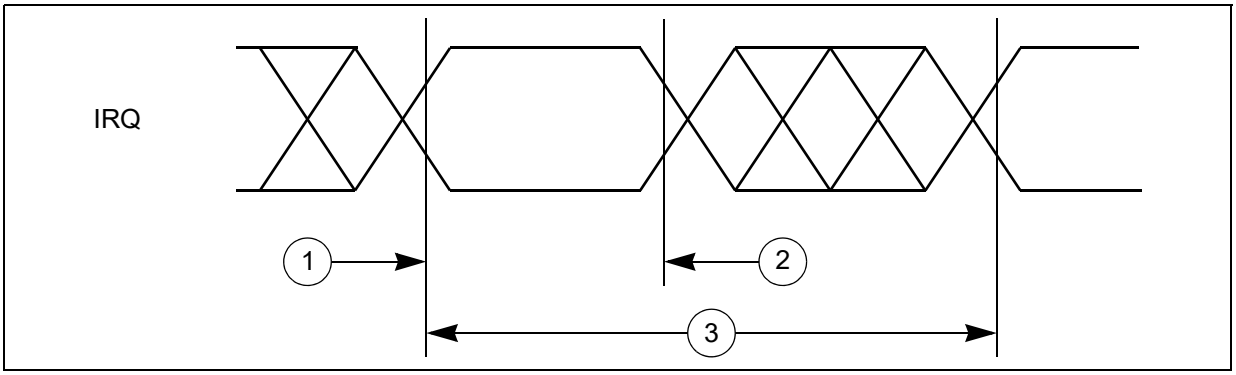
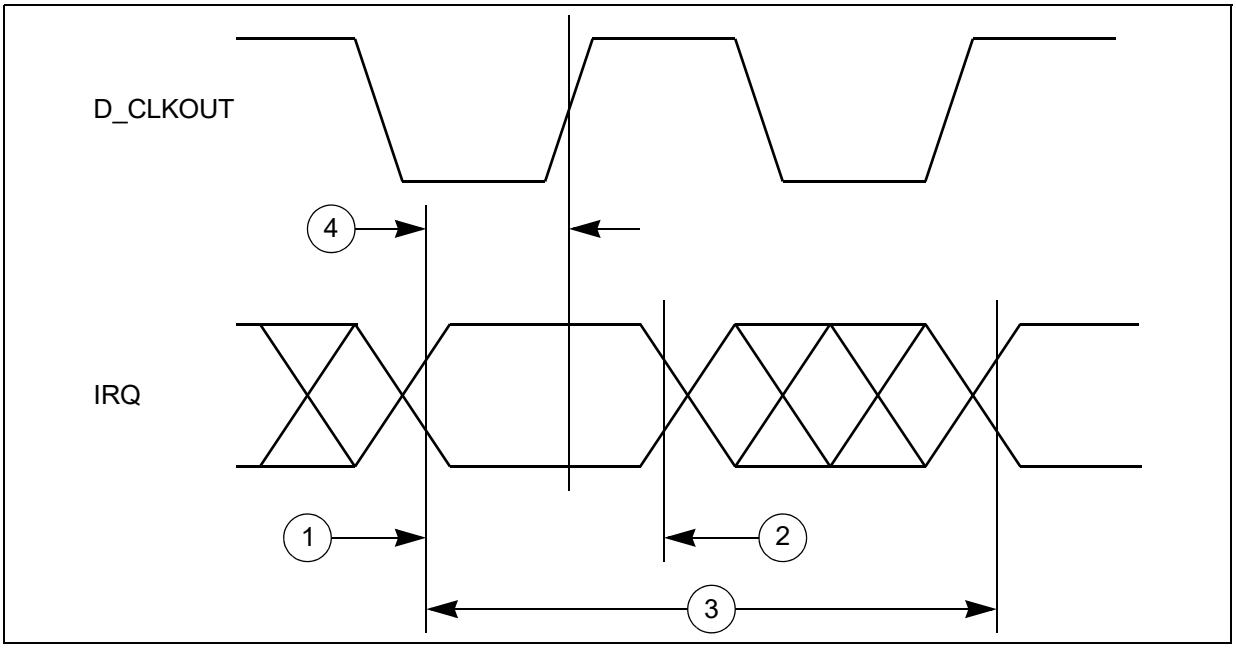


Figure 24. External interrupt timing



3.18.2 DSPI timing with CMOS and LVDS pads

Note: DSPI in TSB mode with LVDS pads can be used to implement Micro Second Channel bus protocol.

DSPI channel frequency support is shown in *Table 51*.

Timing specifications are shown in the tables below.

Table 51. DSPI channel frequency support

DSPI use mode[1]			Max usable frequency (MHz)[2],[3]
CMOS (Master mode)	Full duplex – Classic timing (*Table 52*)	DSPI_0, DSPI_3, DSPI_5, DSPI_6	12
		DSPI_1, DSPI_2, DSPI_4, DSPI_9	17
	Full duplex – Modified timing (*Table 53*)	DSPI_0, DSPI_3, DSPI_5, DSPI_6	12
		DSPI_1, DSPI_2, DSPI_4, DSPI_9	30
	Output only mode (SCK/SOUT/PCS) (*Table 52* and *Table 53*))	—	30
	Output only mode TSB mode (SCK/SOUT/PCS)	—	30
LVDS (Master mode)	Full duplex – Modified timing (*Table 54*)	—	33
	Output only mode TSB mode (SCK/SOUT/PCS) (*Table 55*)	—	40
CMOS (Slave mode Full duplex) (*Table 57*)		—	16

1. Each DSPI module can be configured to use different pins for the interface. Refer to the device pinout Microsoft Excel file attached to the IO_Definition document for the available combinations. It is not possible to reach the maximum performance with every possible combination of pins.
2. Maximum usable frequency can be achieved if used with fastest configuration of the highest drive pads.
3. Maximum usable frequency does not take into account external device propagation delay.

3.18.2.1 DSPI master mode full duplex timing with CMOS and LVDS pads

3.18.2.1.1 DSPI CMOS master mode – classic timing

Note: In the following table, all output timing is worst case and includes the mismatching of rise and fall times of the output pads.

Table 52. DSPI CMOS master classic timing (full duplex and output only) MTFE = 0, CPHA = 0 or 1

#	Symbol		C	Characteristic	Condition		Value[1]		Unit
					Pad drive[2]	Load (C_L)	Min	Max	
1	t_{SCK}	CC	D	SCK cycle time	SCK drive strength				
					Very strong	25 pF	59.0	—	ns
					Strong	50 pF	80.0	—	
					Medium	50 pF	200.0	—	

Table 52. DSPI CMOS master classic timing (full duplex and output only) MTFE = 0, CPHA = 0 or 1 (continued)

#	Symbol		C	Characteristic	Condition		Value(1)		Unit
					Pad drive(2)	Load (C_L)	Min	Max	
2	t_{CSC}	CC	D	PCS to SCK delay	SCK and PCS drive strength				
					Very strong	25 pF	$(N^{(3)} \times t_{SYS}^{(4)}) - 16$	—	ns
					Strong	50 pF	$(N^{(3)} \times t_{SYS}^{(4)}) - 16$	—	
					Medium	50 pF	$(N^{(3)} \times t_{SYS}^{(4)}) - 16$	—	
					PCS medium and SCK strong	PCS = 50 pF SCK = 50 pF	$(N^{(3)} \times t_{SYS}^{(4)}) - 29$	—	
3	t_{ASC}	CC	D	After SCK delay	SCK and PCS drive strength				
					Very strong	PCS = 0 pF SCK = 50 pF	$(M^{(5)} \times t_{SYS}^{(4)}) - 35$	—	ns
					Strong	PCS = 0 pF SCK = 50 pF	$(M^{(5)} \times t_{SYS}^{(4)}) - 35$	—	
					Medium	PCS = 0 pF SCK = 50 pF	$(M^{(5)} \times t_{SYS}^{(4)}) - 35$	—	
					PCS medium and SCK strong	PCS = 0 pF SCK = 50 pF	$(M^{(5)} \times t_{SYS}^{(4)}) - 35$	—	
4	t_{SDC}	CC	D	SCK duty cycle(6)	SCK drive strength				
					Very strong	0 pF	$^1/_2t_{SCK} - 2$	$^1/_2t_{SCK} + 2$	ns
					Strong	0 pF	$^1/_2t_{SCK} - 2$	$^1/_2t_{SCK} + 2$	
					Medium	0 pF	$^1/_2t_{SCK} - 5$	$^1/_2t_{SCK} + 5$	
PCS strobe timing									
5	t_{PCSC}	CC	D	PCSx to $\overline{PCSS}$ time(7)	PCS and PCSS drive strength				
					Strong	25 pF	16.0	—	ns
6	t_{PASC}	CC	D	$\overline{PCSS}$ to PCSx time(7)	PCS and PCSS drive strength				
					Strong	25 pF	16.0	—	ns
SIN setup time									
7	t_{SUI}	CC	D	SIN setup time to SCK(8)	SCK drive strength				
					Very strong	25 pF	25.0	—	ns
					Strong	50 pF	31.0	—	
					Medium	50 pF	52.0	—	

Table 52. DSPI CMOS master classic timing (full duplex and output only) MTFE = 0, CPHA = 0 or 1 (continued)

#	Symbol	C	Characteristic	Condition		Value[1]		Unit
				Pad drive[2]	Load (C_L)	Min	Max	
SIN hold time								
8	t_{HI}	CC	D	SIN hold time from SCK[8]	SCK drive strength			
					Very strong	0 pF	–1.0	—	ns
					Strong	0 pF	–1.0	—	
					Medium	0 pF	–1.0	—	
SOUT data valid time (after SCK edge)								
9	t_{SUO}	CC	D	SOUT data valid time from SCK[9]	SOUT and SCK drive strength			
					Very strong	25 pF	—	7.0	ns
					Strong	50 pF	—	8.0	
					Medium	50 pF	—	16.0	
SOUT data hold time (after SCK edge)								
10	t_{HO}	CC	D	SOUT data hold time after SCK[9]	SOUT and SCK drive strength			
					Very strong	25 pF	–7.7	—	ns
					Strong	50 pF	–11.0	—	
					Medium	50 pF	–15.0	—	

1. All timing values for output signals in this table are measured to 50% of the output voltage.
2. Timing is guaranteed to same drive capabilities for all signals, mixing of pad drives may reduce operating speeds and may cause incorrect operation.
3. N is the number of clock cycles added to time between PCS assertion and SCK assertion and is software programmable using DSPI_CTARx[PSSCK] and DSPI_CTARx[CSSCK]. The minimum value is 2 cycles unless TSB mode or Continuous SCK clock mode is selected, in which case, N is automatically set to 0 clock cycles (PCS and SCK are driven by the same edge of DSPI_CLKn).
4. t_{SYS} is the period of DSPI_CLKn clock, the input clock to the DSPI module. Maximum frequency is 100 MHz (min t_{SYS} = 10 ns).
5. M is the number of clock cycles added to time between SCK negation and PCS negation and is software programmable using DSPI_CTARx[PASC] and DSPI_CTARx[ASC]. The minimum value is 2 cycles unless TSB mode or Continuous SCK clock mode is selected, in which case, M is automatically set to 0 clock cycles (PCS and SCK are driven by the same edge of DSPI_CLKn).
6. t_{SDC} is only valid for even divide ratios. For odd divide ratios the fundamental duty cycle is not 50:50. For these odd divide ratios cases, the absolute spec number is applied as jitter/uncertainty to the nominal high time and low time.
7. PCSx and PCSS using same pad configuration.
8. Input timing assumes an input slew rate of 1 ns (10% – 90%) and uses TTL / Automotive voltage thresholds.
9. SOUT Data Valid and Data hold are independent of load capacitance if SCK and SOUT load capacitances are the same value.

Figure 25. DSPI CMOS master mode — classic timing, CPHA = 0

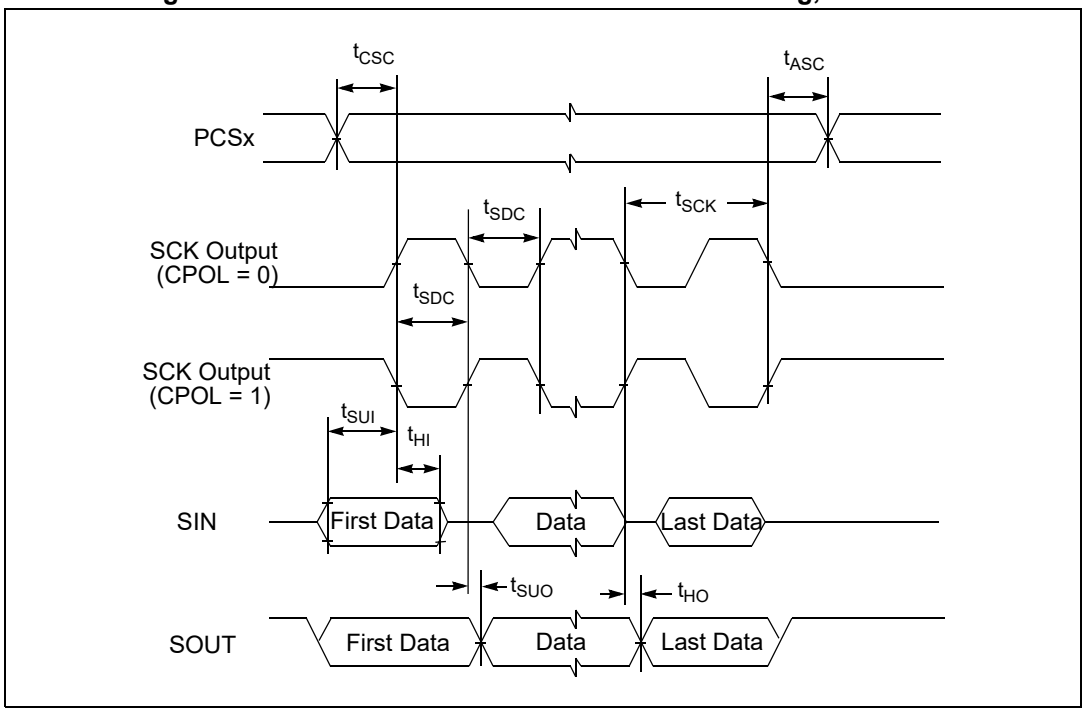


Figure 26. DSPI CMOS master mode — classic timing, CPHA = 1

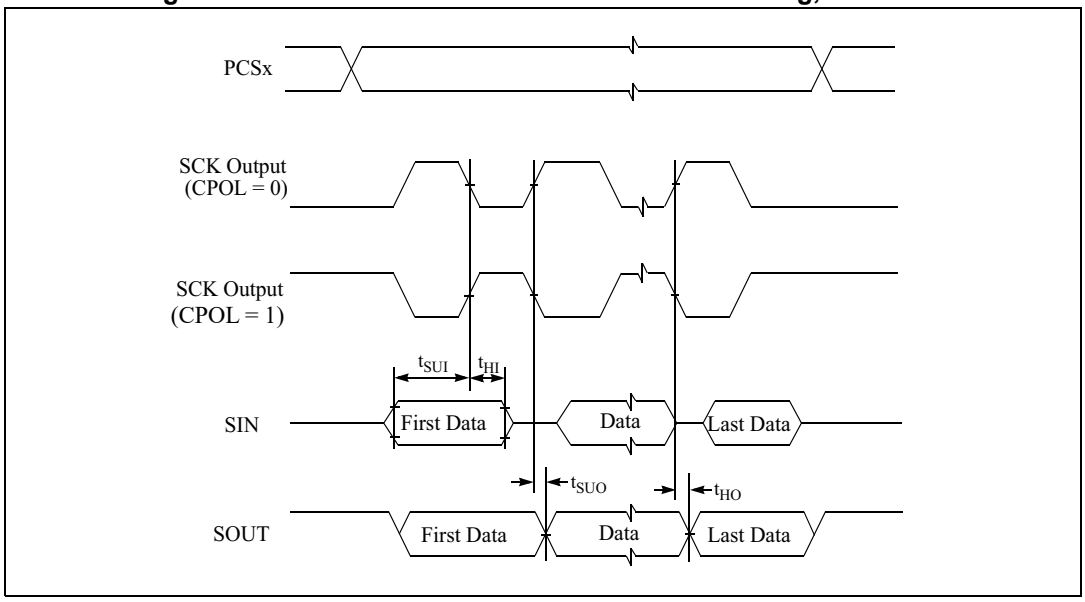
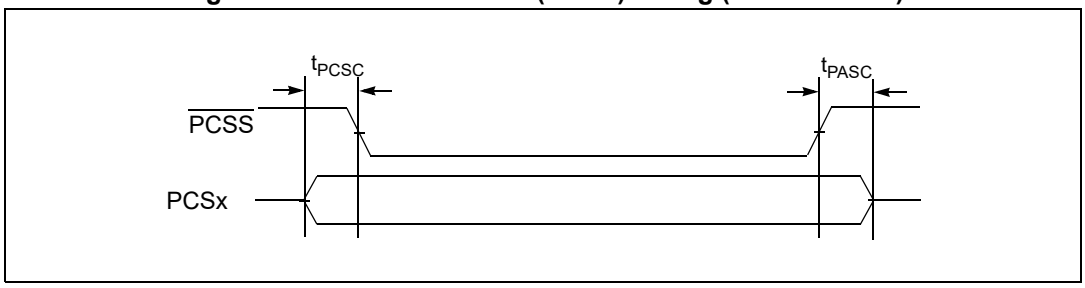


Figure 27. DSPI PCS strobe (PCSS) timing (master mode)



3.18.2.1.2 DSPI CMOS master mode — modified timing

Note: In the following table, all output timing is worst case and includes the mismatching of rise and fall times of the output pads.

Table 53. DSPI CMOS master modified timing (full duplex and output only) MTFE = 1, CPHA = 0 or 1

#	Symbol		C	Characteristic	Condition		Value(1)		Unit
					Pad drive(2)	Load (C_L)	Min	Max	
1	t_{SCK}	CC	D	SCK cycle time	SCK drive strength				
					Very strong	25 pF	33.0	—	ns
					Strong	50 pF	80.0	—	
					Medium	50 pF	200.0	—	
2	t_{CSC}	CC	D	PCS to SCK delay	SCK and PCS drive strength				
					Very strong	25 pF	$(N^{(3)} \times t_{SYS}^{(4)}) - 16$	—	ns
					Strong	50 pF	$(N^{(3)} \times t_{SYS}^{(4)}) - 16$	—	
					Medium	50 pF	$(N^{(3)} \times t_{SYS}^{(4)}) - 16$	—	
					PCS medium and SCK strong	PCS = 50 pF SCK = 50 pF	$(N^{(3)} \times t_{SYS}^{(4)}) - 29$	—	
3	t_{ASC}	CC	D	After SCK delay	SCK and PCS drive strength				
					Very strong	PCS = 0 pF SCK = 50 pF	$(M^{(5)} \times t_{SYS}^{(4)}) - 35$	—	ns
					Strong	PCS = 0 pF SCK = 50 pF	$(M^{(5)} \times t_{SYS}^{(4)}) - 35$	—	
					Medium	PCS = 0 pF SCK = 50 pF	$(M^{(5)} \times t_{SYS}^{(4)}) - 35$	—	
					PCS medium and SCK strong	PCS = 0 pF SCK = 50 pF	$(M^{(5)} \times t_{SYS}^{(4)}) - 35$	—	

Table 53. DSPI CMOS master modified timing (full duplex and output only) MTFE = 1, CPHA = 0 or 1 (continued)

#	Symbol		C	Characteristic	Condition		Value(1)		Unit
					Pad drive(2)	Load (C_L)	Min	Max	
4	t_{SDC}	CC	D	SCK duty cycle(6)	SCK drive strength				
					Very strong	0 pF	$^1/_2t_{SCK} - 2$	$^1/_2t_{SCK} + 2$	ns
					Strong	0 pF	$^1/_2t_{SCK} - 2$	$^1/_2t_{SCK} + 2$	
					Medium	0 pF	$^1/_2t_{SCK} - 5$	$^1/_2t_{SCK} + 5$	
PCS strobe timing									
5	t_{PCSC}	CC	D	PCSx to $\overline{PCSS}$ time(7)	PCS and PCSS drive strength				
					Strong	25 pF	16.0	—	ns
6	t_{PASC}	CC	D	$\overline{PCSS}$ to PCSx time(7)	PCS and PCSS drive strength				
					Strong	25 pF	16.0	—	ns
SIN setup time									
7	t_{SUI}	CC	D	SIN setup time to SCK CPHA = 0(8)	SCK drive strength				
					Very strong	25 pF	$25 - (P^{(9)} \times t_{SYS}^{(4)})$	—	ns
					Strong	50 pF	$31 - (P^{(9)} \times t_{SYS}^{(4)})$	—	
					Medium	50 pF	$52 - (P^{(9)} \times t_{SYS}^{(4)})$	—	
				SIN setup time to SCK CPHA = 1(8)	SCK drive strength				
					Very strong	25 pF	25.0	—	ns
					Strong	50 pF	31.0	—	
					Medium	50 pF	52.0	—	
SIN hold time									
8	t_{HI}	CC	D	SIN hold time from SCK CPHA = 0(8)	SCK drive strength				
					Very strong	0 pF	$-1 + (P^{(9)} \times t_{SYS}^{(3)})$	—	ns
					Strong	0 pF	$-1 + (P^{(9)} \times t_{SYS}^{(3)})$	—	
					Medium	0 pF	$-1 + (P^{(9)} \times t_{SYS}^{(3)})$	—	
				SIN hold time from SCK CPHA = 1(8)	SCK drive strength				
					Very strong	0 pF	–1.0	—	ns
					Strong	0 pF	–1.0	—	
					Medium	0 pF	–1.0	—	

Table 53. DSPI CMOS master modified timing (full duplex and output only) MTFE = 1, CPHA = 0 or 1 (continued)

#	Symbol	C	Characteristic	Condition		Value[1]		Unit
				Pad drive[2]	Load (C_L)	Min	Max	
SOUT data valid time (after SCK edge)								
9	t_{SUO}	CC	D	SOUT data valid time from SCK CPHA = 0, [10]	SOUT and SCK drive strength			
					Very strong	25 pF	—	7.0 + t_{SYS}[4]	ns
					Strong	50 pF	—	8.0 + t_{SYS}[4]	
					Medium	50 pF	—	16.0 + t_{SYS}[4]	
				SOUT data valid time from SCK CPHA = 1[10]	SOUT and SCK drive strength			
					Very strong	25 pF	—	7.0	ns
					Strong	50 pF	—	8.0	
					Medium	50 pF	—	16.0	
SOUT data hold time (after SCK edge)								
10	t_{HO}	CC	D	SOUT data hold time after SCK CPHA = 0[10]	SOUT and SCK drive strength			
					Very strong	25 pF	–7.7 + t_{SYS}[4]	—	ns
					Strong	50 pF	–11.0 + t_{SYS}[4]	—	
					Medium	50 pF	–15.0 + t_{SYS}[4]	—	
				SOUT data hold time after SCK CPHA = 1[10]	SOUT and SCK drive strength			
					Very strong	25 pF	–7.7	—	ns
					Strong	50 pF	–11.0	—	
					Medium	50 pF	–15.0	—	

1. All timing values for output signals in this table are measured to 50% of the output voltage.
2. Timing is guaranteed to same drive capabilities for all signals, mixing of pad drives may reduce operating speeds and may cause incorrect operation.
3. N is the number of clock cycles added to time between PCS assertion and SCK assertion and is software programmable using DSPI_CTARx[PSSCK] and DSPI_CTARx[CSSCK]. The minimum value is 2 cycles unless TSB mode or Continuous SCK clock mode is selected, in which case, N is automatically set to 0 clock cycles (PCS and SCK are driven by the same edge of DSPI_CLKn).
4. t_{SYS} is the period of DSPI_CLKn clock, the input clock to the DSPI module. Maximum frequency is 100 MHz (min t_{SYS} = 10 ns).
5. M is the number of clock cycles added to time between SCK negation and PCS negation and is software programmable using DSPI_CTARx[PASC] and DSPI_CTARx[ASC]. The minimum value is 2 cycles unless TSB mode or Continuous SCK clock mode is selected, in which case, M is automatically set to 0 clock cycles (PCS and SCK are driven by the same edge of DSPI_CLKn).
6. t_{SDC} is only valid for even divide ratios. For odd divide ratios the fundamental duty cycle is not 50:50. For these odd divide ratios cases, the absolute spec number is applied as jitter/uncertainty to the nominal high time and low time.
7. PCSx and PCSS using same pad configuration.
8. Input timing assumes an input slew rate of 1 ns (10% – 90%) and uses TTL / Automotive voltage thresholds.
9. P is the number of clock cycles added to delay the DSPI input sample point and is software programmable using DSPI_MCR[SMPL_PT]. The value must be 0, 1 or 2. If the baud rate divide ratio is /2 or /3, this value is automatically set to 1.

10. SOUT Data Valid and Data hold are independent of load capacitance if SCK and SOUT load capacitances are the same value.

Figure 28. DSPI CMOS master mode — modified timing, CPHA = 0

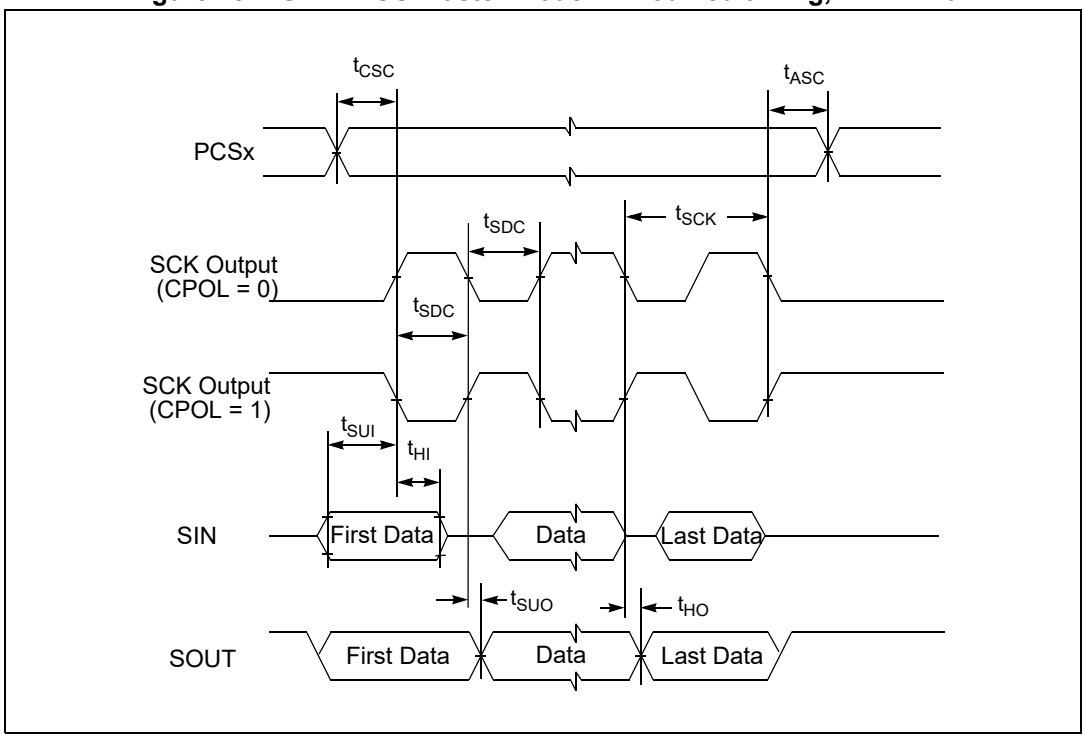


Figure 29. DSPI CMOS master mode — modified timing, CPHA = 1

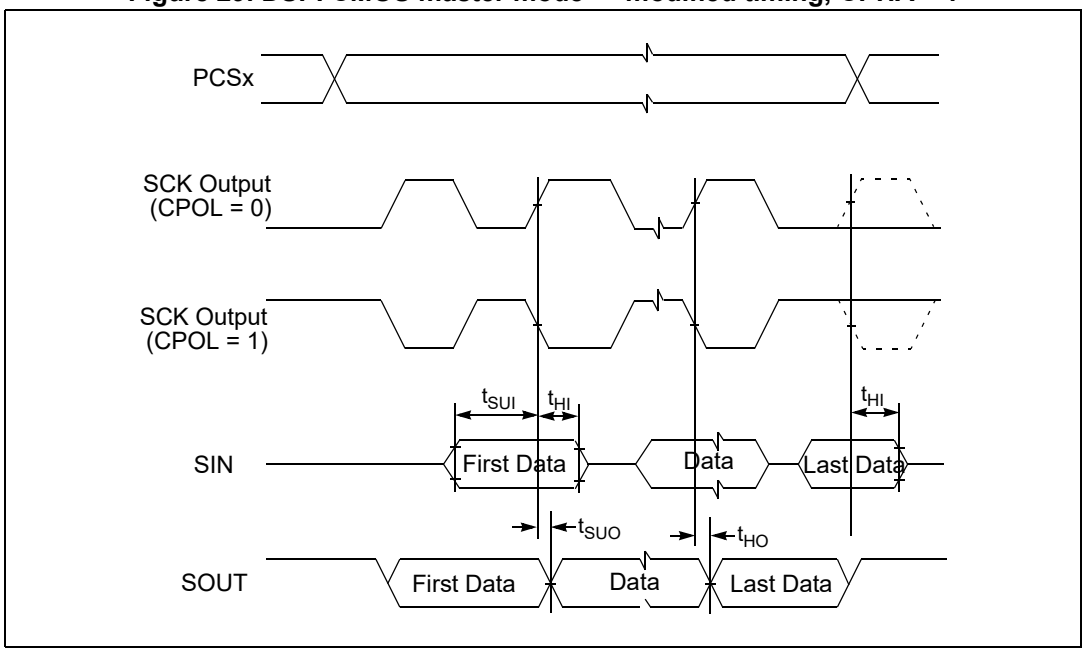
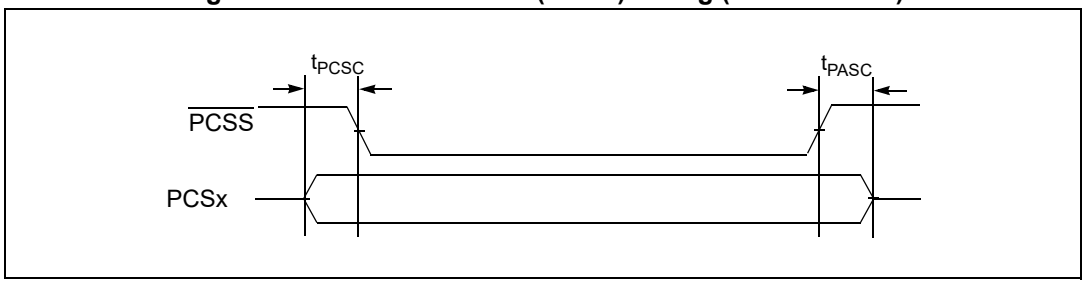


Figure 30. DSPI PCS strobe ($\overline{PCSS}$) timing (master mode)



3.18.2.1.3 DSPI LVDS master mode – modified timing

Table 54. DSPI LVDS master timing — full duplex — modified transfer format (MTFE = 1), CPHA = 0 or 1

#	Symbol		C	Characteristic	Condition		Value(1)		Unit
					Pad drive	Load	Min	Max	
1	t_{SCK}	CC	D	SCK cycle time	LVDS	15 pF to 25 pF differential(2)	30.0	—	ns
2	t_{CSC}	CC	D	PCS to SCK delay (LVDS SCK)	PCS drive strength				
					Very strong	25 pF	$(N^{(3)} \times t_{SYS}^{(4)}) - 10$	—	ns
					Strong	50 pF	$(N^{(3)} \times t_{SYS}^{(4)}) - 10$	—	ns
					Medium	50 pF	$(N^{(3)} \times t_{SYS}^{(4)}) - 32$	—	ns
3	t_{ASC}	CC	D	After SCK delay (LVDS SCK)	Very strong	PCS = 0 pF SCK = 25 pF	$(M^{(5)} \times t_{SYS}^{(4)}) - 8$	—	ns
					Strong	PCS = 0 pF SCK = 25 pF	$(M^{(5)} \times t_{SYS}^{(4)}) - 8$	—	ns
					Medium	PCS = 0 pF SCK = 25 pF	$(M^{(5)} \times t_{SYS}^{(4)}) - 8$	—	ns
4	t_{SDC}	CC	D	SCK duty cycle(6)	LVDS	15 pF to 25 pF differential	$^1/_2t_{SCK} - 2$	$^1/_2t_{SCK} + 2$	ns
7	t_{SUI}	CC	D	SIN setup time					
				SIN setup time to SCK CPHA = 0(7)	SCK drive strength				
					LVDS	15 pF to 25 pF differential	$23 - (P^{(8)} \times t_{SYS}^{(4)})$	—	ns
				SIN setup time to SCK CPHA = 1(7)	SCK drive strength				
					LVDS	15 pF to 25 pF differential	23	—	ns

Table 54. DSPI LVDS master timing — full duplex — modified transfer format (MTFE = 1), CPHA = 0 or 1 (continued)

#	Symbol		C	Characteristic	Condition		Value[1]		Unit
					Pad drive	Load	Min	Max	
8	t_{HI}	CC	D	SIN Hold Time					
				SIN hold time from SCK CPHA = 0[7]	SCK drive strength				
					LVDS	0 pF differential	– 1 + ($P^{(8)}$ × $t_{SYS}^{(4)}$)	—	ns
				SIN hold time from SCK CPHA = 1[7]	SCK drive strength				
					LVDS	0 pF differential	–1	—	ns
9	t_{SUO}	CC	D	SOUT data valid time (after SCK edge)					
				SOUT data valid time from SCK CPHA = 0[9]	SOUT and SCK drive strength				
					LVDS	15 pF to 25 pF differential	—	7.0 + $t_{SYS}^{(4)}$	ns
				SOUT data valid time from SCK CPHA = 1[9]	SOUT and SCK drive strength				
					LVDS	15 pF to 25 pF differential	—	7.0	ns
10	t_{HO}	CC	D	SOUT data hold time (after SCK edge)					
				SOUT data hold time after SCK CPHA = 0[9]	SOUT and SCK drive strength				
					LVDS	15 pF to 25 pF differential	–7.5 + $t_{SYS}^{(4)}$	—	ns
				SOUT data hold time after SCK CPHA = 1[9]	SOUT and SCK drive strength				
					LVDS	15 pF to 25 pF differential	–7.5	—	ns

1. All timing values for output signals in this table are measured to 50% of the output voltage.
2. LVDS differential load considered is the capacitance on each terminal of the differential pair, as shown in *Figure 12*.
3. N is the number of clock cycles added to time between PCS assertion and SCK assertion and is software programmable using DSPI_CTARx[PSSCK] and DSPI_CTARx[CSSCK]. The minimum value is 2 cycles unless TSB mode or Continuous SCK clock mode is selected, in which case, N is automatically set to 0 clock cycles (PCS and SCK are driven by the same edge of DSPI_CLKn).
4. t_{SYS} is the period of DSPI_CLKn clock, the input clock to the DSPI module. Maximum frequency is 100 MHz (min t_{SYS} = 10 ns).
5. M is the number of clock cycles added to time between SCK negation and PCS negation and is software programmable using DSPI_CTARx[PASC] and DSPI_CTARx[ASC]. The minimum value is 2 cycles unless TSB mode or Continuous SCK clock mode is selected, in which case, M is automatically set to 0 clock cycles (PCS and SCK are driven by the same edge of DSPI_CLKn).
6. t_{SDC} is only valid for even divide ratios. For odd divide ratios the fundamental duty cycle is not 50:50. For these odd divide ratios cases, the absolute spec number is applied as jitter/uncertainty to the nominal high time and low time.
7. Input timing assumes an input slew rate of 1 ns (10% – 90%) and LVDS differential voltage = ±100 mV.
8. P is the number of clock cycles added to delay the DSPI input sample point and is software programmable using DSPI_MCR[SMPL_PT]. The value must be 0, 1 or 2. If the baud rate divide ratio is /2 or /3, this value is automatically set to 1.

9. SOUT Data Valid and Data hold are independent of load capacitance if SCK and SOUT load capacitances are the same value.

Figure 31. DSPI LVDS master mode — modified timing, CPHA = 0

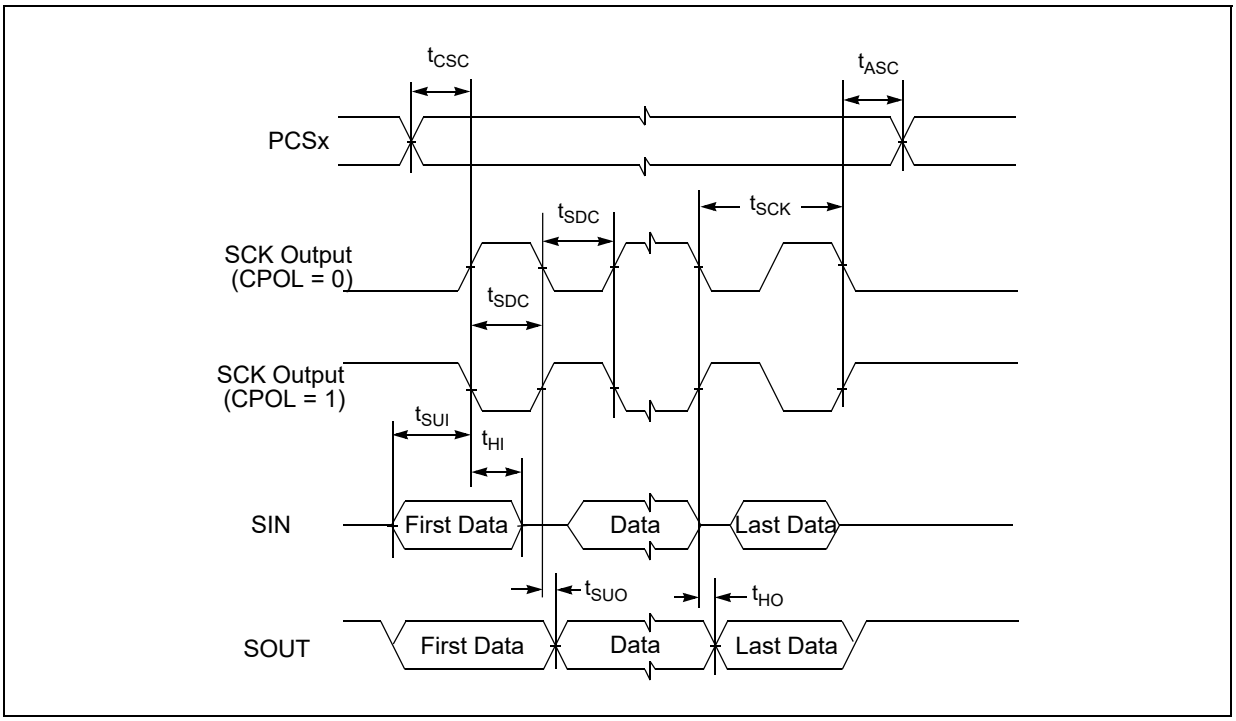
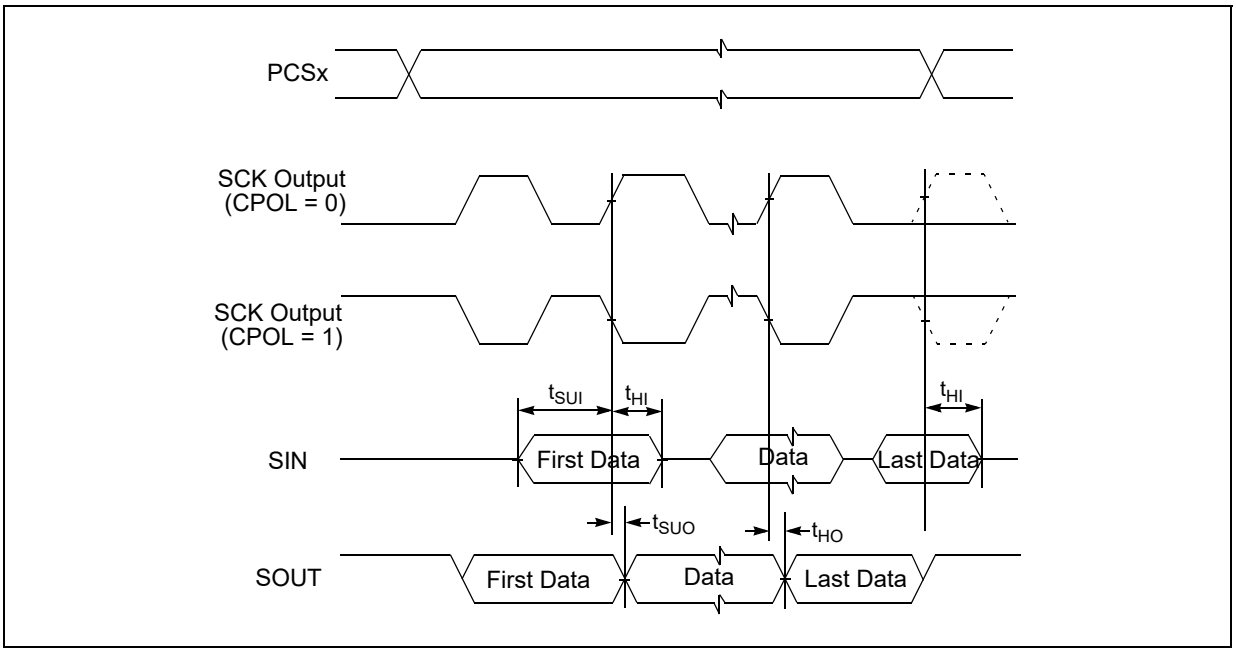


Figure 32. DSPI LVDS master mode — modified timing, CPHA = 1



3.18.2.1.4 DSPI master mode – output only

Note: In the following table:

- *All DSPI timing specifications apply to pins when using LVDS pads for SCK and SOUT and CMOS pad for PCS with pad driver strength as defined. Timing may degrade for weaker output drivers.*
- *TSB = 1 or ITSB = 1 automatically selects MTFE = 1 and CPHA = 1.*

Table 55. DSPI LVDS master timing – output only – timed serial bus mode TSB = 1 or ITSB = 1, CPOL = 0 or 1, continuous SCK clock

#	Symbol		C	Characteristic	Condition		Value		Unit
					Pad drive	Load	Min	Max	
1	t_{SCK}	CC	D	SCK cycle time	LVDS	15 pF to 50 pF differential(1)	25.0	—	ns
2	t_{CSV}	CC	D	PCS valid after SCK(2) (SCK with 50 pF differential load cap.)	Very strong	25 pF	—	6.0	ns
					Strong	50 pF	—	10.5	ns
3	t_{CSH}	CC	D	PCS hold after SCK(2) (SCK with 50 pF differential load cap.)	Very strong	0 pF	–4.0	—	ns
					Strong	0 pF	–4.0	—	ns
4	t_{SDC}	CC	D	SCK duty cycle (SCK with 50 pF differential load cap.)	LVDS	15 pF to 50 pF differential	$^1/_2t_{SCK} - 2$	$^1/_2t_{SCK} + 2$	ns
SOUT data valid time (after SCK edge)									
5	t_{SUO}	CC	D	SOUT data valid time from SCK(3)	SOUT and SCK drive strength				
					LVDS	15 pF to 50 pF differential	—	3.5	ns
SOUT data hold time (after SCK edge)									
6	t_{HO}	CC	D	SOUT data hold time after SCK(3)	SOUT and SCK drive strength				
					LVDS	15 pF to 50 pF differential	–3.5	—	ns

1. LVDS differential load considered is the capacitance on each terminal of the differential pair, as shown in *Figure 12*.
2. With TSB mode or Continuous SCK clock mode selected, PCS and SCK are driven by the same edge of DSPI_CLKn. This timing value is due to pad delays and signal propagation delays.
3. SOUT Data Valid and Data hold are independent of load capacitance if SCK and SOUT load capacitances are the same value.

Note: In the following table:

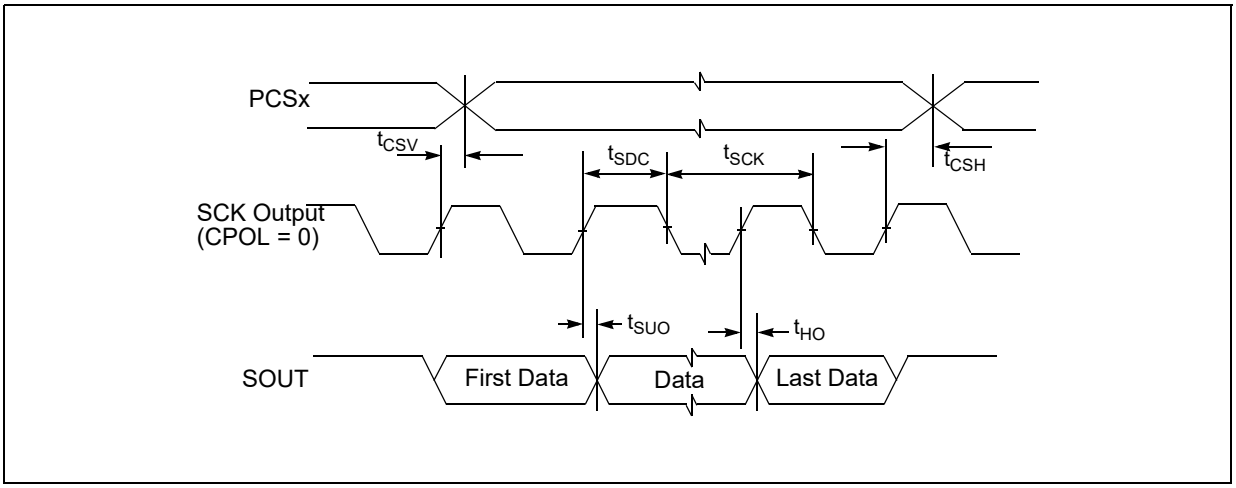
- *All output timing is worst case and includes the mismatching of rise and fall times of the output pads.*
- *TSB = 1 or ITSB = 1 automatically selects MTFE = 1 and CPHA = 1.*

Table 56. DSPI CMOS master timing – output only – timed serial bus mode TSB = 1 or ITSB = 1, CPOL = 0 or 1, continuous SCK clock

#	Symbol		C	Characteristic	Condition		Value(1)		Unit
					Pad drive(2)	Load (C_L)	Min	Max	
1	t_{SCK}	CC	D	SCK cycle time	SCK drive strength				
					Very strong	25 pF	33.0	—	ns
					Strong	50 pF	80.0	—	ns
					Medium	50 pF	200.0	—	ns
2	t_{CSV}	CC	D	PCS valid after SCK(3)	SCK and PCS drive strength				
					Very strong	25 pF	7	—	ns
					Strong	50 pF	8	—	ns
					Medium	50 pF	16	—	ns
					PCS medium and SCK strong	PCS = 50 pF SCK = 50 pF	29	—	ns
3	t_{CSH}	CC	D	PCS hold after SCK(3)	SCK and PCS drive strength				
					Very strong	PCS = 0 pF SCK = 50 pF	–14	—	ns
					Strong	PCS = 0 pF SCK = 50 pF	–14	—	ns
					Medium	PCS = 0 pF SCK = 50 pF	–33	—	ns
					PCS medium and SCK strong	PCS = 0 pF SCK = 50 pF	–35	—	ns
4	t_{SDC}	CC	D	SCK duty cycle(4)	SCK drive strength				
					Very strong	0 pF	$^1/_2t_{SCK} - 2$	$^1/_2t_{SCK} + 2$	ns
					Strong	0 pF	$^1/_2t_{SCK} - 2$	$^1/_2t_{SCK} + 2$	ns
					Medium	0 pF	$^1/_2t_{SCK} - 5$	$^1/_2t_{SCK} + 5$	ns
SOUT data valid time (after SCK edge)									
9	t_{SUO}	CC	D	SOUT data valid time from SCK CPHA = 1(5)	SOUT and SCK drive strength				
					Very strong	25 pF	—	7.0	ns
					Strong	50 pF	—	8.0	ns
					Medium	50 pF	—	16.0	ns
SOUT data hold time (after SCK edge)									
10	t_{HO}	CC	D	SOUT data hold time after SCK CPHA = 1(5)	SOUT and SCK drive strength				
					Very strong	25 pF	–7.7	—	ns
					Strong	50 pF	–11.0	—	ns
					Medium	50 pF	–15.0	—	ns

1. All timing values for output signals in this table are measured to 50% of the output voltage.
2. Timing is guaranteed to same drive capabilities for all signals, mixing of pad drives may reduce operating speeds and may cause incorrect operation.
3. With TSB mode or Continuous SCK clock mode selected, PCS and SCK are driven by the same edge of DSPI_CLKn. This timing value is due to pad delays and signal propagation delays.
4. t_{SDC} is only valid for even divide ratios. For odd divide ratios the fundamental duty cycle is not 50:50. For these odd divide ratios cases, the absolute spec number is applied as jitter/uncertainty to the nominal high time and low time.
5. SOUT Data Valid and Data hold are independent of load capacitance if SCK and SOUT load capacitances are the same value.

Figure 33. DSPI LVDS and CMOS master timing–output only— MTFE = 1, CHPA = 1



3.18.2.2 Slave mode timing

Table 57. DSPI CMOS slave timing — full duplex — normal and modified transfer formats (MTFE = 0/1)

#	Symbol		C	Characteristic	Condition		Min	Max	Unit
					Pad Drive	Load			
1	t_{SCK}	CC	D	SCK Cycle Time(1)	—	—	62	—	ns
2	t_{CSC}	SR	D	$\overline{SS}$ to SCK Delay(1)	—	—	16	—	ns
3	t_{ASC}	SR	D	SCK to $\overline{SS}$ Delay(1)	—	—	16	—	ns
4	t_{SDC}	CC	D	SCK Duty Cycle(1)	—	—	30	—	ns
5	t_A	CC	D	Slave Access Time(1) (2) (3) ($\overline{SS}$ active to SOUT driven)	Very strong	25 pF	—	50	ns
					Strong	50 pF	—	50	ns
					Medium	50 pF	—	60	ns
6	t_{DIS}	CC	D	Slave SOUT Disable Time(1) (2) (3) ($\overline{SS}$ inactive to SOUT High-Z or invalid)	Very strong	25 pF	—	5	ns
					Strong	50 pF	—	5	ns
					Medium	50 pF	—	10	ns

Table 57. DSPI CMOS slave timing — full duplex — normal and modified transfer formats (MTFE = 0/1) (continued)

#	Symbol		C	Characteristic	Condition		Min	Max	Unit
					Pad Drive	Load			
9	t_{SUI}	CC	D	Data Setup Time for Inputs(1)	—	—	10	—	ns
10	t_{HI}	CC	D	Data Hold Time for Inputs(1)	—	—	10	—	ns
11	t_{SUO}	CC	D	SOUT Valid Time(1) (2) (3) (after SCK edge)	Very strong	25 pF	—	30	ns
					Strong	50 pF	—	30	ns
					Medium	50 pF	—	50	ns
12	t_{HO}	CC	D	SOUT Hold Time(1) (2) (3) (after SCK edge)	Very strong	25 pF	2.5	—	ns
					Strong	50 pF	2.5	—	ns
					Medium	50 pF	2.5	—	ns

1. Input timing assumes an input slew rate of 1 ns (10% - 90%) and uses TTL / Automotive voltage thresholds.
2. All timing values for output signals in this table, are measured to 50% of the output voltage.
3. All output timing is worst case and includes the mismatching of rise and fall times of the output pads.

Figure 34. DSPI slave mode — modified transfer format timing (MFTE = 0/1) CPHA = 0

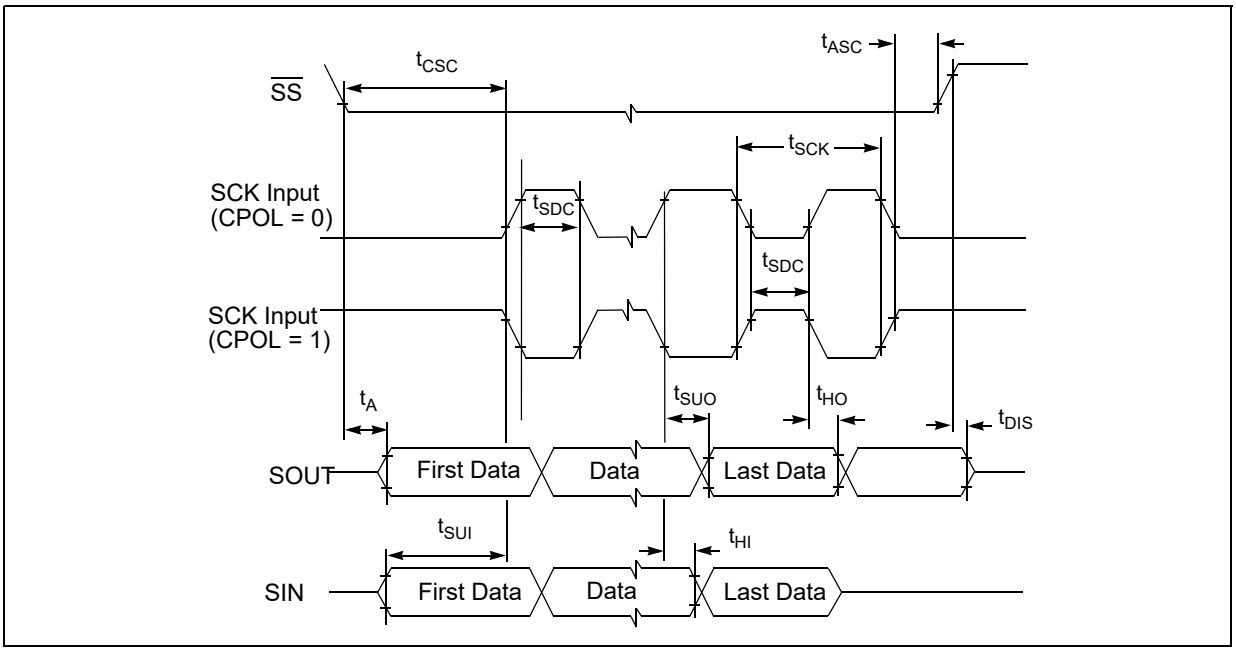
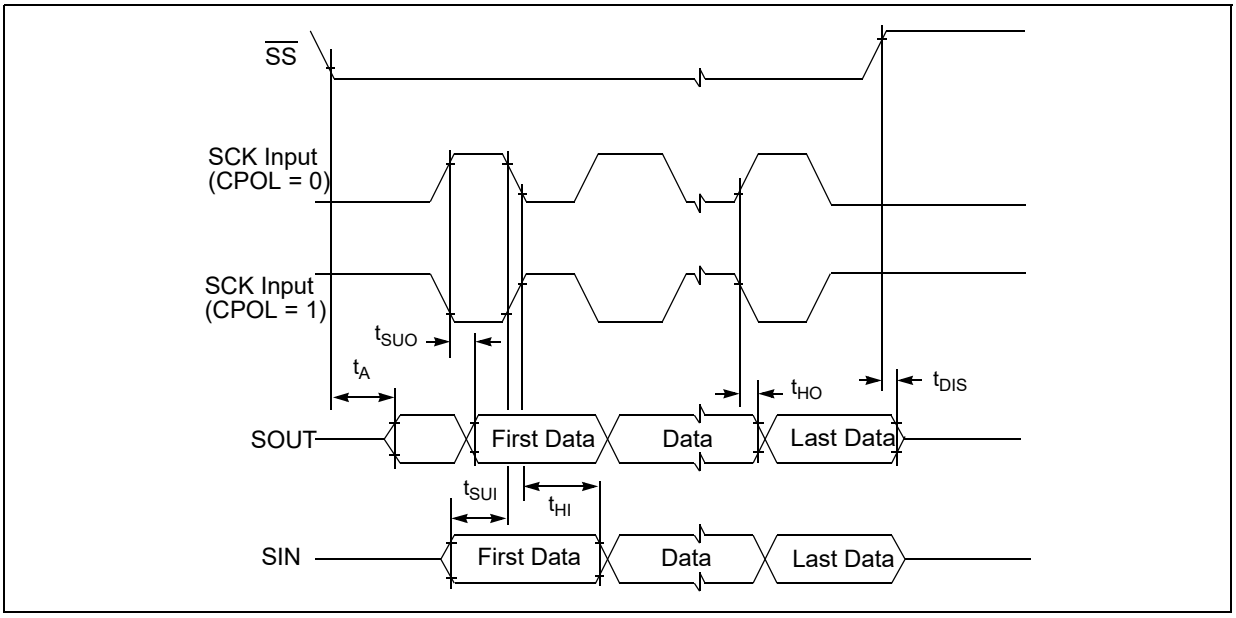


Figure 35. DSPI slave mode — modified transfer format timing (MFTE = 0/1) CPHA = 1



3.18.3 Ethernet timing

The Ethernet provides both MII and RMII interfaces. The MII and RMII signals can be configured for either CMOS or TTL signal levels compatible with devices operating at either 5.0 V or 3.3 V. Please check the device pinout details to review the packages supporting MII and RMII.

3.18.3.1 MII receive signal timing (RXD[3:0], RX_DV, RX_ER, and RX_CLK)

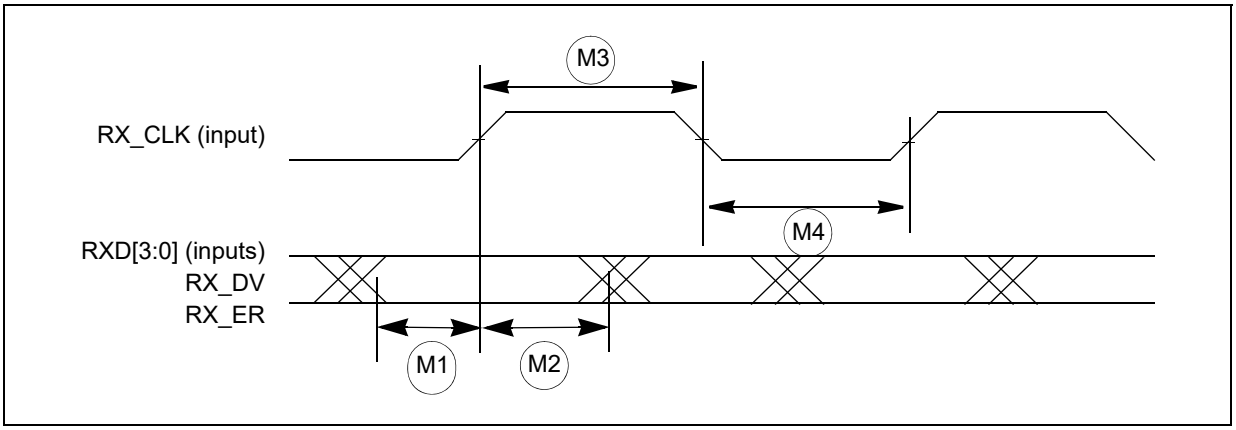
The receiver functions correctly up to a RX_CLK maximum frequency of 25 MHz +1%. There is no minimum frequency requirement. The system clock frequency must be at least equal to or greater than the RX_CLK frequency.

Note: In the following table, all timing specifications are referenced from RX_CLK = 1.4 V to the valid input levels, 0.8 V and 2.0 V.

Table 58. MII receive signal timing

Symbol		C	Characteristic	Value		Unit
				Min	Max	
M1	CC	D	RXD[3:0], RX_DV, RX_ER to RX_CLK setup	5	—	ns
M2	CC	D	RX_CLK to RXD[3:0], RX_DV, RX_ER hold	5	—	ns
M3	CC	D	RX_CLK pulse width high	35%	65%	RX_CLK period
M4	CC	D	RX_CLK pulse width low	35%	65%	RX_CLK period

Figure 36. MII receive signal timing diagram



3.18.3.2 MII transmit signal timing (TXD[3:0], TX_EN, TX_ER, TX_CLK)

The transmitter functions correctly up to a TX_CLK maximum frequency of 25 MHz +1%. There is no minimum frequency requirement. The system clock frequency must be at least equal to or greater than the TX_CLK frequency.

The transmit outputs (TXD[3:0], TX_EN, TX_ER) can be programmed to transition from either the rising or falling edge of TX_CLK, and the timing is the same in either case. This option allows the use of non-compliant MII PHYs.

Refer to the SPC58xNx 32-bit Power Architecture microcontroller *reference manual's* Ethernet chapter for details of this option and how to enable it.

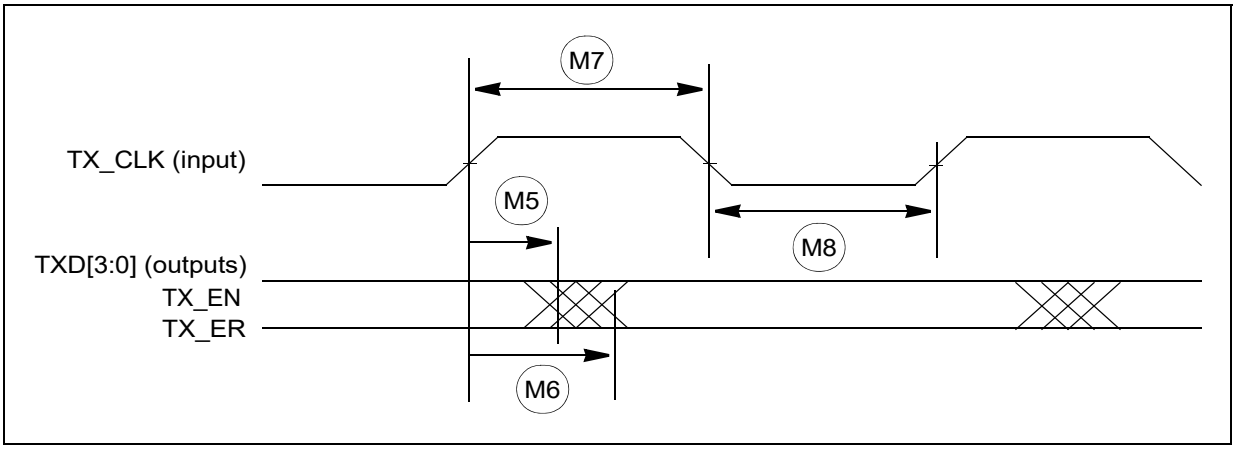
Note: In the following table, all timing specifications are referenced from TX_CLK = 1.4 V to the valid output levels, 0.8 V and 2.0 V.

Table 59. MII transmit signal timing

Symbol		C	Characteristic	Value(1)		Unit
				Min	Max	
M5	CC	D	TX_CLK to TXD[3:0], TX_EN, TX_ER invalid	5	—	ns
M6	CC	D	TX_CLK to TXD[3:0], TX_EN, TX_ER valid	—	25	ns
M7	CC	D	TX_CLK pulse width high	35%	65%	TX_CLK period
M8	CC	D	TX_CLK pulse width low	35%	65%	TX_CLK period

1. Output parameters are valid for C_L = 25 pF, where C_L is the external load to the device. The internal package capacitance is accounted for, and does not need to be subtracted from the 25 pF value

Figure 37. MII transmit signal timing diagram



3.18.3.3 MII async inputs signal timing (CRS and COL)

Table 60. MII async inputs signal timing

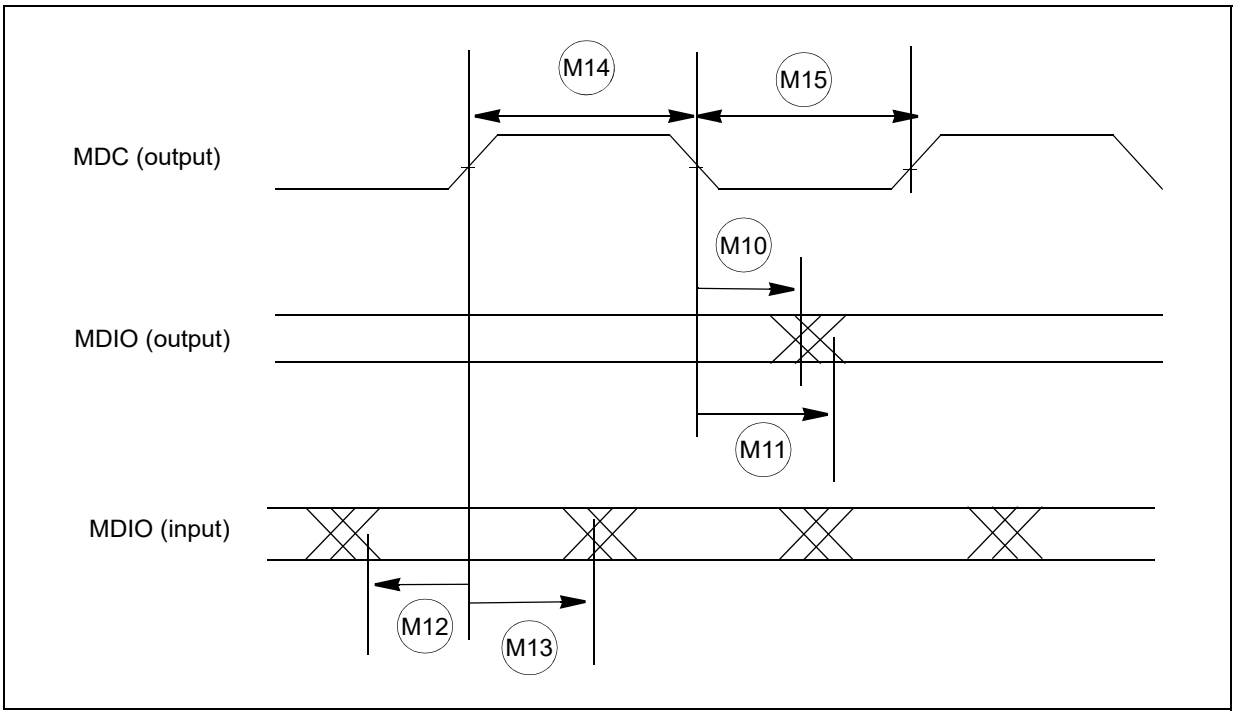
Symbol		C	Characteristic	Value		Unit
				Min	Max	
M9	CC	D	CRS, COL minimum pulse width	1.5	—	TX_CLK period

Figure 38. MII async inputs timing diagram

3.18.3.4 MII and RMII serial management channel timing (MDIO and MDC)

The Ethernet functions correctly with a maximum MDC frequency of 2.5 MHz.

Figure 39. MII serial management channel timing diagram



3.18.3.5 MII and RMII serial management channel timing (MDIO and MDC)

The Ethernet functions correctly with a maximum MDC frequency of 2.5 MHz.

Note: In the following table, all timing specifications are referenced from MDC = 1.4 V (TTL levels) to the valid input and output levels, 0.8 V and 2.0 V (TTL levels). For 5 V operation, timing is referenced from MDC = 50% to 2.2 V/3.5 V input and output levels.

Table 61. MII serial management channel timing

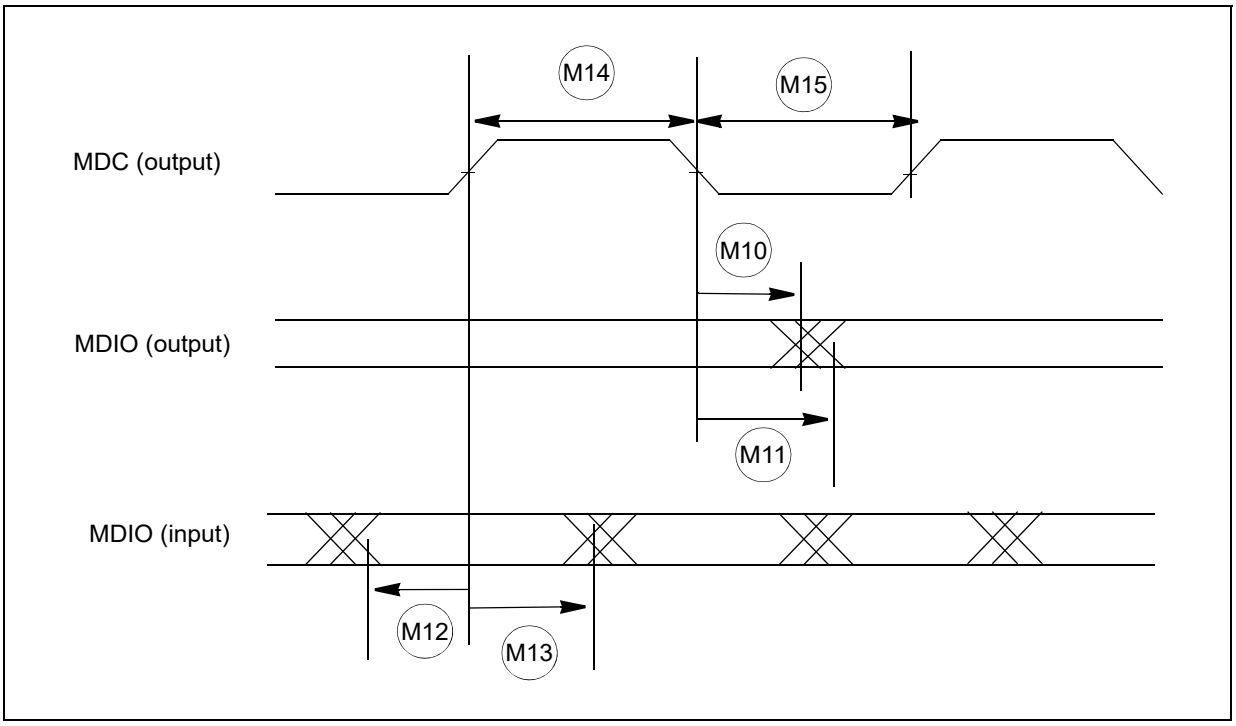
Symbol		C	Characteristic	Value		Unit
				Min	Max	
M10	CC	D	MDC falling edge to MDIO output invalid (minimum propagation delay)	0	—	ns
M11	CC	D	MDC falling edge to MDIO output valid (max prop delay)	—	25	ns
M12	CC	D	MDIO (input) to MDC rising edge setup	10	—	ns
M13	CC	D	MDIO (input) to MDC rising edge hold	0	—	ns
M14	CC	D	MDC pulse width high	40%	60%	MDC period
M15	CC	D	MDC pulse width low	40%	60%	MDC period

Note: In the following table, all timing specifications are referenced from MDC = 1.4 V (TTL levels) to the valid input and output levels, 0.8 V and 2.0 V (TTL levels). For 5 V operation, timing is referenced from MDC = 50% to 2.2 V/3.5 V input and output levels.

Table 62. RMII serial management channel timing

Symbol		C	Characteristic	Value		Unit
				Min	Max	
M10	CC	D	MDC falling edge to MDIO output invalid (minimum propagation delay)	0	—	ns
M11	CC	D	MDC falling edge to MDIO output valid (max prop delay)	—	25	ns
M12	CC	D	MDIO (input) to MDC rising edge setup	10	—	ns
M13	CC	D	MDIO (input) to MDC rising edge hold	0	—	ns
M14	CC	D	MDC pulse width high	40%	60%	MDC period
M15	CC	D	MDC pulse width low	40%	60%	MDC period

Figure 40. MII serial management channel timing diagram



3.18.3.6 RMII receive signal timing (RXD[1:0], CRS_DV)

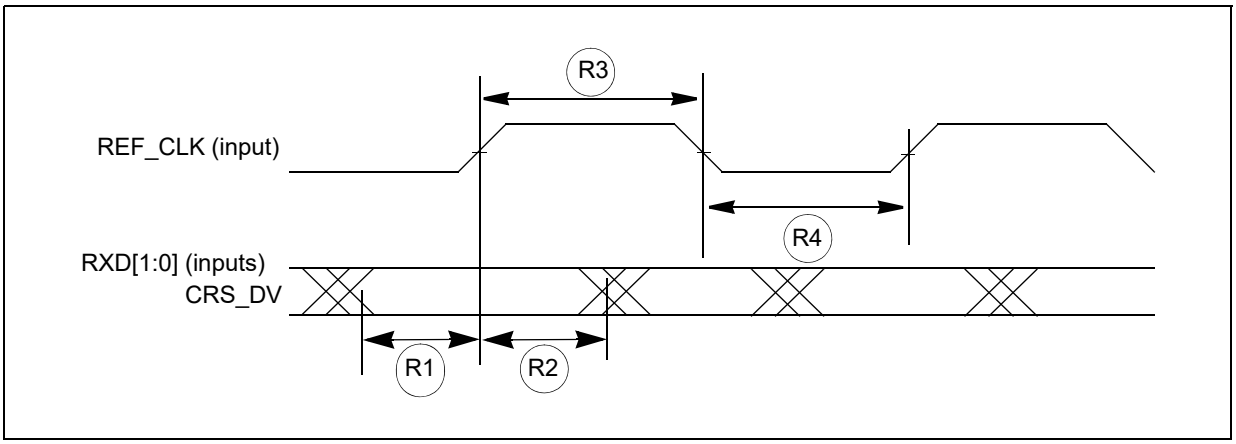
The receiver functions correctly up to a REF_CLK maximum frequency of 50 MHz +1%. There is no minimum frequency requirement. The system clock frequency must be at least equal to or greater than the RX_CLK frequency, which is half that of the REF_CLK frequency.

Note: In the following table, all timing specifications are referenced from REF_CLK = 1.4 V to the valid input levels, 0.8 V and 2.0 V.

Table 63. RMII receive signal timing

Symbol		C	Characteristic	Value		Unit
				Min	Max	
R1	CC	D	RXD[1:0], CRS_DV to REF_CLK setup	4	—	ns
R2	CC	D	REF_CLK to RXD[1:0], CRS_DV hold	2	—	ns
R3	CC	D	REF_CLK pulse width high	35%	65%	REF_CLK period
R4	CC	D	REF_CLK pulse width low	35%	65%	REF_CLK period

Figure 41. RMII receive signal timing diagram



3.18.3.7 RMII transmit signal timing (TXD[1:0], TX_EN)

The transmitter functions correctly up to a REF_CLK maximum frequency of 50 MHz + 1%. There is no minimum frequency requirement. The system clock frequency must be at least equal to or greater than the TX_CLK frequency, which is half that of the REF_CLK frequency.

The transmit outputs (TXD[1:0], TX_EN) can be programmed to transition from either the rising or falling edge of REF_CLK, and the timing is the same in either case. This option allows the use of non-compliant RMII PHYs.

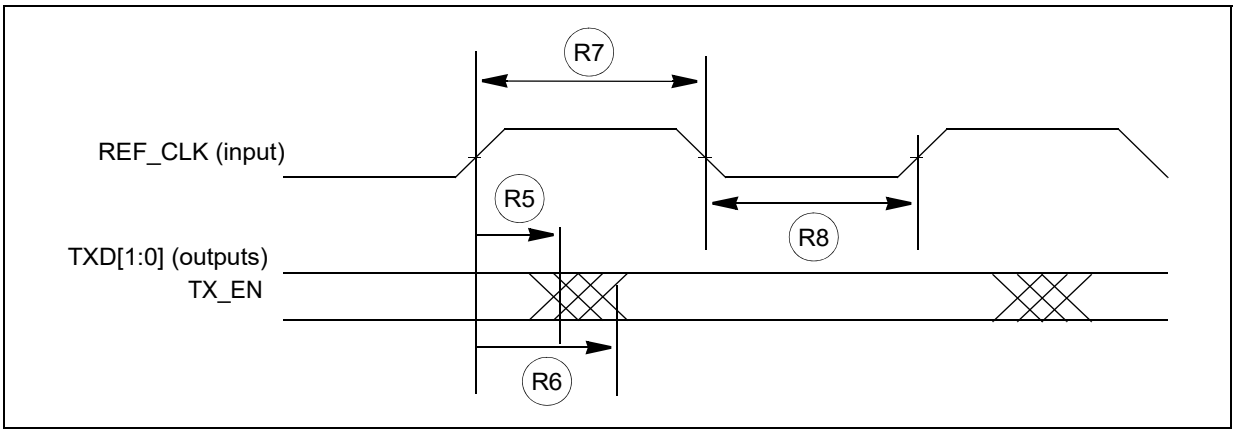
Note: In the following table, all timing specifications are referenced from REF_CLK = 1.4 V to the valid output levels, 0.8 V and 2.0 V.

RMII transmit signal valid timing specified is considering the rise/fall time of the ref_clk on the pad as 1ns.

Table 64. RMII transmit signal timing

Symbol		C	Characteristic	Value		Unit
				Min	Max	
R5	CC	D	REF_CLK to TXD[1:0], TX_EN invalid	2	—	ns
R6	CC	D	REF_CLK to TXD[1:0], TX_EN valid	—	14	ns
R7	CC	D	REF_CLK pulse width high	35%	65%	REF_CLK period
R8	CC	D	REF_CLK pulse width low	35%	65%	REF_CLK period

Figure 42. RMII transmit signal timing diagram



3.18.4 FlexRay timing

This section provides the FlexRay Interface timing characteristics for the input and output signals.

These are recommended numbers as per the FlexRay EPL v3.0 specification, and subject to change per the final timing analysis of the device.

3.18.4.1 TxEN

Figure 43. TxEN signal

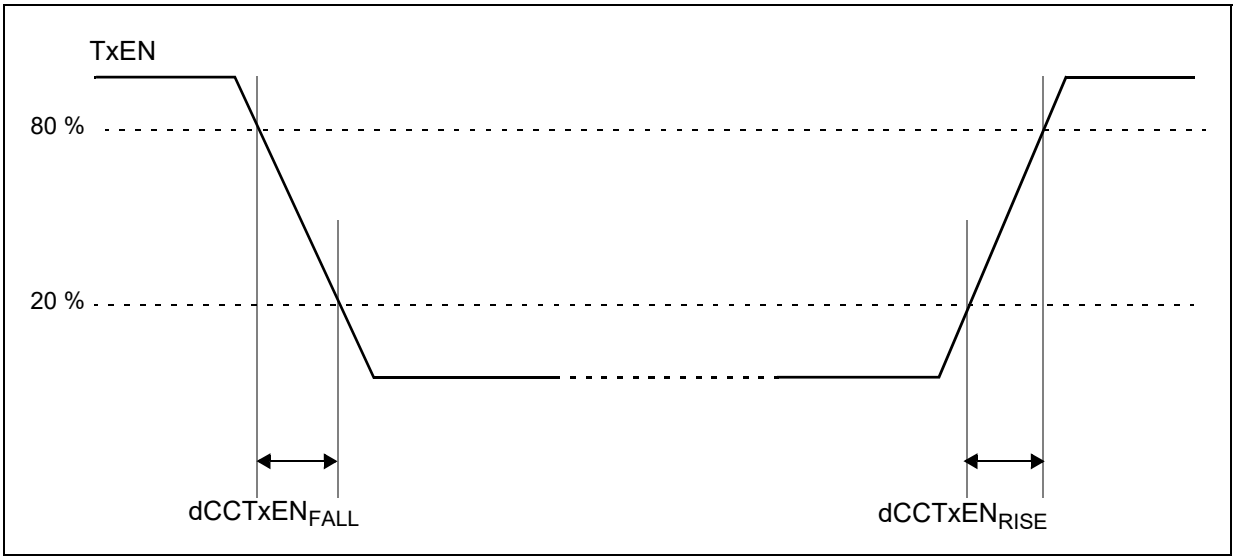
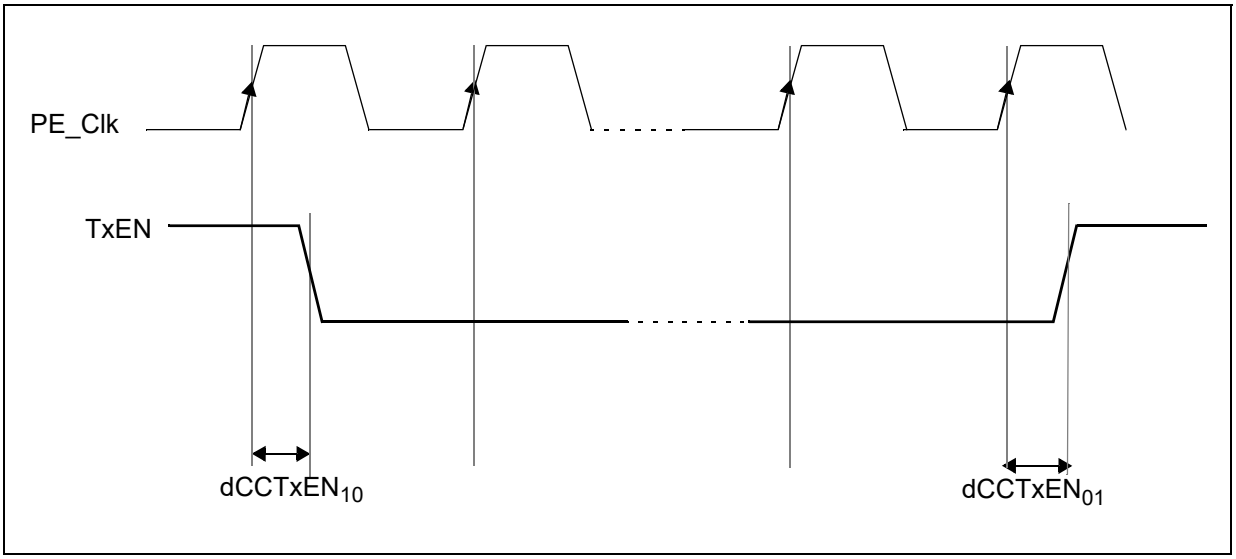


Table 65. TxEN output characteristics

Symbol		C	Characteristic[1] [2]	Value		Unit
				Min	Max	
dCCTxEN$_{RISE25}$	CC	D	Rise time of TxEN signal at CC	—	9	ns
dCCTxEN$_{FALL25}$	CC	D	Fall time of TxEN signal at CC	—	9	ns
dCCTxEN$_{01}$	CC	D	Sum of delay between Clk to Q of the last FF and the final output buffer, rising edge	—	25	ns
dCCTxEN$_{10}$	CC	D	Sum of delay between Clk to Q of the last FF and the final output buffer, falling edge	—	25	ns

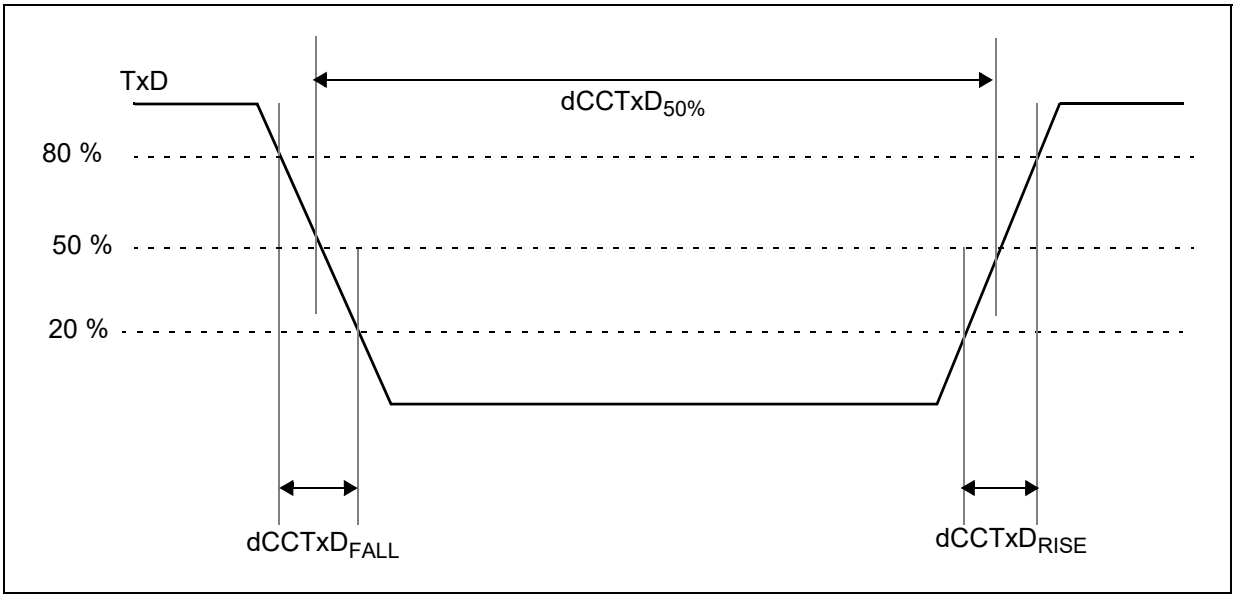
1. TxEN pin load maximum 25 pF.
2. Pad configured as VERY STRONG.

Figure 44. TxEN signal propagation delays



3.18.4.2 TxD

Figure 45. TxD signal



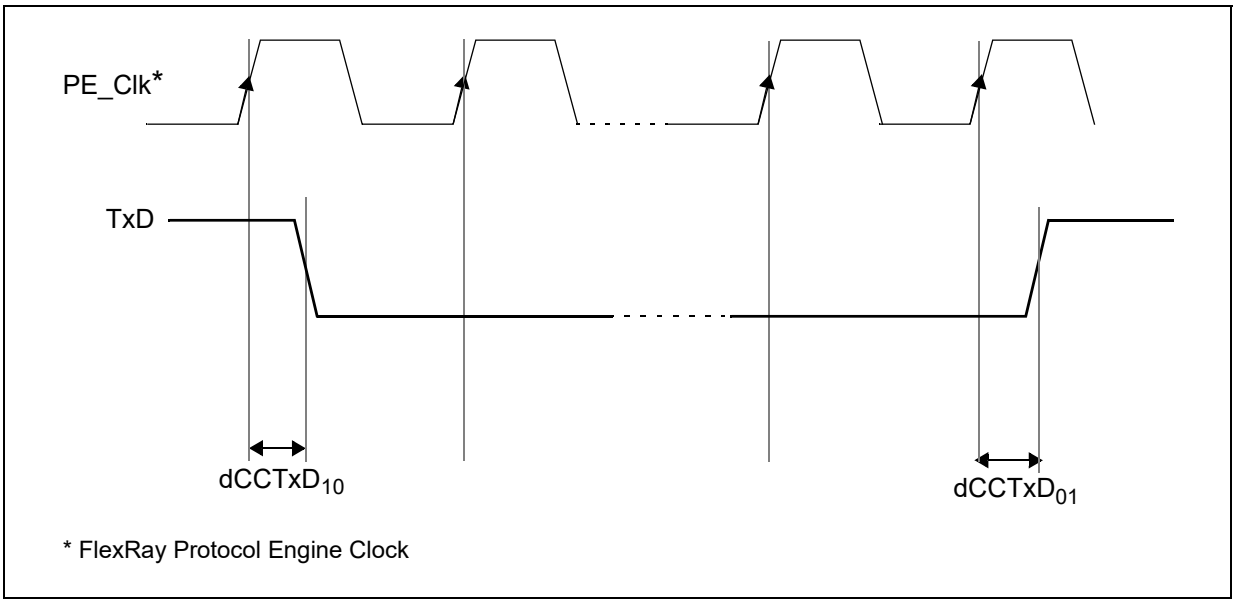
Note: In the following table, specifications valid according to FlexRay EPL 3.0.1 standard with 20%–80% levels and a 10 pF load at the end of a 50 Ohm, 1 ns stripline. Please refer to the Very Strong I/O pad specifications.

Table 66. TxD output characteristics

Symbol		C	Characteristic[1],[2]	Value		Unit
				Min	Max	
dCCTxAsym	CC	D	Asymmetry of sending CC at 25 pF load (= $dCCTxD_{50\%}$ − 100 ns)	–2.45	2.45	ns
$dCCTxD_{RISE25}$+$dCCTxD_{FALL25}$	CC	D	Sum of Rise and Fall time of TxD signal at the output pin[3]	—	9[4]	ns
		D		—	9[5]	
$dCCTxD_{01}$	CC	D	Sum of delay between Clk to Q of the last FF and the final output buffer, rising edge	—	25	ns
$dCCTxD_{10}$	CC	D	Sum of delay between Clk to Q of the last FF and the final output buffer, falling edge	—	25	ns

1. TxD pin load maximum 25 pF.
2. Pad configured as VERY STRONG.
3. Sum of transition time simulation is performed according to Electrical Physical Layer Specification 3.0.1 and the entire temperature range of the device has been taken into account.
4. $V_{DD\_HV\_IO}$ = 5.0 V ± 10%, Transmission line Z = 50 ohms, t_{delay} = 1 ns, C_L = 10 pF.
5. $V_{DD\_HV\_IO}$ = 3.3 V ± 10%, Transmission line Z = 50 ohms, t_{delay} = 0.6 ns, C_L = 10 pF.

Figure 46. TxD Signal propagation delays



3.18.4.3 RxD

Table 67. RxD input characteristics

Symbol		C	Characteristic	Value		Unit
				Min	Max	
C_CCRxD	CC	D	Input capacitance on RxD pin	—	7	pF
uCCLogic_1	CC	D	Threshold for detecting logic high	35	70	%

Table 67. RxD input characteristics (continued)

Symbol		C	Characteristic	Value		Unit
				Min	Max	
uCCLogic_0	CC	D	Threshold for detecting logic low	30	65	%
$dCCRxD_{01}$	CC	D	Sum of delay from actual input to the D input of the first FF, rising edge	—	10	ns
$dCCRxD_{10}$	CC	D	Sum of delay from actual input to the D input of the first FF, falling edge	—	10	ns
dCCRxAsymAccept15	CC	D	Acceptance of asymmetry at receiving CC with 15 pF load	–31.5	44	ns
dCCRxAsymAccept25	CC	D	Acceptance of asymmetry at receiving CC with 25 pF load	–30.5	43	ns

3.18.5 PSI5 timing

The following table describes the PSI5 timing.

Table 68. PSI5 timing

Symbol		C	Parameter	Value		Unit
				Min	Max	
t_{MSG_DLY}	CC	D	Delay from last bit of frame (CRC0) to assertion of new message received interrupt	—	3	µs
t_{SYNC_DLY}	CC	D	Delay from internal sync pulse to sync pulse trigger at the SDOUT_PSI5_n pin	—	2	µs
t_{MSG_JIT}	CC	D	Delay jitter from last bit of frame (CRC0) to assertion of new message received interrupt	—	1	cycles(1)
t_{SYNC_JIT}	CC	D	Delay jitter from internal sync pulse to sync pulse trigger at the SDOUT_PSI5_n pin	—	+/-±(1 PSI5_1µs_CLK + 1 PBRIDGEn_CLK)	cycles

1. Measured in PSI5 clock cycles (PBRIDGEn_CLK on the device). Minimum PSI5 clock period is 20 ns.

3.18.6 CAN timing

The following table describes the CAN timing.

Table 69. CAN timing

Symbol		C	Parameter	Condition	Value			Unit
					Min	Typ	Max	
$t_{P(RX:TX)}$	CC	D	CAN controller propagation delay time standard pads	Medium type pads 25pF load	—	—	70	ns
	CC	D		Medium type pads 50pF load	—	—	80	
	CC	D		STRONG, VERY STRONG type pads 25pF load	—	—	60	
	CC	D		STRONG, VERY STRONG type pads 50pF load	—	—	65	

3.18.7 UART timing

UART channel frequency support is shown in the following table.

Table 70. UART frequency support

LINFlexD clock frequency LIN_CLK (MHz)	Oversampling rate	Voting scheme	Max usable frequency (Mbaud)
80	16	3:1 majority voting	5
	8		10
	6	Limited voting on one sample with configurable sampling point	13.33
	5		16
	4		20
100	16	3:1 majority voting	6.25
	8		12.5
	6	Limited voting on one sample with configurable sampling point	16.67
	5		20
	4		25

3.18.8 I2C timing

The I^2C AC timing specifications are provided in the following tables.

Note: In the following table, I2C input timing is valid for Automotive and TTL inputs levels, hysteresis enabled, and an input edge rate no slower than 1 ns (10% – 90%).

Table 71. I2C input timing specifications – SCL and SDA

No.	Symbol		C	Parameter	Value		Unit
					Min	Max	
1	—	CC	D	Start condition hold time	2	—	PER_CLK Cycle(1)
2	—	CC	D	Clock low time	8	—	PER_CLK Cycle

Table 71. I2C input timing specifications – SCL and SDA (continued)

No.	Symbol		C	Parameter	Value		Unit
					Min	Max	
3	—	CC	D	Bus free time between Start and Stop condition	4.7	—	µs
4	—	CC	D	Data hold time	0.0	—	ns
5	—	CC	D	Clock high time	4	—	PER_CLK Cycle
6	—	CC	D	Data setup time	0.0	—	ns
7	—	CC	D	Start condition setup time (for repeated start condition only)	2	—	PER_CLK Cycle
8	—	CC	D	Stop condition setup time	2	—	PER_CLK Cycle

1. PER_CLK is the SoC peripheral clock, which drives the I^2C BIU and module clock inputs. See the Clocking chapter in the device reference manual for more detail.

Note: In the following table:

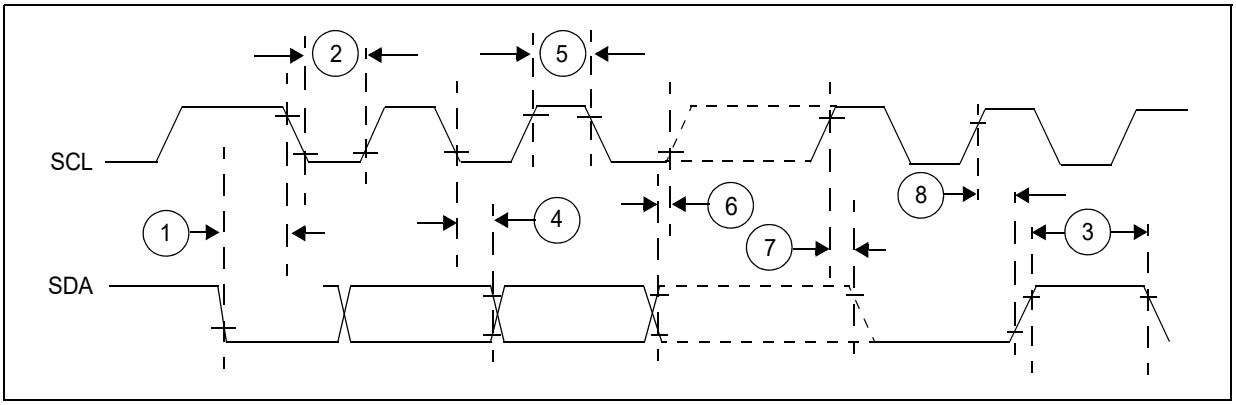
- *All output timing is worst case and includes the mismatching of rise and fall times of the output pads.*
- *Output parameters are valid for CL = 25 pF, where CL is the external load to the device (lumped). The internal package capacitance is accounted for, and does not need to be subtracted from the 25 pF value.*
- *Timing is guaranteed to same drive capabilities for all signals, mixing of pad drives may reduce operating speeds and may cause incorrect operation.*
- *Programming the IBFD register (I2C bus Frequency Divider) with the maximum frequency results in the minimum output timings listed. The I2C interface is designed to scale the data transition time, moving it to the middle of the SCL low period. The actual position is affected by the pre-scale and division values programmed in the IBC field of the IBFD register.*

Table 72. I2C output timing specifications — SCL and SDA

No.	Symbol		C	Parameter	Value		Unit
					Min	Max	
1	—	CC	D	Start condition hold time	6	—	PER_CLK Cycle(1)
2	—	CC	D	Clock low time	10	—	PER_CLK Cycle
3	—	CC	D	Bus free time between Start and Stop condition	4.7	—	µs
4	—	CC	D	Data hold time	7	—	PER_CLK Cycle
5	—	CC	D	Clock high time	10	—	PER_CLK Cycle
6	—	CC	D	Data setup time	2	—	PER_CLK Cycle
7	—	CC	D	Start condition setup time (for repeated start condition only)	20	—	PER_CLK Cycle
8	—	CC	D	Stop condition setup time	10	—	PER_CLK Cycle

1. PER_CLK is the SoC peripheral clock, which drives the I^2C BIU and module clock inputs. See the Clocking chapter in the device reference manual for more detail.

Figure 47. I²C input/output timing



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

The following table lists the case numbers for SPC58xNx.

Table 73. Package case numbers

Package type	Device type
eLQFP176	Production
FPBGA292	Production

4.1 eLQFP176 package information

Refer to *Section 4.1.1: Package mechanical drawings and data information* for full description of below figures and table notes.

Figure 48. eLQFP176 package outline

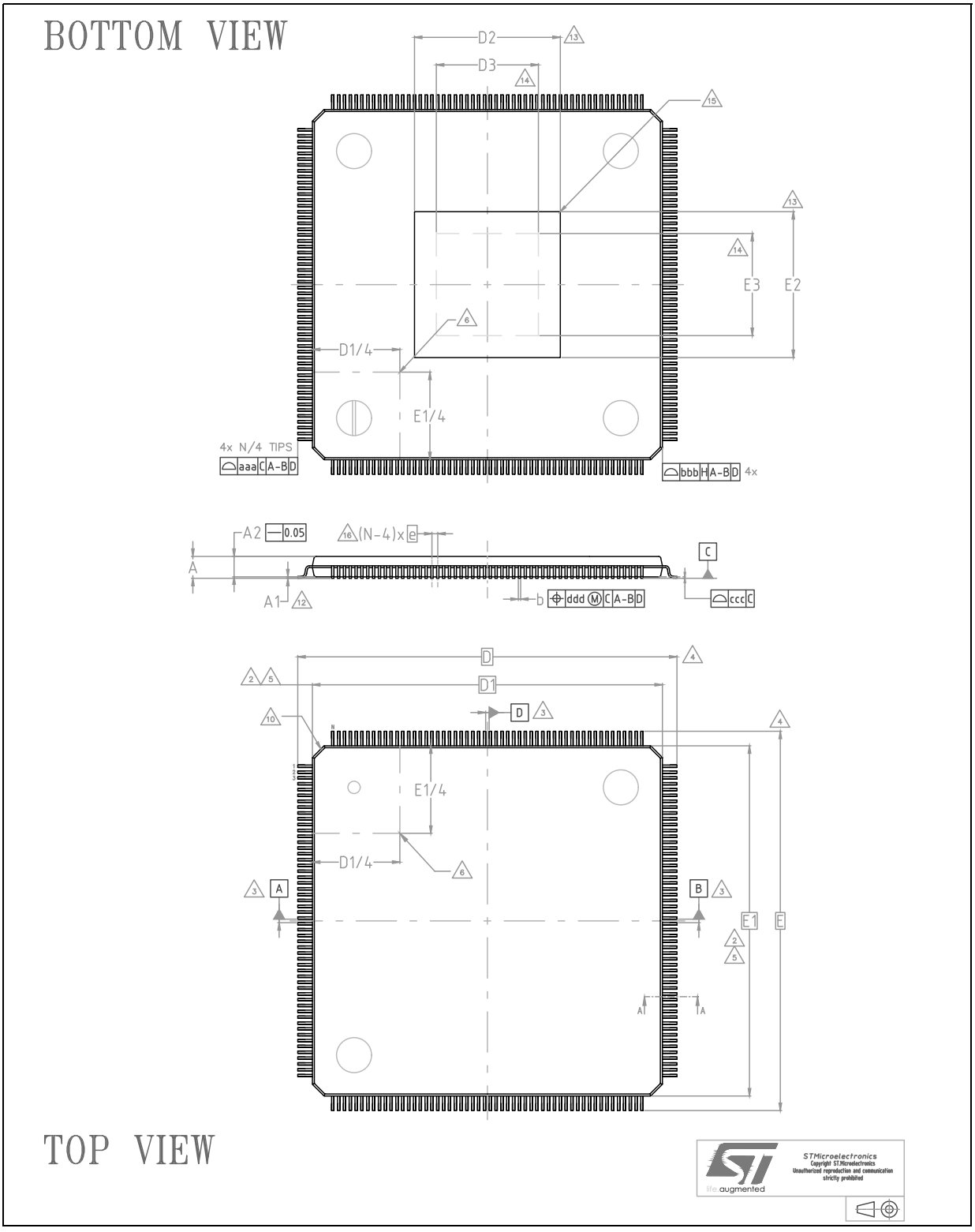


Figure 49. eLQFP176 section A-A

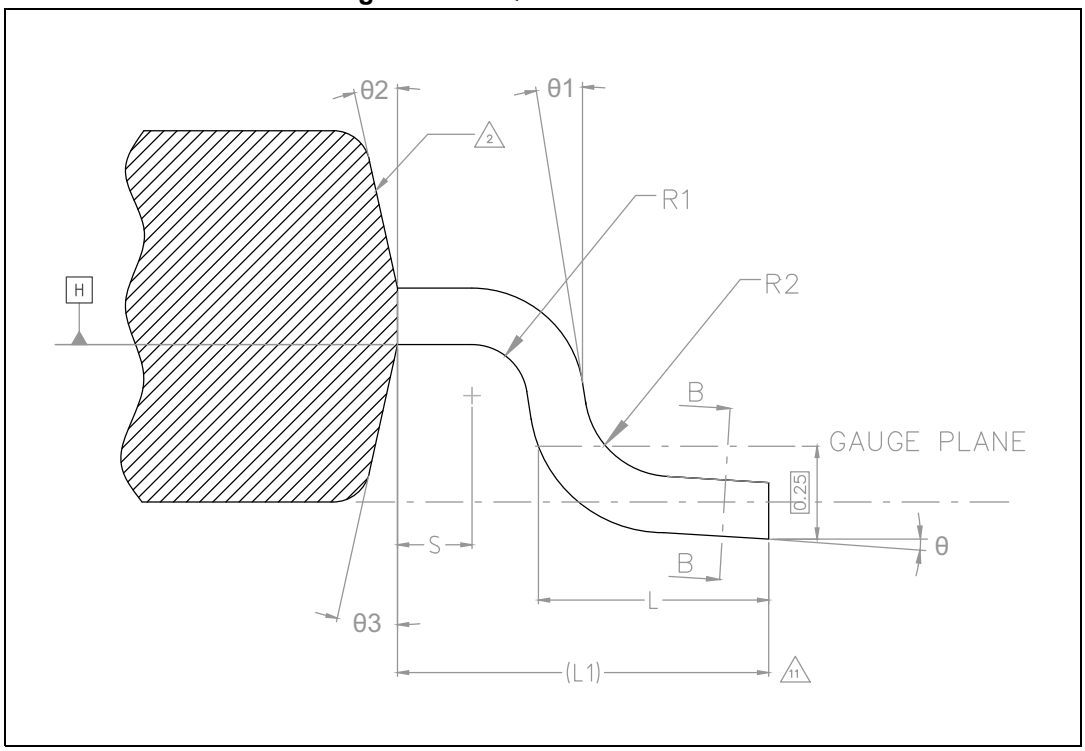


Figure 50. eLQFP176 section B-B

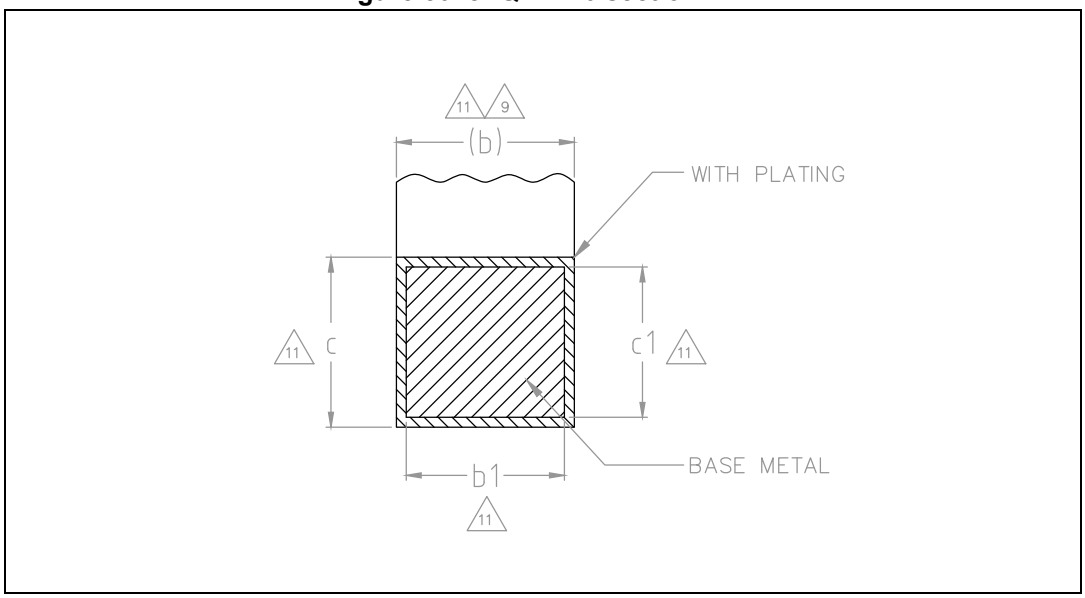


Table 74. eLQFP176 package mechanical data

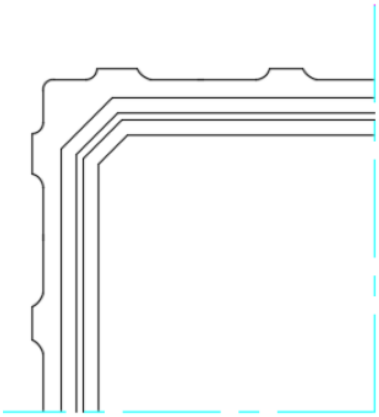
Symbol	Dimensions[7],[17]		
	Min.	Nom.	Max.
Θ	0°	3.5°	7°
Θ1	0°	—	—
Θ2	10°	12°	14°
Θ3	10°	12°	14°
A[15]	—	—	1.60
A1[12]	0.05	—	0.15
A2[15]	1.35	1.40	1.45
b[8],[9],[11]	0.17	0.22	0.27
b1[11]	0.17	0.20	0.23
c[11]	0.09	—	0.20
c1[11]	0.09	—	0.16
D[4]	26.00 BSC		
D1[2],[5]	24.00 BSC		
D2[13]	—	—	8.97
D3[14]	7.30	—	—
e	0.50 BSC		
E[4]	26.00 BSC		
E1[2],[5]	24.00 BSC		
E2[13]	—	—	8.97
E3[14]	7.30	—	—
L	0.45	0.60	0.75
L1	1.00 REF		
N[16]	176		
R1	0.08	—	—
R2	0.08	—	0.20
S	0.20	—	
aaa[1],[18]	0.20		
bbb[1],[18]	0.20		
ccc[1],[18]	0.08		
ddd[1],[18]	0.08		

4.1.1 Package mechanical drawings and data information

The following notes are related to *Figure 48*, *Figure 49*, *Figure 50* and *Table 74*:

1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994.
2. The Top package body size may be smaller than the bottom package size by as much as 0.15 mm.
3. Datums A-B and D to be determined at datum plane H.
4. To be determined at seating datum plane C.
5. Dimensions D1 and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is “0.25 mm” per side. D1 and E1 are Maximum plastic body size dimensions including mold mismatch.
6. Details of pin 1 identifier are optional but must be located within the zone indicated.
7. All dimensions are in millimeter except where explicitly noted.
8. No intrusion allowed inwards the leads.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum “b” dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.
10. Exact shape of each corner is optional.
11. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
12. A1 is defined as the distance from the seating plane to the lowest point on the package body.
13. Dimensions D2 and E2 show the maximum exposed metal area on the package surface where the exposed pad is located (if present). It includes all metal protrusions from exposed pad itself. Type of exposed pad on SPC58xNx is as *Figure 51*. End user should verify D2 and E2 dimensions according to the specific device application.
14. Dimensions D3 and E3 show the minimum solderable area, defined as the portion of exposed pad which is guaranteed to be free from resin flashes/bleeds, bordered by internal edge of inner groove.
15. The optional exposed pad is generally coincident with the top or bottom side of the package and not allowed to protrude beyond that surface.
16. “N” is the max number of terminal positions for the specified body size.
17. Critical dimensions:
    a) Stand-Off
    b) Overall Width
    c) Lead Coplanarity
18. For symbols, recommended values and tolerances, see *Table 75*.

Figure 51. eLQFP176 leadframe pad design



Note: number, dimensions and positions of grooves are for reference only.

Table 75. eLQFP176 symbol definitions

Symbol	Definition	Notes
aaa	The tolerance that controls the position of the terminal pattern with respect to Datum A and B. The center of the tolerance zone for each terminal is defined by basic dimension e as related to Datum A and B.	For flange-molded packages, this tolerance also applies for basic dimensions D1 and E1. For packages tooled with intentional terminal tip protrusions, aaa does not apply to those protrusions.
bbb	The bilateral profile tolerance that controls the position of the plastic body sides. The centers of the profile zones are defined by the basic dimensions D and E.	—
ccc	The unilateral tolerance located above the seating plane where in the bottom surface of all terminals must be located.	This tolerance is commonly know as the “coplanarity” of the package terminals.
ddd	The tolerance that controls the position of the terminals to each other. The centers of the profile zones are defined by basic dimension e.	This tolerance is normally compounded with tolerance zone defined by “b”.

4.2 FPBGA292 package information

Refer to *Section 4.2.1: Package mechanical drawings and data information* for full description of below figures and table notes.

Figure 52. FPBGA292 package outline

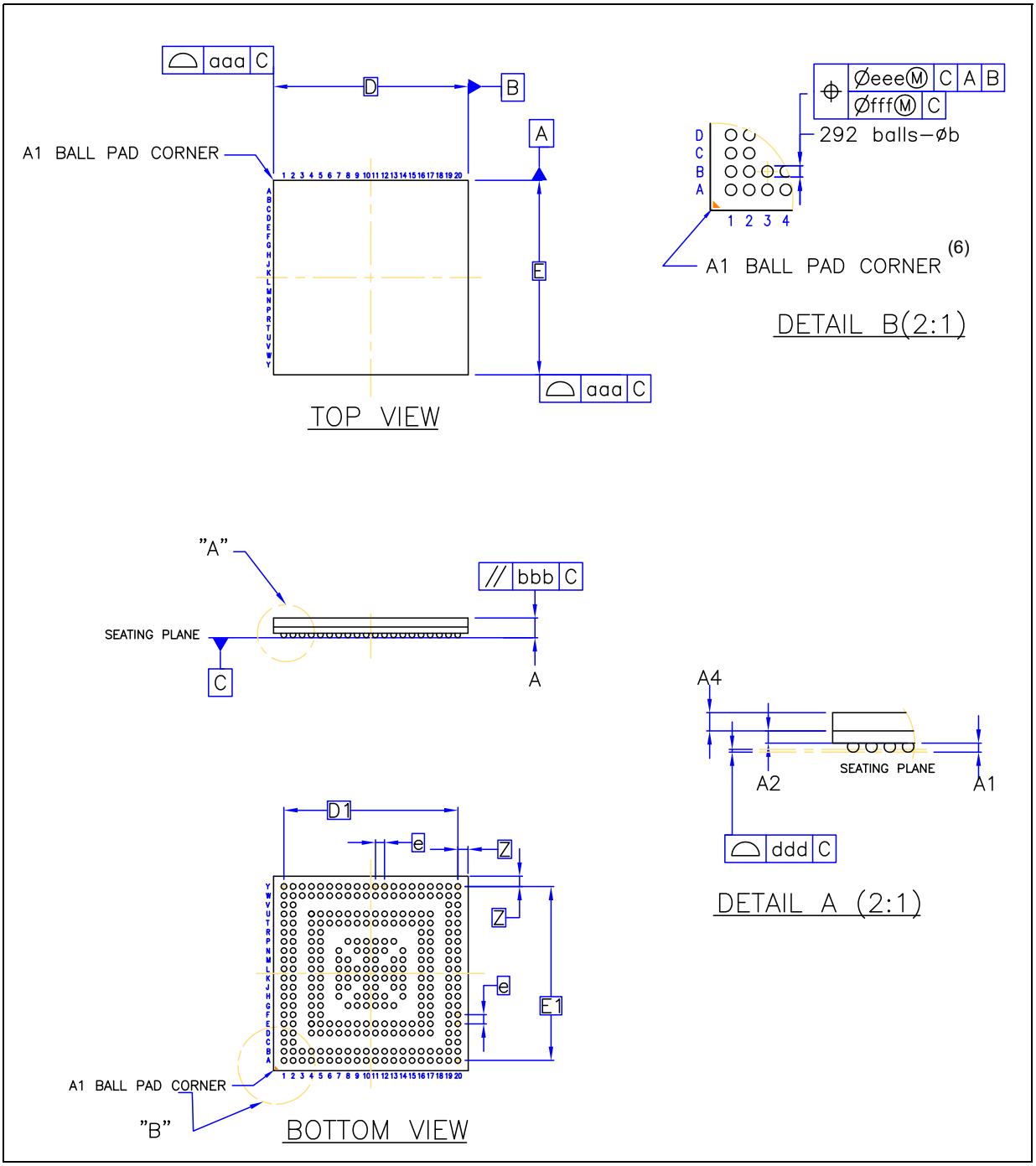


Table 76. FPBGA292 package mechanical data

Symbol	Dimensions (in millimeter)		
	Min.	Typ.	Max.
A(1)	–	–	1.8
A1	0.35	–	–

Table 76. FPBGA292 package mechanical data (continued)

Symbol	Dimensions (in millimeter)		
	Min.	Typ.	Max.
A2	–	0.53	–
A4	–	–	0.80
D	16.85	17.00	17.15
D1	–	15.20	–
E	16.85	17.00	17.15
E1	–	15.20	–
e	–	0.80	–
b(2)	0.50	0.55	0.60
Z	–	0.90	–
aaa	–	–	0.15
bbb	–	–	0.10
ddd(3)	–	–	0.12
eee(4)	–	–	0.15
fff(5)	–	–	0.08

4.2.1 Package mechanical drawings and data information

The following notes are related to *Figure 52* and *Table 76*:

1. FPBGA stands for Fine Pitch Plastic Ball Grid Array.
   Fine pitch: e < 1.00 mm pitch.
   Low Profile: The total profile height (Dim A) is measured from the seating plane to the top of the component.
   The maximum total package height is calculated by the following methodology (tolerance values):

$$Amax = A_1(TYP) + A_2(TYP) + A_4(TYP) + \sqrt{(A_1)^2 + (A_2)^2 + (A_4)^2}$$

2. The typical ball diameter before mounting is 0.55mm.
3. Ref. JEDEC MO_219G_BGA Low Profile, Fine Pitch Ball Grid Array Family, 0.80MM Pitch (SQ. & RECT.)
4. The tolerance of position that controls the location of the pattern of balls with respect to datums A and B. For each ball there is a cylindrical tolerance zone eee perpendicular to datum C and located on true position with respect to datums A and B as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone.
5. The tolerance of position that controls the location of the balls within the matrix with respect to each other. For each ball there is a cylindrical tolerance zone fff perpendicular to datum C and located on true position as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone. Each tolerance zone fff in the array is contained entirely in the respective zone eee above. The axis of each ball must lie simultaneously in both tolerance zones.

6. The terminal A1 corner must be identified on the top surface by using a corner chamfer, ink or metallized markings, or other feature of package body or integral heatslug. A distinguishing feature is allowable on the bottom surface of the package to identify the terminal A1 corner. Exact shape of each corner is optional.

4.3 Package thermal characteristics

The following tables describe the thermal characteristics of the device. The parameters in this chapter have been evaluated by considering the device consumption configuration reported in the *Section 3.7: Device consumption*.

4.3.1 LQFP176

Table 77. Thermal characteristics for 176 exposed pad LQFP package

Symbol		C	Parameter[1]	Conditions	Value	Unit
$R_{\theta JA}$	CC	D	Junction-to-Ambient, Natural Convection[2]	Four layer board (2s2p)	21	°C/W
$R_{\theta JMA}$	CC	D	Junction-to-Moving-Air, Ambient[2]	at 200 ft./min., four layer board (2s2p)	15.5	°C/W
$R_{\theta JB}$	CC	D	Junction-to-board[3]	—	9.2	°C/W
$R_{\theta JCtop}$	CC	D	Junction-to-case top[4]	—	7.6	°C/W
$R_{\theta JCbottom}$	CC	D	Junction-to-case bottom[5]	—	1	°C/W
Ψ_{JT}	CC	D	Junction-to-package top[6]	Natural convection	1	°C/W

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.
3. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
4. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
5. Thermal resistance between the die and the exposed pad ground on the bottom of the package based on simulation without any interface resistance.
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

4.3.2 FPBGA292

Table 78. Thermal characteristics for 292-pin FPBGA

Symbol		C	Parameter[1]	Conditions	Value	Unit
$R_{\theta JA}$	CC	D	Junction-to-Ambient, Natural Convection [2]	Four layer board (2s2p)	22.2	°C/W
$R_{\theta JB}$	CC	D	Junction-to-board[3]	—	10.5	°C/W
$R_{\theta JC}$	CC	D	Junction-to-case[4]	—	6.7	°C/W
Ψ_{JT}	CC	D	Junction-to-package top[5]	Natural convection	1	°C/W

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-6 with the board (JESD51-9) horizontal.
3. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
4. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
5. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

4.3.3 General notes for specifications at maximum junction temperature

An estimation of the chip junction temperature, T_J, can be obtained from the equation:

Equation 1
$T_J = T_A + (R_{\theta JA} * P_D)$

where:

T_A = ambient temperature for the package (°C)

$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)

P_D = power dissipation in the package (W)

The thermal resistance values used are based on the JEDEC JESD51 series of standards to provide consistent values for estimations and comparisons. The differences between the values determined for the single-layer (1s) board compared to a four-layer board that has two signal layers, a power and a ground plane (2s2p), demonstrate that the effective thermal resistance is not a constant. The thermal resistance depends on the:

- Construction of the application board (number of planes)
- Effective size of the board which cools the component
- Quality of the thermal and electrical connections to the planes
- Power dissipated by adjacent components

Connect all the ground and power balls to the respective planes with one via per ball. Using fewer vias to connect the package to the planes reduces the thermal performance. Thinner planes also reduce the thermal performance. When the clearance between the vias leaves the planes virtually disconnected, the thermal performance is also greatly reduced.

As a general rule, the value obtained on a single-layer board is within the normal range for the tightly packed printed circuit board. The value obtained on a board with the internal planes is usually within the normal range if the application board has:

- One oz. (35 micron nominal thickness) internal planes
- Components are well separated
- Overall power dissipation on the board is less than 0.02 W/cm^2

The thermal performance of any component depends on the power dissipation of the surrounding components. In addition, the ambient temperature varies widely within the application. For many natural convection and especially closed box applications, the board temperature at the perimeter (edge) of the package is approximately the same as the local air temperature near the device. Specifying the local ambient conditions explicitly as the board temperature provides a more precise description of the local ambient conditions that determine the temperature of the device.

At a known board temperature, the junction temperature is estimated using the following equation:

Equation 2
$T_J = T_B + (R_{\theta JB} * P_D)$

where:

T_B = board temperature for the package perimeter (°C)

$R_{\theta JB}$ = junction-to-board thermal resistance (°C/W) per JESD51-8

P_D = power dissipation in the package (W)

When the heat loss from the package case to the air does not factor into the calculation, the junction temperature is predictable if the application board is similar to the thermal test condition, with the component soldered to a board with internal planes.

The thermal resistance is expressed as the sum of a junction-to-case thermal resistance plus a case-to-ambient thermal resistance:

Equation 3

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)

$R_{\theta JC}$ = junction-to-case thermal resistance (°C/W)

$R_{\theta CA}$ = case to ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device related and is not affected by other factors. The thermal environment can be controlled to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For example, change the air flow around the device, add a heat sink, change the mounting arrangement on the printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device. This description is most useful for packages with heat sinks where 90% of the heat flow is through the case to heat sink to ambient. For most packages, a better model is required.

A more accurate two-resistor thermal model can be constructed from the junction-to-board thermal resistance and the junction-to-case thermal resistance. The junction-to-case thermal resistance describes when using a heat sink or where a substantial amount of heat is dissipated from the top of the package. The junction-to-board thermal resistance describes the thermal performance when most of the heat is conducted to the printed circuit board. This model can be used to generate simple estimations and for computational fluid dynamics (CFD) thermal models. More accurate compact Flotherm models can be generated upon request.

To determine the junction temperature of the device in the application on a prototype board, use the thermal characterization parameter (Ψ_{JT}) to determine the junction temperature by measuring the temperature at the top center of the package case using the following equation:

Equation 4

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

T_T = thermocouple temperature on top of the package (°C)

Ψ_{JT} = thermal characterization parameter (°C/W)

P_D = power dissipation in the package (W)

The thermal characterization parameter is measured in compliance with the JESD51-2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. Position the thermocouple so that the thermocouple junction rests on the package. Place a small amount of epoxy on the thermocouple junction and approximately 1 mm of wire extending from the junction. Place the thermocouple wire flat against the package case to avoid measurement errors caused by the cooling effects of the thermocouple wire.

When board temperature is perfectly defined below the device, it is possible to use the thermal characterization parameter (Ψ_{JPB}) to determine the junction temperature by

measuring the temperature at the bottom center of the package case (exposed pad) using the following equation:

Equation 5

$$T_J = T_B + (\Psi_{JPB} \times P_D)$$

where:

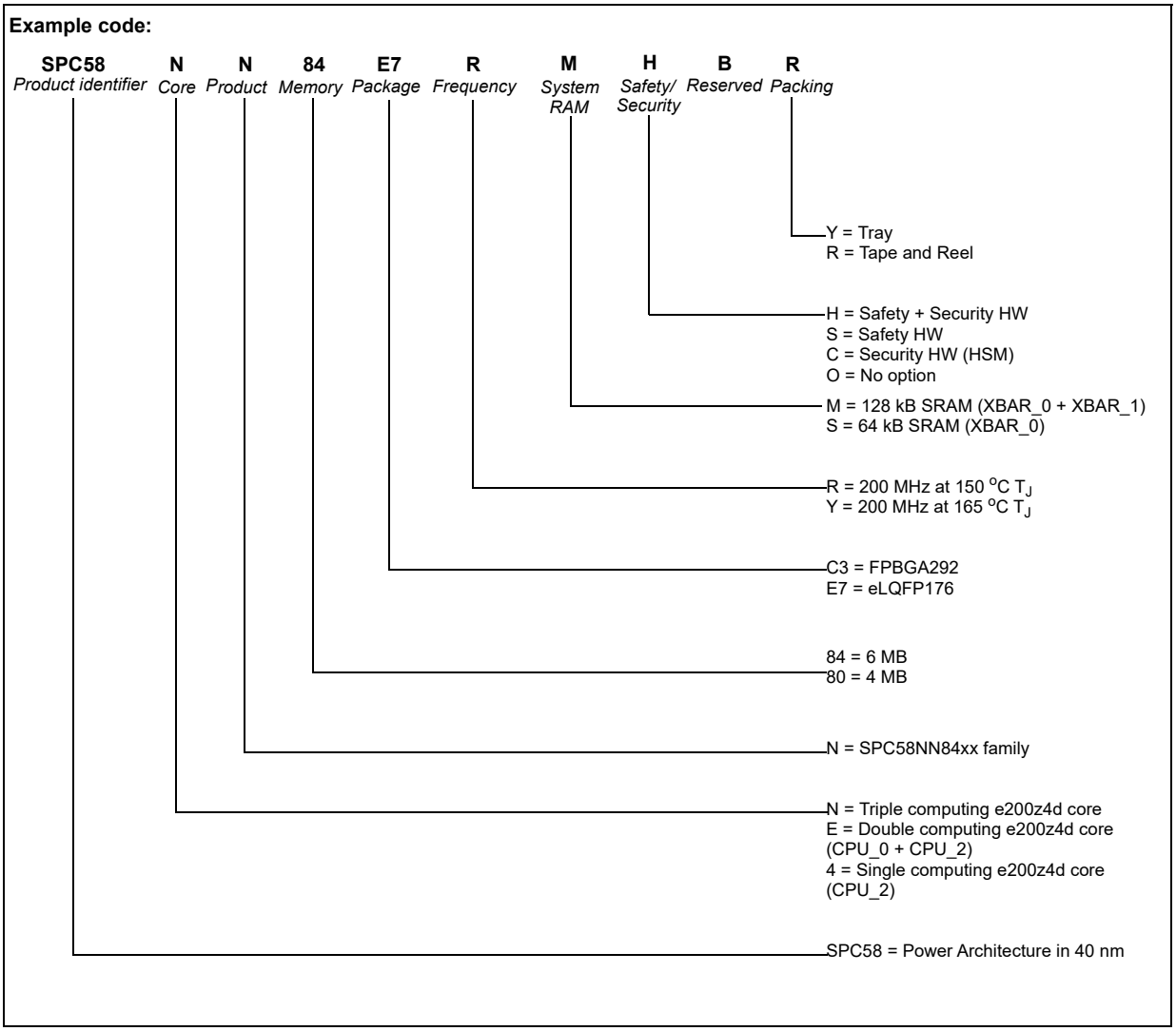
T_T = thermocouple temperature on bottom of the package (°C)

Ψ_{JT} = thermal characterization parameter (°C/W)

P_D = power dissipation in the package (W)

5 Ordering information

Figure 53. Ordering information scheme



Note: Please contact your ST sales office to ask for the availability of a particular commercial product.

Features (for instance flash, RAM or peripherals) not included in the commercial product cannot be used. ST cannot be called to take any liability for features used outside the commercial product.

Table 79. Code Flash options

SPC58xN84 (6M)	SPC58xN80 (4M)	Partition	Start address	End address
16	16	0	0x00FC0000	0x00FC3FFF
16	16	0	0x00FC4000	0x00FC7FFF
16	16	1	0x00FC8000	0x00FCBFFF

Table 79. Code Flash options (continued)

SPC58xN84 (6M)	SPC58xN80 (4M)	Partition	Start address	End address
16	16	1	0x00FCC000	0x00FCFFFF
32	32	0	0x00FD0000	0x00FD7FFF
32	32	1	0x00FD8000	0x00FDFFFF
64	64	0	0x00FE0000	0x00FEFFFF
64	64	0	0x00FF0000	0x00FFFFFF
128	128	0	0x01000000	0x0101FFFF
128	128	1	0x01020000	0x0103FFFF
256	256	0	0x01040000	0x0107FFFF
256	256	0	0x01080000	0x010BFFFF
256	256	0	0x010C0000	0x010FFFFF
256	256	0	0x01100000	0x0113FFFF
256	256	0	0x01140000	0x0117FFFF
256	256	0	0x01180000	0x011BFFFF
256	256	0	0x011C0000	0x011FFFFF
256	256	1	0x01200000	0x0123FFFF
256	256	1	0x01240000	0x0127FFFF
256	256	1	0x01280000	0x012BFFFF
256	256	1	0x012C0000	0x012FFFFF
256	256	1	0x01300000	0x0133FFFF
256	256	1	0x01340000	0x0137FFFF
256	256	1	0x01380000	0x013BFFFF
256	NA	5	0x013C0000	0x013FFFFF
256	NA	5	0x01400000	0x0143FFFF
256	NA	5	0x01440000	0x0147FFFF
256	NA	5	0x01480000	0x014BFFFF
256	NA	5	0x014C0000	0x014FFFFF
256	NA	5	0x01500000	0x0153FFFF
256	NA	5	0x01540000	0x0157FFFF
256	NA	5	0x01580000	0x015BFFFF

Table 80. RAM options [1]

SPC58NN84	SPC58EN84	SPC58EN80	SPC584N80	Type	Start address	End address
512	512	512	512			
64	64	64	64	PRAMC_0	0x40070000	0x4007FFFF
64	64	64	64	PRAMC_2	0x40080000	0x4008FFFF
128	128	128	128	D_MEM CPU_0	0x50800000	0x5081FFFF
128	128	128	128	D_MEM CPU_1	0x51800000	0x5181FFFF
128	128	128	128	D_MEM CPU_2	0x52800000	0x5281FFFF

1. RAM size is the sum of TCM and SRAM.

6 Revision history

Table 81. Document revision history

Date	Revision	Changes
13-Jul-2016	1	Initial release.
27-Jun-2017	2	Following are the changes for this release of the document: Updated the cover page. *Table 2: SPC58xNx feature summary*: – Updated the table. *Section 1.5: Features*: – Updated the bullet points in this section. *Section 3.1: Introduction*: – Removed text “The IPs and...for the details”. – Removed the two notes. *Chapter 2: Package pinouts and signal descriptions*: – Updated this section. *Table 3: Parameter classifications*: – Updated the description of classification tag “T”. *Table 4: Absolute maximum ratings*: – For parameter “I_{INJ}”, text “DC” removed from description. – Added text “Exposure to absolute ... reliability” – Added text “even momentarily” – Updated values in conditions column. – Added parameter T_{TRIN}. – For parameter “T_{STG}”, maximum value updated from “175” to “125” – Added new parameter “T_{PAS}” – For parameter “I_{INJ}”, description updated from “maximum...PAD” to “maximum DC...pad” *Table 5: Operating conditions*: – Footnote “1.260 V - 1.290 V range .. temperature profile” updated to Text “... average supply value below or equal to 1.236 V ...” – Footnote “Positive and negative Dynamic current ... Pulse 3b (ISO 7637-2:2011 5.6.3)”: Text added “... Pulse 2a(ISO 7637-2:2011 5.6.2) ...” – Added footnote “The maximum number...” to parameter F_{SYS}. – For parameter “V_{DD_LV}”, changed the classification from “D” to “P” – For parameter “$V_{DD\_HV\_ADR\_S}$-$V_{DD\_HV\_ADV}$”, swapped the conditions and Min columns. – For parameter “V_{DD_LV}”, updated the table footnote in min column. – For parameter “V_{DD_LV}”, added footnote “If the internal LVD100...” – For parameter “$V_{DD\_HV\_ADR\_S}$”, removed the second row. – For parameter $V_{DD\_HV\_ADR\_S}$-$V_{DD\_HV\_ADV}$, updated the min value. – Removed note “Core voltage as ....” – Changed the max value of parameter V_{RAMP_LV} to “20”.

Table 81. Document revision history (continued)

Date	Revision	Changes
27-Jun-2017	2 (cont')	*Table 6: PRAM wait states configuration*: – Added this new table. *Section 3.6: Temperature profile*: – Added text "Mission profile with junction....representative for validation". *Table 7: Device supply relation during power-up/power-down sequence*: – Updated the table. – "$V_{DD\_HV\_PMC}$" removed from Supply 2. *Table 9: Device consumption*: – Updated table and its values. *Section 3.8: I/O pad specification*: – Replaced all occurrences of "50 pF load" with "CL=50pF". – Removed note "The external ballast...." *Section 3.8.2: I/O output DC characteristics*: – Changed "WEAK" to "WEAK/SLOW" – Changed "STRONG" to "STRONG/FAST" – Changed "VERY STRONG" to "VERY STRONG / VERY FAST" – Added note "10%/90% is the...." *Table 11: I/O input electrical characteristics*: – Added parameter "V_{ihcmos} BD" – Updated footnote 1 – For parameter V_{ihcmos} BD, replaced classification "P" with "T", and updated conditions column. – Added "Automotive" levels. – Added note "In case of current..." – For parameter "Vihcmos BD", swapped the conditions for off and on. *Table 13: WEAK/SLOW I/O output characteristics*: – Added "10%-90% in description of parameter "t_{TR_W}". – For parameter "F_{max_W}", updated condition "25 pF load" to "CL=25pF" – For parameter "t_{TR_S}", changed min value (25 pF load) from "4" to "3" – Changed min value (50 pF load) from "6" to "5" – For parameter "$\|t_{SKEW\_W}\|$", changed max value from "30" to "25". *Table 14: MEDIUM I/O output characteristics*: – Added "10%-90% in description of parameter "t_{TR_M}". – For parameter "$\|t_{SKEW\_M}\|$", changed max value from "30" to "25". *Table 15: STRONG/FAST I/O output characteristics*: – Added "10%-90% in description of parameter "t_{TR_S}". – Parameter "I_{DCMAX_S}" updated: – Condition added "V_{DD}=5V±10% – Condition added "V_{DD}=3.3V±10%, Max value updated to 5.5mA – For parameter "$\|t_{SKEW\_S}\|$", changed max value from "30" to "25".

Table 81. Document revision history (continued)

Date	Revision	Changes
27-Jun-2017	2 (cont')	*Table 17: I/O consumption*: – Updated all the max values of parameters I_{DYN_W} and I_{DYN_M} *Table 19: Reset Pad state during power-up and reset*: – Added this table. *Table 20: PLL0 electrical characteristics*: – For parameter "I_{PLL0}", classification changed from "C" to "T". – Footnote "Jitter values...measurement" added for parameters: $\lvert\Delta_{PLL0PHI0SPJ}\rvert$ $\lvert\Delta_{PLL0PHI1SPJ}\rvert$ $\Delta_{PLL0LTJ}$ *Table 21: PLL1 electrical characteristics*: – For parameter "I_{PLL1}", classification changed from "C" to "T". – Footnote "Jitter values...measurement" added for parameter "$\lvert\Delta_{PLL1PHI0SPJ}\rvert$" *Section 3.11: Oscillators*: Added this section. *Table 25: SARn ADC electrical specification*: – Footnote "The injected current...only adjacent ones" updated to "All channels of all SAR-ADC12bit ... to current injection" – For parameter f_{ADCK} (High frequency mode), changed min value from "7.5" to "> 13.33". – Deleted footnote "Values are subject to change (possibly improved to ±2 LSB) after characterization" – Added footnote "When using a GAIN ... resolution of 15 bits" to parameter "RESOLUTION". – Added footnote "Conversion offset ... offset error" to parameter V_{OFFSET}. – Removed footnote "SNR value guaranteed ... frequency range" from parameters- $SNR_{DIFF150}$ and $SNR_{DIFF333}$. – In V_{cmrr}, changed "SR" to "CC" and "D" to "T" – Changed min value from "1.5" to "—" in parameter "I_{ADV_D}" – Changed min value from "3" to "—" in parameter "ΣI_{ADR_D}". – Added footnote "Consumption is given ... set-up" to parameter "ΣI_{ADR_D}" – Removed footnote "Sampling is .... $f_{ADCD\_M}/2$" – Updated footnote "S/D ADC is ...12 dB" – Classification for parameter "$I_{ADCREFH}$" changed from "C" to "T". *Table 27: SDn ADC electrical specification*: – Footnote "All channels of...subject to current injection" added for parameter $\Delta_{SNRINJ2}$ – Added table footnote "This parameter ...3 dB less" to parameters - $SNR_{DIFF150}$, $SNR_{DIFF333}$, and SNR_{SE150} – Replaced the max value of ΣIADR_D of "16" with "80". – For parameter f_{ADCD_S}, updated the conditions column and added new conditions with their max values. – For parameter δ_{RIPPLE}, updated the conditions column – Added note "Propagation of the information..." to parameter $t_{LATENCY}$. – Updated all the conditions, for parameter $F_{rolloff}$ (all modes), .

Table 81. Document revision history (continued)

Date	Revision	Changes
27-Jun-2017	2 (cont')	*Table 26: ADC-Comparator electrical specification*: – Classification for parameter "$I_{ADCREFH}$" changed from "C" to "T" – Removed table footnote "Values are subject to change (possibly improved to ±2 LSB) after characterization" – For parameter C_{P2}, updated the max value to "1". *Table 24: ADC pin specification*: – For I_{LKG}, changed condition "C" to "—". Updated *Figure 8: Input equivalent circuit (Fast SARn and SARB channels)* *Table 30: Temperature sensor electrical characteristics*: – For "temperature monitoring range", classification removed (was C) *Table 31: LVDS pad startup and receiver electrical characteristics,* – For parameter ILVDS_BIAS, changed the characteristics to "C" – For parameter RIN ($V_{DD\_HV\_IO}$ = 3.3 V ± 10% -40 °C<Tj<165 °C), updated the max value to 160. *Table 32: LFAST transmitter electrical characteristics,,*: – Footnote "The transition time is measured from..." removed. *Table 35: LFAST PLL electrical characteristics*: – Min and Max value of parameter "ERR_{REF}" updated from "TBD" to "-1" and "+1" respectively – Max value of parameter "PN" updated from "TBD" to "-58" – Frequency of parameter "ΔPER_{REF}" updated from "10MHz" to "20MHz". – Max value of parameter "ΔPER_{REF}" for condition "Single period" updated from "TBD" to "350" – Min and Max value of parameter "ΔPER_{REF}" for condition "Long period" updated from "TBD" to "-500" and "+500" respectively. *Table 37: Power management regulators*: – Removed text "In parts packaged with LQFP176, the auxiliary and clamp regulators cannot be enabled" from note 2. – Added table footnote 4: Parts with SMPS enabled can only be used in this mode and EXTREG_SEL has to be set to V_{SS} – Added footnote "Parts with ... be set to VSS" to Bernina. – Removed note "Standby regulator ..". – Removed text "In parts packaged with LQFP176...." from note 2. *Table 38: External components integration*: – For PMOS, replaced "STT4P3LLH6" with "PMPB100XPEA" – For NMOS, replaced "STT6N3LLH6" with "PMPB55XNEA" – Added table footnote to typ value of C_{S2}. – Updated the parameters under "SMPS Regulator Mode" – Removed table footnote "External components number....." *Table 41: SMPS Regulator specifications*: – Removed "Power-up, before trimming, no load", from V_{SMPS}. – Updated the Min, Typ, and Max values for "After trimming, max load" – Added parameter $\delta F_{SMPS.}$ – Updated parameter V_{SMPS}. – Added new parameter δF_{SMPS}

Table 81. Document revision history (continued)

Date	Revision	Changes
27-Jun-2017	2 (cont')	*Table 42: Voltage monitor electrical characteristics*: – For V_{POR031_C}, changed the max value from 0.85 to 0.97. – For $T_{VMFILTER}$, replaced T with D. – Min value of "V_{POR200_C}" updated from "1.96" to "1.80" – Max value of "V_{POR031_C}" updated from ".85" "0.97" – Changed the min value of parameter V_{POR200_C} from "1.96" to "1.80" – Changed the max value of parameter V_{POR031_C} from "0.85" to "0.97" – Changed the condition of parameter $T_{VMFILTER}$ from "T" to "D" *Table 39: Auxiliary regulator specifications*: – Classification of parameter "IDD_{AUX}" changed from "T" to "P". *Figure 15: Voltage monitor threshold definition*: – Updated the figure. *Section 3.17: Flash memory*: – Updated this section. *Figure 27: DSPI CMOS master mode — classic timing, CPHA = 1*: – Updated this figure. *Table 47: Nexus debug port timing*: – Classification of parameters "t_{EVTIPW}" and "t_{EVTOPW}" changed from "P" to "D". *Table 51: DSPI channel frequency support*: – Added column to show slower and faster frequencies. *Table 53: DSPI CMOS master modified timing (full duplex and output only) MTFE = 1, CPHA = 0 or 1*: – Changed the Min value of tSCK (very strong) from 33 to 59. *Table 54: DSPI LVDS master timing — full duplex — modified transfer format (MTFE = 1), CPHA = 0 or 1*: – Added footnote "LVDS differential load considered is the capacitance on each terminal of the differential pair, as shown in *Figure 12*" to t_{SCK}. *Table 55: DSPI LVDS master timing – output only – timed serial bus mode TSB = 1 or ITSB = 1, CPOL = 0 or 1, continuous SCK clock,*: – Added footnote "LVDS differential load ....". – Added column to show slower and faster frequencies. *Section 3.18.6: CAN timing*: – Added this new section. *Table 76: Thermal characteristics for 176 exposed pad LQFP package* and *Table 77: Thermal characteristics for 292-pin BGA*: – Updated the tables and its values. *Figure 51: Ordering information scheme*: – Updated the figure. *Table 78: Code Flash options*: – Added this new table. *Table 79: RAM options*: – Added this new table.

Table 81. Document revision history (continued)

Date	Revision	Changes
27-Sep-2017	3	Following are the changes for this release of the document: *Table 4: Absolute maximum ratings*: – Added text “In the range [1.26-1.33] V and if the above-mentioned.....” to note 1. *Table 9: Device consumption*: – “I_{DD_LKG}”: Classification “P” changed to “C” for all devices when T_J = 40 °C – “I_{DD_LKG}”: Added footnote “I_{DD_LKG} and I_{DD_LV} are reported as...” – “I_{DD_LV}”: added Footnote “I_{DD_LKG} and I_{DD_LV} are reported as...” *Table 20: PLL0 electrical characteristics*: – Added “f_{INFIN}” – Symbol “f_{INFIN}” : changed “C” by “—” in column “C” *Table 21: PLL1 electrical characteristics*: – Added “f_{INFIN}” – Symbol “f_{INFIN}” : changed “C” by “—” in column “C” *Table 24: ADC pin specification*: – Updated Max value for C_S *Table 25: SARn ADC electrical specification*: – Added symbols tADCINIT and tADCBIASINIT *Table 38: External components integration*: – For parameter C_{S1_B}, replaced “HV supply” with “LV supply” in parameter description column. *Figure 15: Voltage monitor threshold definition*: – Right blue line adjusted on the top figure. *Table 69: CAN timing*: – Removed parameter $t_{PLP(RX:TX)}$.

Table 81. Document revision history (continued)

Date	Revision	Changes
12-Mar-2018	4	Removed KGD symbol from Cover page *Table 1: Device summary*: Removed KGD-related data. *Chapter 2: Package pinouts and signal descriptions*: Rephrased introduction sentence since the pinout excel file will no longer be attached to the datasheet *Chapter 3: Electrical characteristics* Reformated introduction paragraph *Section 3.3: Operating conditions*: Replaced reference to IO_definition excel file by "the device pin out IO definition excel file" *Section 3.7: Device consumption*: *Table 9: Device consumption*: “I_{DD_LKG}”: Classification “P” changed to “C” for all devices when T_J = 40 °C “I_{DD_LKG}”: Added footnote “I_{DD_LKG} and I_{DD_LV} are reported as...” For I_{SPIKE} updated footnote and “SR” to “CC” and for I_{SR} updated the second footnote. “I_{DD_LV}”: added Footnote “I_{DD_LKG} and I_{DD_LV} are reported as...” Update table footnote number 4. *Section 3.8: I/O pad specification*: Reformated note from introduction Replaced all references to the IO_definitions excel file by “the device pinout IO definition excel file” *Table 15: STRONG/FAST I/O output characteristics*: updated values for t_{TR_S} for condition CL = 25 pF and CL = 50 pF *Table 16: VERY STRONG/VERY FAST I/O output characteristics* “tTR20-80” replaced by “tTR20-8_V” “tTRTTL” replaced by “tTRTTL_V” “$\Sigma t_{TR20-80}$” replaced by “$\Sigma t_{TR20-80\_V}$” *Section 3.9: Reset pad (PORST, ESR0) electrical characteristics* *Table 18: Reset PAD electrical characteristics*: replaced reference to IO_definition excel file by "Refer to the device pin out IO definition excel file" *Section 3.10: PLLs*: *Table 20: PLL0 electrical characteristics*: $\lvert\Delta_{PLL0PHI0SPJ}\rvert$: changed “T” by “D” and added pk-pk to Conditions value $\lvert\Delta_{PLL0PHI1SPJ}\rvert$: added pk-pk to Conditions value Added “f_{INFIN}” *Table 21: PLL1 electrical characteristics*: Added “f_{INFIN}” *Table 20: PLL0 electrical characteristics* and *Table 21: PLL1 electrical characteristics*: Symbol “f_{INFIN}” : changed “C” by “—” in column “C”

Table 81. Document revision history (continued)

Date	Revision	Changes
12-Mar-2018	4 (cont')	*Section 3.11: Oscillators*: *Table 22: External 40 MHz oscillator electrical specifications*:changed "i.e." by "that is" in note "Amplitude on the EXTAL... Changed table footnote 3 by: This value is determined by the crystal manufacturer and board design, and it can potentially be higher than the maximum provided. *Section 3.12: ADC system* Removed reference to KGD. *Table 24: ADC pin specification*: updated Max value for C_S updated Max value for C_S For parameter C_{P2}, updated the max value from "1" to "2". Added electrical specification for $R_{20K\Omega}$ symbol. changed Max value = 1 by 2 for Cp2 SARB channels *Table 25: SARn ADC electrical specification*: added symbols tADCINIT and tADCBIASINIT column "C" splitted and added "D" for I_{ADV_S} *Table 26: ADC-Comparator electrical specification*: column "C" splitted and added "D" for I_{ADV_S} Added "ADC comparator mode" condition to the following two parameters: $I_{ADCREFH}$ Min: - and Max: 19.5 µA $I_{ADCREFL}$ Min: - and Max: 20.5 µA *Section 3.14: LFAST pad electrical characteristics* *Figure 9: LFAST and MSC/DSPI LVDS timing definition*: Updated figure *Section 3.16: Power management* Changed "flash" by "Flash" *Table 38: External components integration*: For parameter C_{S1_B}, replaced "HV supply" with "LV supply" in parameter description column. Removed reference to KGD. *Section 3.16.1: Power management integration*: added sentence "It is recommended...device itself" for all devices *Figure 14: SMPS Regulator Mode*: figure updated and footnote added *Table 41: SMPS Regulator specifications*: For "ΔIDD_{SMPS}" updated the Min and Max values. Added a table footnote. *Section 3.17: Flash memory* *Table 44: Flash memory program and erase specifications (Continued)*: Updated *Table 45: Flash memory Life Specification*: Updated *Section 3.18: AC Specifications* *Table 69: CAN timing*: Removed parameter $t_{PLP(RX:TX)}$. added columns for "CC" and "D"

Table 81. Document revision history (continued)

Date	Revision	Changes
12-Mar-2018	4 (cont')	*Table 65: TxEN output characteristics*: added table footnote " Pad configured as VERY STRONG." *Table 66: TxD output characteristics,,*: changed note 3 to apply to the whole table *Chapter 4: Package information*: *Table 75: FPBGA292 package mechanical data*: updated Amax formula in table footnote 2. *Section 4.3: Package thermal characteristics* Reformated note from introduction *Table 77: Thermal characteristics for 292-pin BGA*: Updated values for $R_{\theta JA,}$ $R_{\theta JB}$ and $R_{\theta JC}$ *Chapter 5: Ordering information* *Table 79: RAM options*: Updated PRAMC_2 start address *Figure 51: Ordering information scheme*: Removed reference to KGD.

Table 81. Document revision history (continued)

Date	Revision	Changes
04-June-2019	5	Cover page: minor format changes. *Chapter 2: Package pinouts and signal descriptions*: – *2.: Pin descriptions*: removed LVDS pins. *Chapter 3: Electrical characteristics*: Minor format changes. *Section 3.2: Absolute maximum ratings*: minor format changes. – *Table 4: Absolute maximum ratings*: added cross reference to footnote 3 to all V_{DD_HV*} and V_{IN}. *Section 3.3: Operating conditions* *Table 5: Operating conditions*: – T_J: for Max value = 165, changed to $T_{J\_140\ Grade}$ and updated Classification tag and Conditions. – T_J: for Max value = 150, changed to $T_{J\_125\ Grade}$ and updated Conditions. – T_A: for Max value = 125, changed to $T_{A\_125\ Grade}$. – Added row with $T_{A\_140\ Grade}$. *Section 3.4: Electrostatic discharge (ESD)*: minor format changes. *Section 3.7: Device consumption* – *Table 9: Device consumption*: updated table footnote 4 and moved footnote 1 to Value column. *Section 3.9: Reset pad (PORST, ESR0) electrical characteristics* – *Figure 5: Startup Reset requirements*: deleted V_{DDMIN}. *Section 3.10: PLLs* *Table 20: PLL0 electrical characteristics*: – The maximum value of $f_{PLL0PHI0}$ is changed from “400” to “FSYS” with a footnote. – Changed Condition from T to D for $\lvert\Delta_{PLL0PHI1SPJ}\rvert$, $\Delta_{PLL0LTJ}$ and I_{PLL0}. *Section 3.11: Oscillators* – *Table 22: External 40 MHz oscillator electrical specifications*: table footnote 1 updated: “DCF clients XOSC_LF_EN and XOSC_EN_40MHZ” changed by “XOSC_FREQ_SEL”. – *Table 23: Internal RC oscillator electrical specifications*: updated Max value for I_{FIRC}. *Section 3.12: ADC system*: – Editorial and formatting changes. – *Figure 8: Input equivalent circuit (Fast SARn and SARB channels)*: added parameter “C_{EXT}: external capacitance” and component to scheme. – *Table 24: ADC pin specification*: added row for symbol “C_{EXT} / SR”. *Section 3.12.2: SAR ADC 12 bit electrical specification*: – Minor format and editorial changes. – *Table 25: SARn ADC electrical specification*: created rows with T_j = 150°C and 165°C for $I_{ADCREFH}$, $I_{ADCREFL}$ and I_{ADV_S}. *Section 3.12.3: SAR ADC 10 bit electrical specification*: – Minor format changes. – *Table 26: ADC-Comparator electrical specification*: created rows with T_j = 150°C and 165°C or $I_{ADCREFH}$, $I_{ADCREFL}$ and I_{ADV_S}.

Table 81. Document revision history (continued)

Date	Revision	Changes
04-June-2019	5 (Cont')	*Section 3.12.4: S/D ADC electrical specification*: – Minor format and editorial changes. – Added note. – *Table 27: SDn ADC electrical specification*: Updated Max value before calibration for V_{OFFSET}, IBIAS, I_{ADV_D}. Updated footnote "S/D ADC is functional...". Added footnote "The absolute value..." for $\|\delta_{GAIN}\|$. Added one line with $T_j < 165°C$ for $\|\delta_{GAIN}\|$ and ΣI_{ADR_D}. Updated Min value for V_{cmrr}. *Section 3.12.5: SD ADC filter modes* – Updated paragraph "In Bypass FIR mode...". – Removed *Table 30: Digital output codes in full scale Bypass FIR mode*. – Added *Table 29: Digital output codes in full scale*. *Section 3.14: LFAST pad electrical characteristics* – *Table 31: LVDS pad startup and receiver electrical characteristics,*: Updated footnote #12 starting with "Value valid for LFAST mode..." with new sentence containing DSPI mode related data. Removed the last sentence of Note "Total internal capacitance...". *Section 3.16: Power management* – *Table 38: External components integration*: Added unit to Max value for C_{s2} and C_{s1_A}. Updated Conditions for C_{BV}. – *Table 41: SMPS Regulator specifications*: Changed condition for IDD_{SMPS}. – *Table 42: Voltage monitor electrical characteristics*: added footnote "Even if LVD/HVD ...". *Section 3.17: Flash memory* – *Table 43: Wait State configuration*: changed the minimum frequency from 40 to 55 MHz for APC=001. *Section 3.18: AC Specifications* – *Table 47: Nexus debug port timing*: Updated Min values for t_{TCYC} Absolute minimum TCK cycle time. Updated Max value on line 15. – *Figure 20: Nexus output timing*: deleted this figure. – *Section 3.18.3.7: RMII transmit signal timing (TXD[1:0], TX_EN)*: added Note "RMII transmit ... as 1ns". *Chapter 4: Package information* Minor format changes. *Section 4.1: eLQFP176 package information*: updated section according latest POA. – *Figure 52: FPBGA292 package outline*: Minor format changes. *Section 4.3: Package thermal characteristics*: – Minor formatting changes. – *Table 77: Thermal characteristics for 176 exposed pad LQFP package*: updated values for $R_{\theta JA}$, $R_{\theta JCtop}$, $R_{\theta JMA}$ and $R_{\theta JB}$.

Table 81. Document revision history (continued)

Date	Revision	Changes
04-June-2019	5 (Cont')	– *Section 4.3.2: FPBGA292*: updated package name in the section title. – *Table 78: Thermal characteristics for 292-pin FPBGA*: updated values for $R_{\theta JA}$and $R_{\theta JB}$ symbols. *Chapter 5: Ordering information* – *Figure 53: Ordering information scheme*: changed Reserved code from A to B.
06-Dec-2021	6	*Table 20: PLL0 electrical characteristics*: – Changed the value in column C for $\lvert\Delta_{PLL0PHI1SPJ}\rvert$ from D to T. – Updated Max value for $f_{PLL0PHI0}$ symbol and removed the footnote. *Table 21: PLL1 electrical characteristics*: Changed the value in column C for I_{PLL1} from T to D. *Table 24: ADC pin specification*: Updated unit for Symbol R_{SAFEPD}. *Section 3.12.1: ADC input description*: Updated the section. *Section 3.12.5: SD ADC filter modes*: Updated Device Number in the paragraph. *Table 38: External components integration*: – Updated table, notes content and numbering – Updated Min value for R_E – Updated Typ value for C_{LVN} – Added note 2 for C_{FLA} – Added note 6 for C_{ADC} *Table 42: Voltage monitor electrical characteristics*: Updated table footnote *1.* *Figure 26: DSPI CMOS master mode — classic timing, CPHA = 1*: Updated figure. *Figure 53: Ordering information scheme*: Updated code description for 4 in N Core.

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