STE70N60DM2

N-channel 600 V, 0.037 Ω typ., 70 A MDmesh™ DM2 Power MOSFET in a ISOTOP™ package

Datasheet - target specification

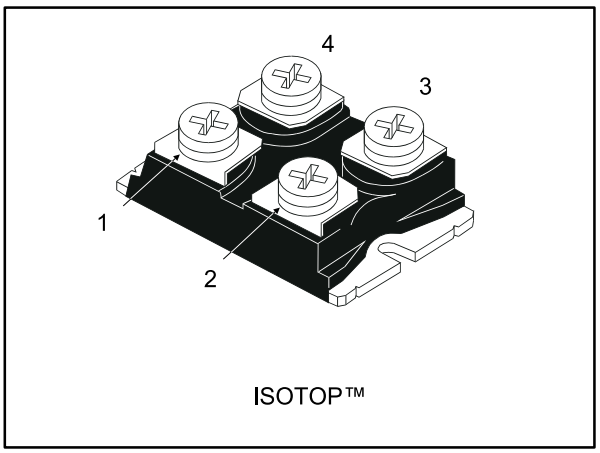
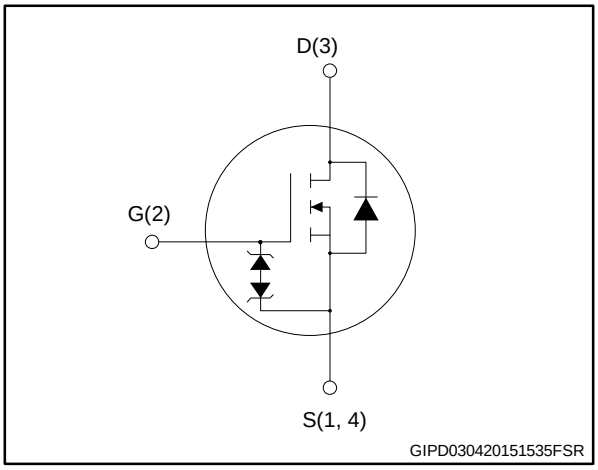


Figure 1: Internal schematic diagram



Features

Order code	V_{DS} @T_{jmax}	$R_{DS(on)}$ max	I_D
STE70N60DM2	650 V	0.042 Ω	70 A

- Fast-recovery body diode
- Extremely low gate charge and input capacitance
- Low on-resistance $R_{DS(on)}$
- 100% avalanche tested
- Extremely high dv/dt and avalanche capabilities
- Zener-protected

Applications

- Switching applications

Description

This high voltage N-channel Power MOSFET is part of the MDmesh DM2 fast recovery diode series. It offers very low recovery charge and time (Q_{rr}, t_{rr}) combined with low $R_{DS(on)}$, rendering it suitable for the most demanding high efficiency converters and ideal for bridge topologies and ZVS phase-shift converters.

Table 1: Device summary

Order code	Marking	Packages	Packaging
STE70N60DM2	70N60DM2	ISOTOP	Tube

Contents

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate- source voltage	± 25	V
I_D	Drain current (continuous) at T_C = 25 °C	70	A
I_D	Drain current (continuous) at T_C = 100 °C	44	A
I_{DM} (1)	Drain current (pulsed)	280	A
P_{TOT}	Total dissipation at T_C = 25 °C	494	W
I_{AR}	Max current during repetitive or single pulse avalanche (pulse width limited by T_{JMAX})	10	A
E_{AS}	Single pulse avalanche energy (starting T_j = 25°C, I_D = I_{AR}, V_{DD} = 50V)	1500	mJ
dv/dt (2)	Peak diode recovery voltage slope	40	V/ns
dv/dt (3)	MOSFET dv/dt ruggedness	50	V/ns
V_{ISO}	Isolation withstand voltage applied between each pin and heatsink plate (AC voltage, t = 60 s)	2500	V
T_{stg}	Storage temperature	- 55 to 150	°C
T_j	Max. operating junction temperature	150	°C

Notes:

(1)Pulse width limited by safe operating area.

(2)I_{SD} ≤ 68 A, di/dt = 400 A/µs, V_{DD} = 400 V, $V_{DS\ (peak)}$ < $V_{(BR)DSS}$.

(3)V_{DS} ≤ 480 V

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case max	0.253	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient max	30	°C/W

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 4: On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0	600			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 600 V			10	µA
		V_{DS} = 600 V, T_C=125 °C			100	µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 25 V			±5	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on- resistance	V_{GS} = 10 V, I_D = 34 A		0.037	0.042	Ω

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0	-	5500	-	pF
C_{oss}	Output capacitance		-	250	-	pF
C_{rss}	Reverse transfer capacitance		-	3	-	pF
$C_{oss.eq}$(1)	Equivalent output capacitance	V_{GS} = 0, V_{DS} = 0 to 480 V	-	430	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz open drain	-	2	-	Ω
Q_g	Total gate charge	V_{DD} = 480 V, I_D = 68 A, V_{GS} = 10 V See *Figure 3: "Gate charge test circuit"*	-	120	-	nC
Q_{gs}	Gate-source charge		-	25	-	nC
Q_{gd}	Gate-drain charge		-	60	-	nC

Notes:

(1)$C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 300 V, I_D = 34 A, R_G = 4.7 Ω, V_{GS} = 10 V See *Figure 2: "Switching times test circuit for resistive load"*	-	17	-	ns
t_r	Rise time		-	16	-	ns
$t_{d(off)}$	Turn-off delay time		-	86	-	ns
t_f	Fall time		-	10.5	-	ns

Table 7: Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		70	A
I_{SDM}(1)	Source-drain current (pulsed)		-		280	A
V_{SD}(2)	Forward on voltage	I_{SD} = 70 A, V_{GS} = 0	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 68 A, di/dt = 100 A/µs V_{DD} = 100 V See *Figure 4: "Test circuit for inductive load switching and diode recovery times"*	-	145		ns
Q_{rr}	Reverse recovery charge		-	0.76		µC
I_{RRM}	Reverse recovery current		-	10.5		A
t_{rr}	Reverse recovery time	I_{SD} = 68 A, di/dt = 100 A/µs V_{DD} = 100 V, T_j = 150 °C See *Figure 4: "Test circuit for inductive load switching and diode recovery times"*	-	250		ns
Q_{rr}	Reverse recovery charge		-	2.6		µC
I_{RRM}	Reverse recovery current		-	21		A

Notes:

(1)Pulse width limited by safe operating area.

(2)Pulsed: pulse duration = 300 µs, duty cycle 1.5%

3 Test circuits

Figure 2: Switching times test circuit for resistive load

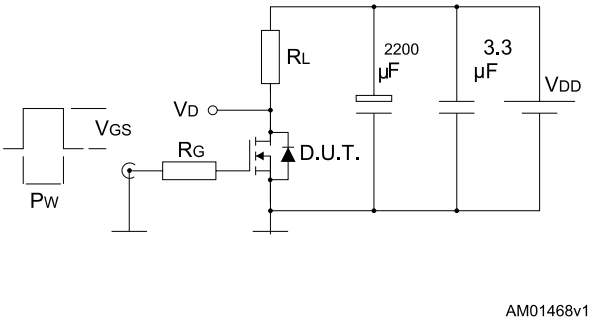


Figure 3: Gate charge test circuit

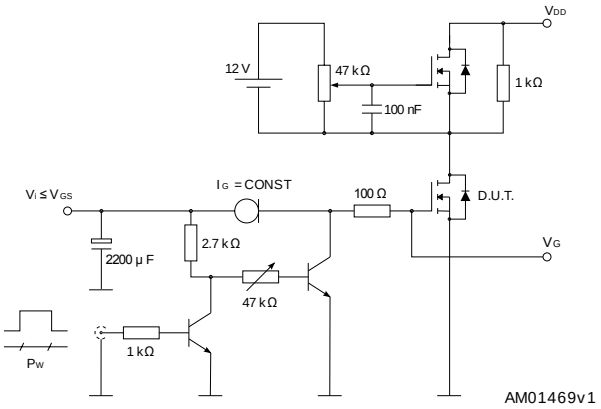


Figure 4: Test circuit for inductive load switching and diode recovery times

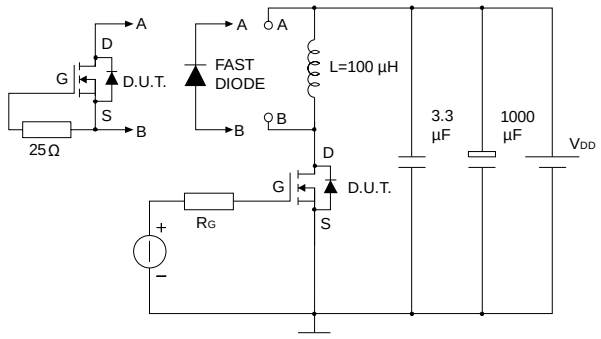


Figure 5: Unclamped inductive load test circuit

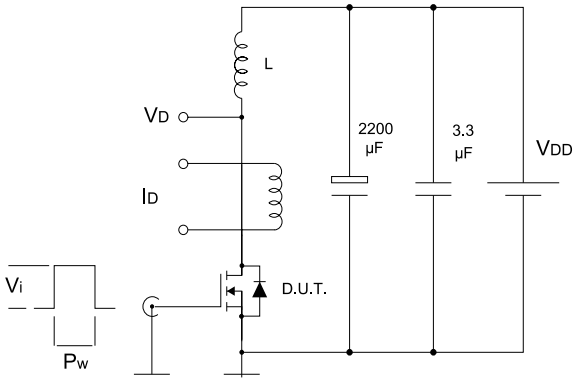


Figure 6: Unclamped inductive waveform

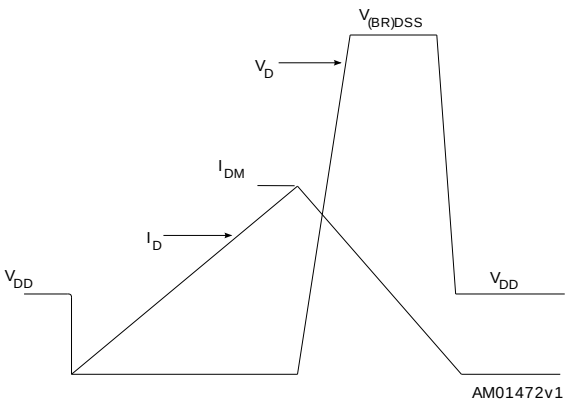
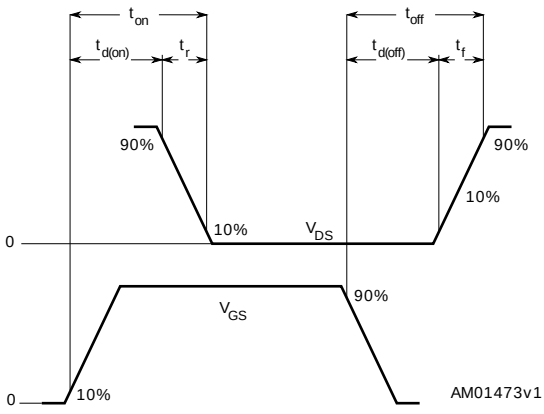


Figure 7: Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

4.1 ISOTOP package information

Figure 8: ISOTOP outline

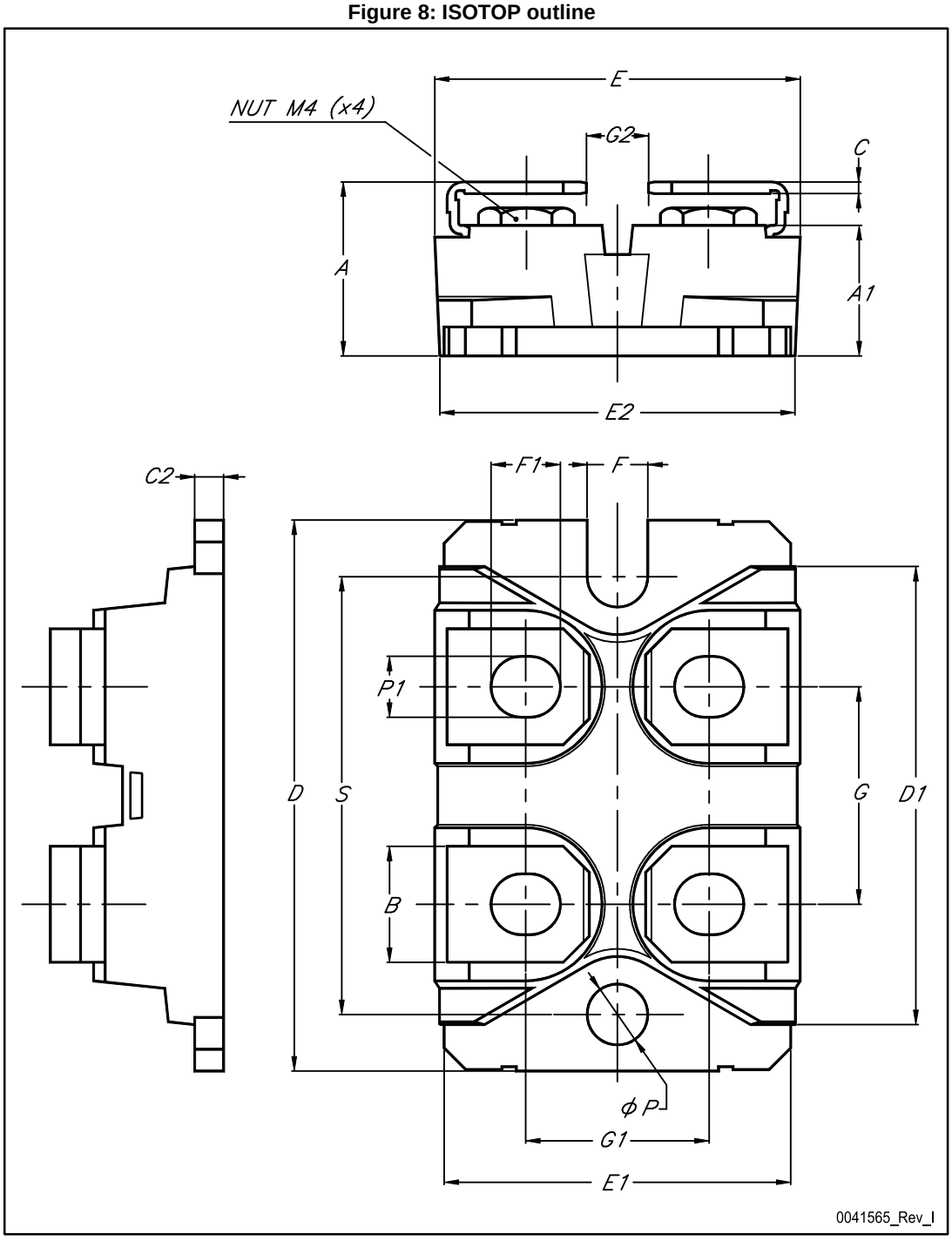


Table 8: ISOTOP mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	11.80		12.20
A1	8.90		9.10
B	7.80		8.20
C	0.75		0.85
C2	1.95		2.05
D	37.80		38.20
D1	31.50		31.70
E	25.15		25.50
E1	23.85		24.15
E2		24.80	
G	14.90		15.10
G1	12.60		12.80
G2	3.50		4.30
F	4.10		4.30
F1	4.60		5
ØP	4		4.30
P1	4		4.40
S	30.10		30.30

5 Revision history

Table 9: Document revision history

Date	Revision	Changes
03-Apr-2015	1	Initial release.

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