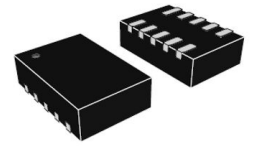
STEF512SRDB

Datasheet

Dual eFuse for 5 V and 12 V rails



DFN10 (2 x 3 mm)

Maturity status link
STEF512SRDB

Features

- 5 V and 12 V channels into one chip
- 25 V absolute maximum input voltage
- Precise output overvoltage clamp
- Fixed overcurrent protection trip points
- Fast reverse current protection on 5 V channel
- Thermal protection
- Latch-off thermal protection
- Input undervoltage lockout
- Adjustable output voltage slew rate for each channel by external capacitors
- Integrated 40 mΩ power MOSFETs
- 100 ms safety start-up delay
- SAS disable and enable pins
- 5 V embedded LDO
- - 3 V transient protection
- DFN10 (2 x 3 mm) package

Applications

- HDD and SSD
- Hard disk array and NAS
- Hot-swap, hot-plug protection

Description

The STEF512SRDB is an integrated dual electronic fuse, designed to protect circuitry on the output from overcurrent and overvoltage events, in those applications requiring hot-swap operation and in-rush current control.

The device embeds two electronic fuses, one for the 5 V rail and one for the 12 V rail.

Thanks to the very low ON-resistance of the integrated power MOSFETs, the voltage drop from the main supply to the load is very low during normal operation. The 5 V channel provides a reverse blocking feature, preventing current flow to the input in case of brownout or shutdown.

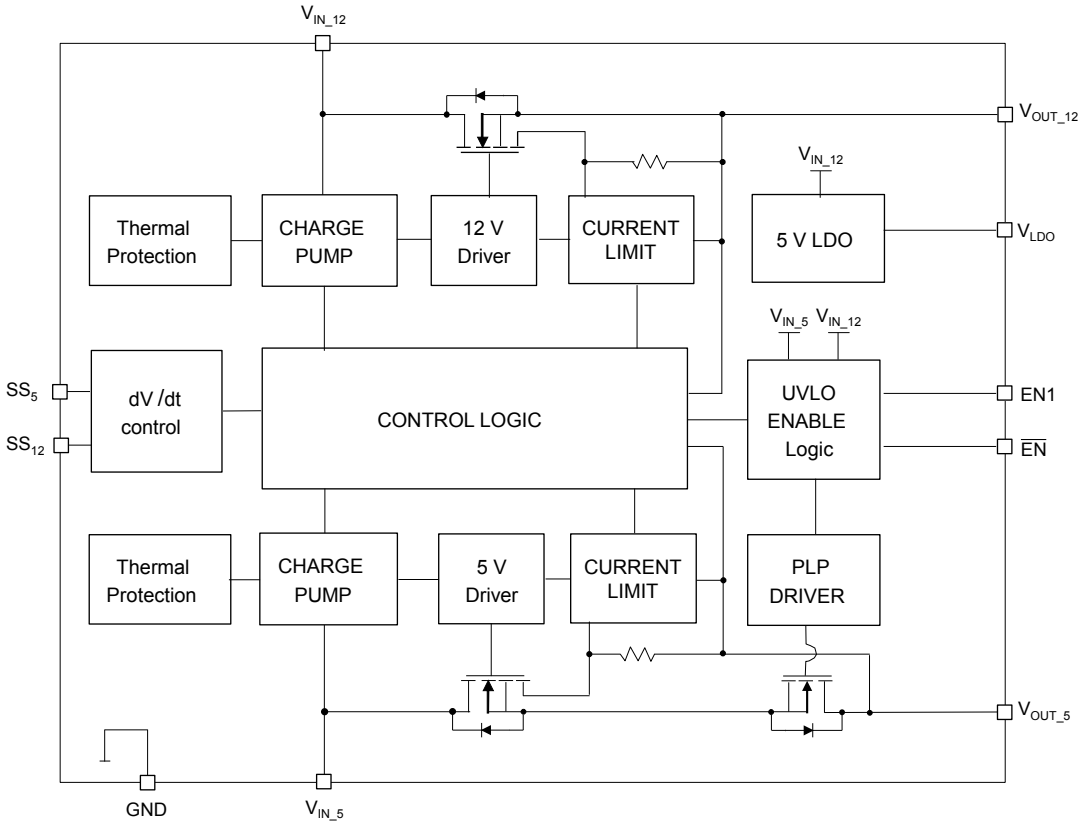
The start-up time of each eFuse can be adjusted by the user, via two small soft-start capacitors, connected to the relevant pins. In this way the in-rush current at startup can be kept under control. The maximum load current is precisely limited, by utilizing a sense FET topology, to factory-defined values.

The device also provides precise overvoltage clamp for each channel, preventing the load being damaged from power supply failures, and undervoltage lockout (UVLO), assuring that the input voltage is above the minimum operating threshold, before the power device is turned on.

When an overload condition occurs, the STEF512SRDB limits the output current to the predefined safe value. If the anomalous overload condition persists, the device goes into thermal shutdown, the internal switch is open and the load is disconnected from the power supply. 5 V fixed LDO is available to supply external load up to 10 mA.

1 Diagram

Figure 1. Block diagram



2 Pin configuration

Figure 2. **Pin connection (top view)**

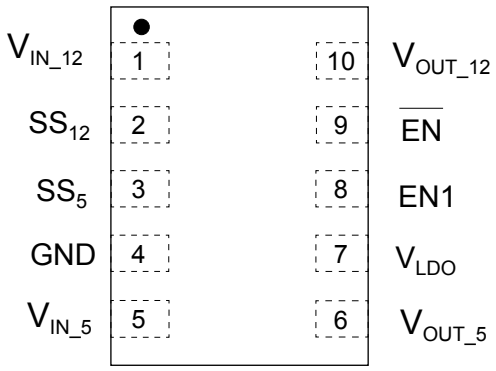


Table 1. **Pin description**

Pin n°	Symbol	Function
1	V_{IN_12}	12 V rail supply voltage
2	SS_{12}	Soft-start adjustment pin for the 12 V rail. A capacitor must be connected between this pin and GND to program the output voltage slew rate. Do not leave floating
3	SS_5	Soft-start adjustment pin for the 5 V rail. A capacitor must be connected between this pin and GND to program the output voltage slew rate. Do not leave floating
4	GND	Ground
5	V_{IN_5}	5 V rail supply voltage
6	V_{OUT_5}	5 V rail output voltage
7	V_{LDO}	5 V embedded LDO, bypass to GND with a 1 µF ceramic
8	EN1	Auxiliary enable pin, see Section 6.3. This pin is internally pulled up to 3.3 V via 3.3 MΩ resistor after both input voltages exceed the UVLO threshold
9	$\overline{EN}$	SAS disable input: set this pin logic-low to turn on the device, high to turn off the device. This pin is internally pulled down to GND via 3.3 MΩ resistor
10	V_{OUT_12}	12 V rail output voltage

3 Typical application

Figure 3. **Typical application circuit**

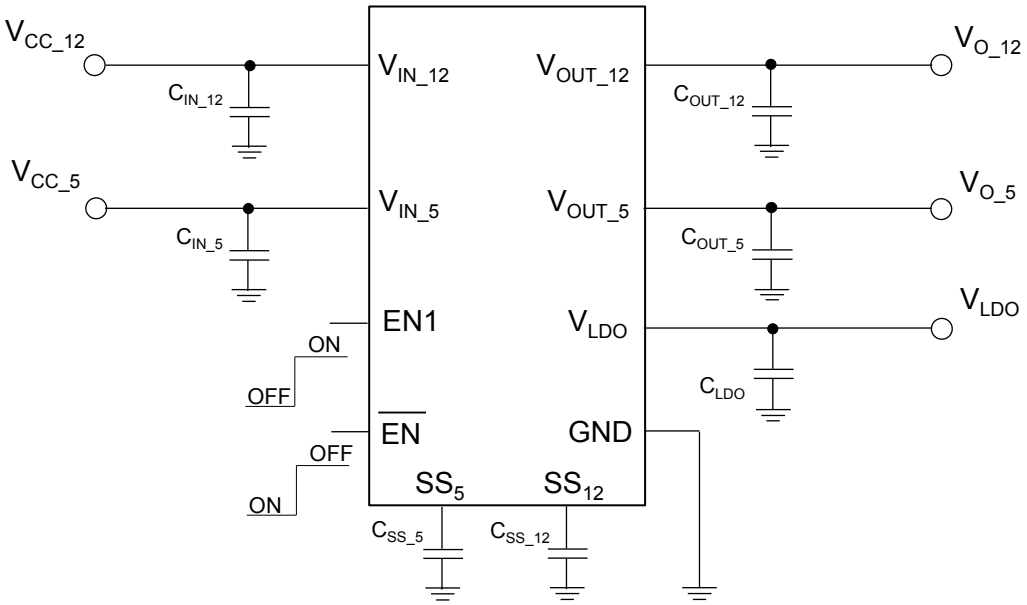


Table 2. **Recommended application components**

Symbol	Description	Min.	Typ.	Max.	Unit
C_{IN_12}	Input capacitor 12 V rail (1)	0	1		µF
C_{IN_5}	Input capacitor 5 V rail (1)	0	1		µF
C_{OUT_12}	Output capacitor 12 V rail	10	47		µF
C_{OUT_5}	Output capacitor 5 V rail	10	47		µF
C_{SS_5}	Soft start capacitor 5 V rail	10	100	1000	nF
C_{SS_12}	Soft start capacitor 12 V rail	10	100	1000	nF
C_{LDO}	LDO bypass capacitor	0.47	1	10	µF

1. *This value must be considered with DC-bias derating characteristics of capacitance used. In case of long wires cable application see Section 6.7.*

4 Maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{IN_5}	5 V supply voltage	-0.3 to 25	V
	Negative transient tolerance (< 1 ms)	-3	V
V_{IN_12}	12 V supply voltage	-0.3 to 25	V
	Negative transient tolerance (< 1 ms)	-3	V
V_{OUT_5}	5 V output voltage	-0.3 to 7	V
V_{OUT_12}	12 V output voltage	-0.3 to V_{IN} + 0.3	V
V_{LDO}	LDO output voltage	-0.3 to 7	V
I_{LDO}	LDO output current	50	mA
I_{OUT_5}	Continuous output current (1) 5 V channel	3	A
I_{OUT_12}	Continuous output current (1) 12 V channel	3.6	A
$V_{\overline{EN}}$, V_{EN1}	Enable pins	-0.3 to 7	V
SS_x	Soft-start pin voltage	-0.3 to 7	V
P_D	Continuous power dissipation	Internal limited	
$T_{J\text{-}OP}$	Operating junction temperature range	-40 to 125	°C
$T_{J\text{-}MAX}$	Maximum junction temperature (internal limited)	150	°C
T_{STG}	Storage temperature range	-55 to 150	°C

1. *This value can be applied for guaranteed lifetime. Higher value can be applied for a time lower than 200 ms. The maximum allowable power dissipation is a function of the maximum junction temperature $T_{J\text{-}MAX}$, the junction-to-ambient thermal resistance R_{thJA}, and the ambient temperature T_A. It can be estimated by: $P_{D(MAX)} = (T_{J(MAX)} - T_A) / R_{thJA}$. Exceeding the maximum allowable power dissipation produces overheating that may cause thermal shutdown.*

Note: Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. All values are referred to GND.

Table 4. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal resistance junction-ambient (1)	82	°C/W
R_{thJC}	Thermal resistance junction-case	12	°C/W

1. *Based on JESD51-7, 4-layer PCB.*

Table 5. ESD performance

Symbol	Parameter	Test conditions	Value	Unit
ESD	ESD protection voltage	HBM	2	kV
		CDM	500	V

5 Electrical characteristics

T_J = 25°C, V_{IN_5} = 5 V, V_{IN_12} = 12 V, $V_{\overline{EN}}$ = 0 V, V_{EN1} = 1.8 V, C_{IN} = 1 µF, C_{OUT} = 10 µF, C_{LDO} = 1 µF, C_{SS5} = C_{SS12} = 100 nF; unless otherwise specified.

Table 6. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
5 V rail						
V_{IN_5}	Operating input voltage		4.5		18	V
V_{Clamp_5}	Average output clamping voltage	V_{IN_5} = 18 V	5.5	5.7	5.8	V
V_{UVLO_5}	Undervoltage lockout	Turn-on, V_{IN_5} rising	3.9	4	4.1	V
		Hysteresis		300		mV
R_{DSon_5}	On-resistance	T_J = 25°C, I_{OUT_5} = 500 mA		45		mΩ
		T_J = 125°C (1)			70	mΩ
I_{L_5}	Off-state leakage current	$V_{\overline{EN}}$ = 5 V, V_{OUT_5} = GND			1	µA
I_{PLP_5}	Power loss protection reverse leakage current	$V_{\overline{EN}}$ = 0 V, V_{OUT_5} = 5 V, V_{IN_5} < V_{UVLO_5} or EN1 = GND			1	µA
T_{PLP}	Power loss protection intervention time	$V_{\overline{EN}}$ = 0 V, V_{OUT_5} = 5 V, V_{IN_5} < V_{UVLO_5} or EN1 = GND (falling edge), I_{PLP_5} < 1 µA, (see Section 6.7)		300		ns
I_{TRIP_5}	Overcurrent trip point (2)			3		A
I_{HOLD_5}	Overload current limit	V_{OUT_5} > 2.5 V	2.35	2.5	2.85	A
I_{SHORT_5}	Short-circuit current	V_{OUT_5} < 2.5 V		1.55		A
$dV/dt_{\_5}$	Output voltage ramp time	From 10% to 90% of V_{OUT_5}	11	13	16	ms
12 V rail						
V_{IN_12}	Operating input voltage		10.5		18	V
V_{Clamp_12}	Average output clamping voltage	V_{IN_12} = 18 V	14.5	15	15.5	V
V_{UVLO_12}	Undervoltage lockout	Turn-on, V_{IN_12} rising	7.7	8.5	9.3	V
		Hysteresis		800		mV
R_{DSon_12}	On-resistance	T_J = 25°C, I_{OUT_12} = 500 mA		40		mΩ
		T_J = 125°C(1)			65	mΩ
I_{L_12}	Off-state leakage current	$V_{\overline{EN}}$ = 5 V, V_{OUT_12} = GND			3	µA
I_{TRIP_12}	Overcurrent trip point (2)			4.5		A
I_{HOLD_12}	Overload current limit	V_{OUT_12} > 7.5 V	2.95	3.1	3.25	A
I_{SHORT_12}	Short-circuit current	V_{OUT_12} < 7.5 V		1.6		A
$dV/dt_{\_12}$	Output voltage ramp time	From 10% to 90% of V_{OUT_12}	11	13	16	ms
5 V LDO						
V_{LDO}	V_{OUT} accuracy	I_{LDO} = 1 mA	- 3		3	%
I_{OUT}	Output current capability	Any ENx condition, V_{IN_5} and V_{IN_12} > V_{UVLO_X}	10			mA

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Line	Line regulation	V_{IN_12} from 10 to 15 V		10		mV
Load	Load regulation	I_{LDO} = 1 mA		25		mV
I_{SC}	Short-circuit protection		50			mA
T_{ON}	Start-up time	V_{LDO} from 10% to 90% V_{IN_5} and V_{IN_12} > V_{UVLO_X}		1		ms
Common features						
V_{IL}	Low level input voltage ($\overline{EN}$, EN1)				0.5	V
V_{IH}	High level input voltage ($\overline{EN}$, EN1)		1.4			V
V_{pull1}	EN1 pull-up voltage	EN1 floating		3.3		V
$R_{Pull-up}$	Pull-up resistor on EN1			3.3		MΩ
$R_{Pull-down}$	Pull-down resistor on $\overline{EN}$	$\overline{EN}$ = floating		3.3		MΩ
T_{DELAY}	Start-up output delay time	V_{IN_12} and V_{IN_5} > V_{UVLO_X}	80	100	120	ms
$I_{\overline{EN}}$	$\overline{EN}$ leakage	$V_{\overline{EN}}$ = 5 V		1.5		µA
I_Q	Quiescent current (GND)	Device operating, no Load		350	600	µA
		Off-state, $V_{\overline{EN}}$ = 5 V, including LDO and ENx currents		150		µA
Thermal protection						
T_{SD}	Shutdown temperature (3)			165		°C
	Hysteresis			20		°C

1. *Values across temperature range are guaranteed by design/correlation and tested in production only at ambient temperature.*
2. *Guaranteed by design, but not tested in production. Ramp-up time from 0 A to I_{TRIP} point 1 ms @ 5 V, 100 µs @ 12 V. Minimum I_{TRIP} point is always higher than I_{HOLD_min} +10%.*
3. *Guaranteed by design, but not tested in production.*

6 Functional description

The STEF512SRDB embeds a 5 V and a 12 V electronic fuse (eFuse). Each eFuse is an intelligent load switch, able to limit the voltage or the current during fault events, such as input overvoltage or output overload respectively.

For this purpose, it contains 2 digital control loops, one limiting the output voltage and one limiting the input current.

During normal operation the eFuse behaves as a low-resistance Power FET, therefore the output voltage follows the input one. In case of overvoltage or overcurrent event, the eFuse limits the V_{GS} of the internal FET, in order to clamp the output voltage or current respectively. During such events the die temperature increases due to the power dissipation and so, if the fault persists and the overtemperature threshold is overcome, the device goes into thermal shutdown, the internal FET is turned off and the load disconnected from the power supply.

Each eFuse provides factory-trimmed undervoltage lockout feature and user-adjustable output voltage linear rise time Δt [ms] (from 10% to 90% of V_{OUT}) to limit the in-rush current into the output capacitor during the start-up phase.

Given the desired time interval Δt, the capacitance to be added on the C_{ss_x} pin with nominal input voltage V_{IN_12} = 12 V, V_{IN_5} = 5 V can be calculated using the following theoretical formula.

$$\Delta t[ms] = C_{SS\_X}[nF] \times 0.13 \quad (1)$$

6.1 Undervoltage lockout

Undervoltage lockout circuit prevents each eFuse from turning on if the supply voltage is below the UVLO rising threshold. During operation, if the input voltage of one channel falls below (V_{UVLO_x} - V_{Hyst_x}), the outputs of both channels are turned off simultaneously and LDO output shuts down at the same time.

6.2 Start-up sequence and voltage clamp

The typical start-up sequence of the eFuse is described below and shown in Figure 4, Figure 5 and Figure 6:

- The power supply is connected to the V_{IN_x} pins and higher than the undervoltage lockout threshold
- The disable pin $\overline{EN}$ and the auxiliary EN1 pin are asserted according to Table 7. Enable pins truth table by the user to enable the device
- After a delay of 100 ms the eFuse starts ramping up the output voltage
- Each channel ramps up with a rate set by the relevant C_{SSx}
- If the input voltage continues rising, above the overvoltage threshold (V_{Clamp_x}), as a consequence of a failure in the power supply, the eFuse limits the output voltage to V_{Clamp_x}. The eFuse keeps operating in this state until it hits its overtemperature threshold and shuts down. Whenever the eFuse is in thermal shutdown, it does not restart automatically, see Section 6.2. The eFuse can be restarted manually by toggling the $\overline{EN}$ pin or EN1, or performing a power-up cycle, (this is effective as soon as the die temperature drops by at least the overtemperature hysteresis).

Figure 4. Typical start-up sequence with EN1 and $\overline{EN}$ in ON-state before input power supply connection

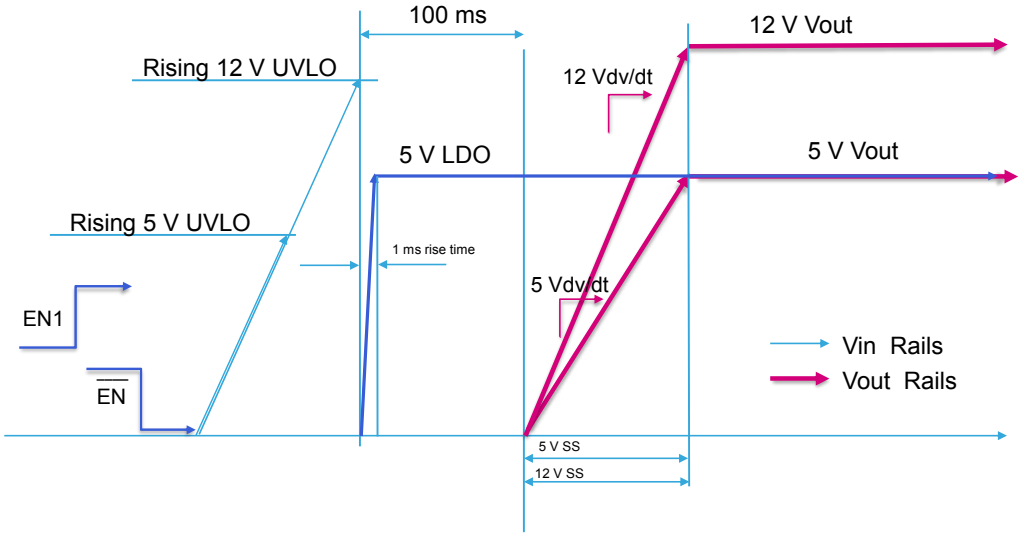


Figure 5. Typical start-up sequence with EN1 and/or $\overline{EN}$ in ON-state after time delay

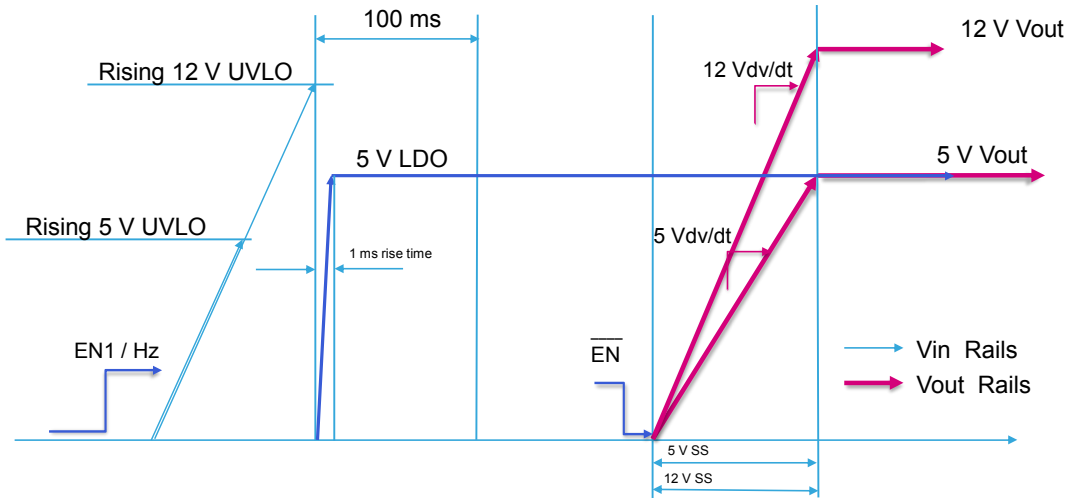


Figure 6. **Typical start-up sequence with EN1 or $\overline{EN}$ in ON-state during time delay**

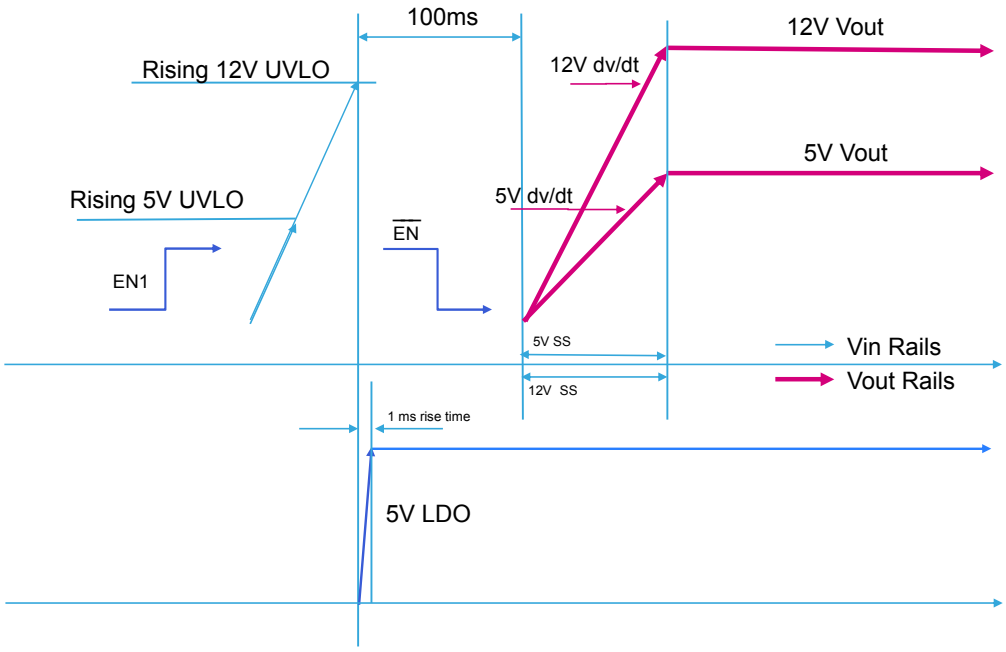
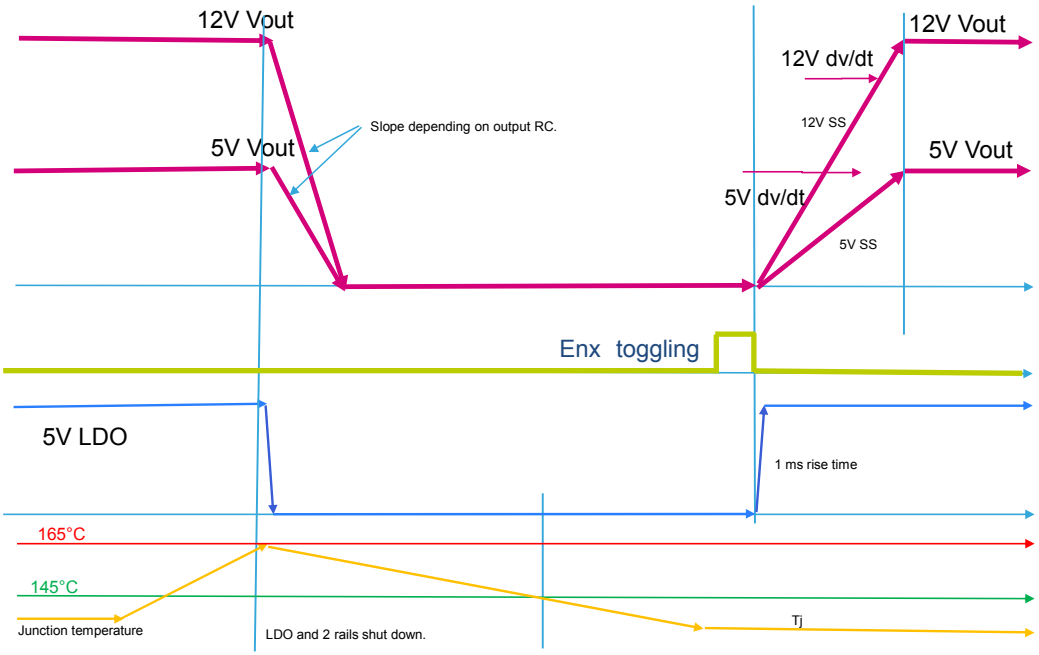


Figure 7. **LDO and output channels during thermal event**



6.3 Enable pins

The device provides an SAS-compliant chip disable pin $\overline{EN}$ and an auxiliary enable pin EN1.

The auxiliary enable pin can be used to implement customized start-up/shutdown sequences, in conjunction with other system companion chips (such as power combos in the HDD) and it is pulled up to the internal preregulated voltage (typ. 3.3 V), through 3.3 MΩ resistors, as soon as the input voltage of both channels surpasses the UVLO thresholds.

It is not recommended to use LDO output as external pull-up voltage of EN1 pin.

As a logic input it controls the eFuse ON/OFF status, together with the $\overline{EN}$ pin. If this function is not needed in the application, it can be left floating. The device ON/OFF behavior depends on the enable pins as described in the following truth table:

Table 7. Enable pins truth table

$\overline{EN}$	EN1	Device status
HZ/0	0	Off
HZ/0	HZ/1	On
1	0	Off
1	HZ/1	Off

According to the above table and the internal pull-up configuration, if both enable pins are left floating, the device is in the ON status.

6.4 Current limit function after startup

In case of overcurrent with moderate slew rate the soft control limits output current at the I_{HOLD} threshold and the gate of the power MOSFET is driven by constant current source/sink.

Instead, in case of fast overcurrent event or short-circuit event with output current reaching I_{TRIP} threshold the hard control shorts immediately the gate to source by a strong pull-down. See Figure 8, Figure 9 and Figure 10.

During current limitation phase the eFuse provides 2 levels of current limit protection according to output voltage level, see Figure 11 and Figure 12. If output voltage falls to 7.5 V for a 12 V channel (2.5 V for a 5 V channel) the current control loop changes the current limitation threshold from I_{HOLD} to I_{SHORT}.

Figure 8. Current control loop block diagram

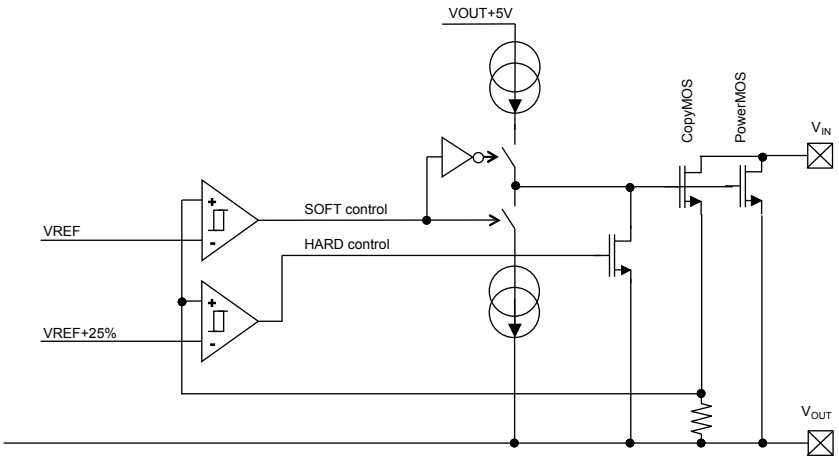


Figure 9. **Overcurrent protection in case of short-circuit event**

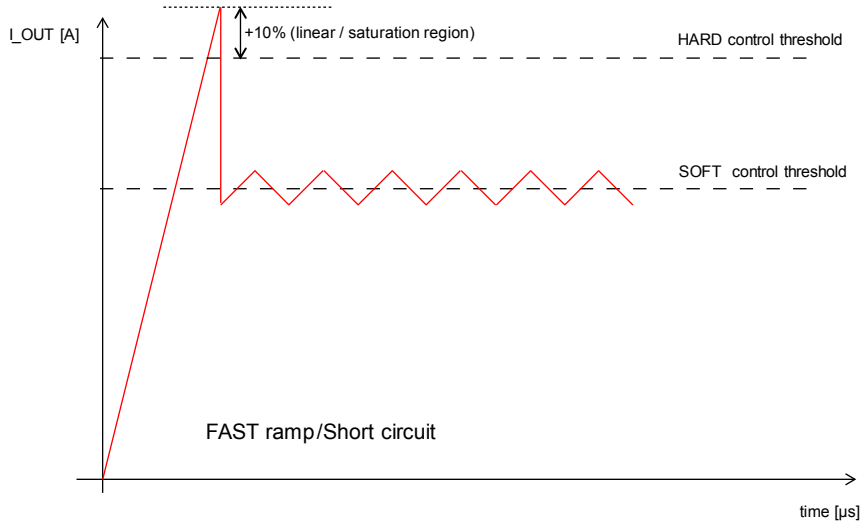


Figure 10. **Overcurrent protection in case of overload with slow slew rate**

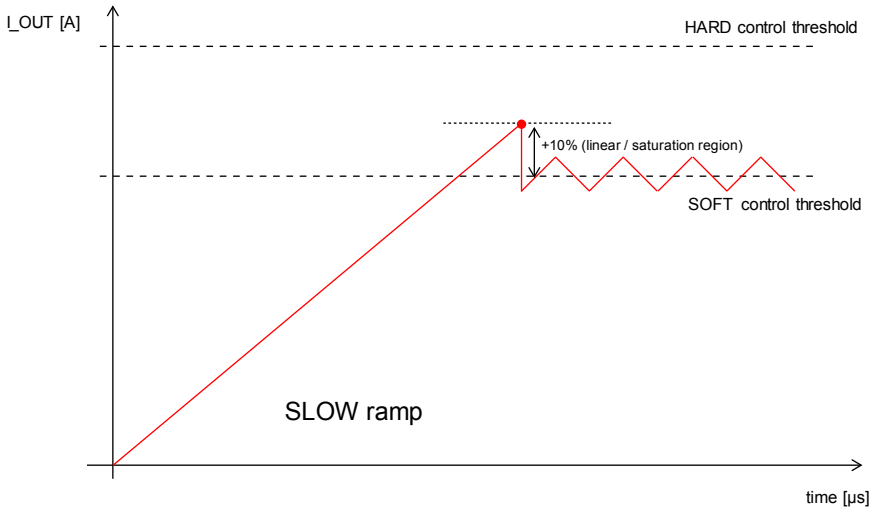


Figure 11. **Current limit function graph (5 V channel)**

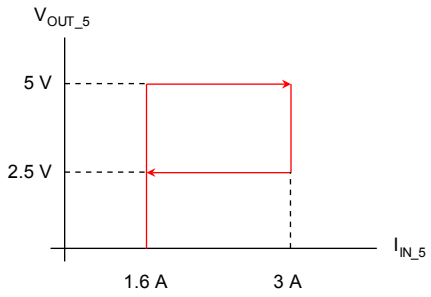
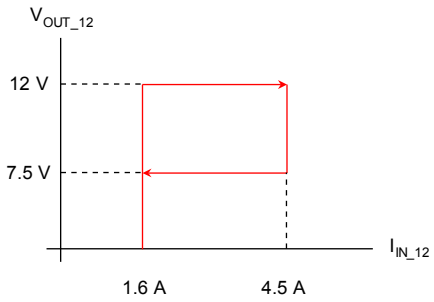


Figure 12. **Current limit function graph (12 V channel)**



6.5 Thermal shutdown

If the device temperature exceeds the thermal threshold, typically 165°C, the thermal shutdown circuitry turns the power MOSFET off, thus disconnecting the load. The device keeps the output channels and LDO output in OFF mode until the temperature goes below the hysteresis value and a toggling of the enable is performed or a power-on reset is applied.

The device is also equipped with a differential thermal protection that avoids damage in case of fast thermal gradients inside the chip. When the differential thermal protection is activated both the channel and the LDO are switched off. This protection works in auto-retry mode. The device restarts automatically when the thermal conditions go back into the normal operating region.

6.6 Reverse current blocking feature on the 5 V channel

The 5 V eFuse contains a second power transistor (M2) that is able to prevent significant current flowing back from the 5 V output into the 5 V input, in case of input short to ground, brownout or deep input voltage glitch. The simplified structure is shown in Figure 13.

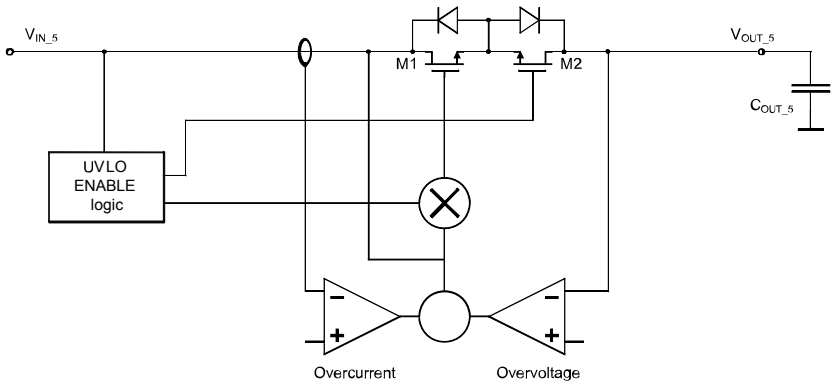
Reverse blocking MOSFET M2 is controlled by the UVLO circuit and EN1 signal.

It should be noted that when V_{IN_5} undervoltage is detected, the M2 is turned off immediately (asynchronously), however the main MOSFET M1 is kept ON for the next 10 µs due to the deglitch circuit.

If the input voltage recovers within the deglitch time, the eFuse is able to rapidly restore its normal operating state (warm restart). Otherwise, the eFuse shuts down completely.

As soon as the UVLO threshold has been reached again, the eFuse restarts with normal soft-start cycle.

Figure 13. **5 V reverse current protection block diagram**



6.7 External capacitors and application tips

Input and output capacitors are mandatory to reduce the transient effects of stray inductances which may be present on the input and output power paths. In fact, when the STEF512SRDB interrupts the current flow, input inductance generates a positive voltage spike on the input, and output inductance generates a negative voltage spike on the output. To reduce the effects of such transients, a C_{IN} capacitor of at least 1 µF (including derating effects) must be connected between the input pin and GND, and located as close as possible to the device.

For the same reason, a C_{OUT} capacitor of at least 10 µF must be connected at the output port.

When the device is connected to the power supplies by means of long wires, whose inductance is higher than 1 µH, the input capacitor should be increased.

It is suggested to provide for additional protections and methods for addressing these transients, such as:

- Minimizing inductance of the input and output tracks
- TVS diodes on the input to absorb inductive spikes placed as close as possible to input pins
- Schottky diode on the output to absorb negative spikes
- Combination of ceramic and electrolytic capacitors on the input and output.

7 Typical characteristics

The following plots refer to the typical application circuit with Vcc_12 = 12 V, Vcc_5 = 5 V, Iout_12 = 0 A, Iout_5 = 0 A, Iout_LDO = 0 A, unless otherwise noted, at T_A = 25°C.

Figure 14. Quiescent current vs. temperature (ON Mode)

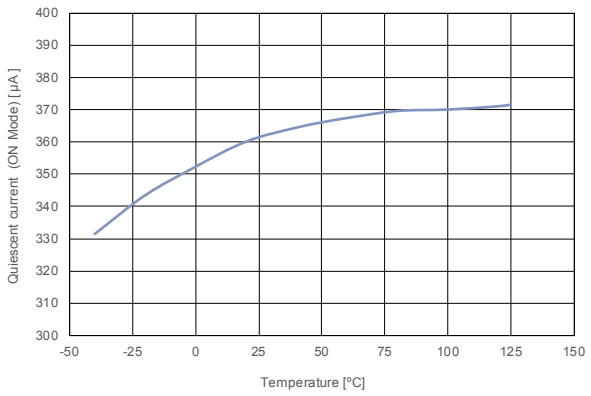


Figure 15. Quiescent current vs. temperature (OFF Mode)

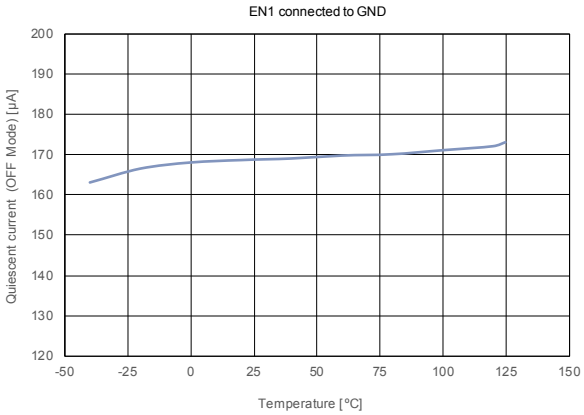


Figure 16. R_{DS_ON} 12 V vs. temperature

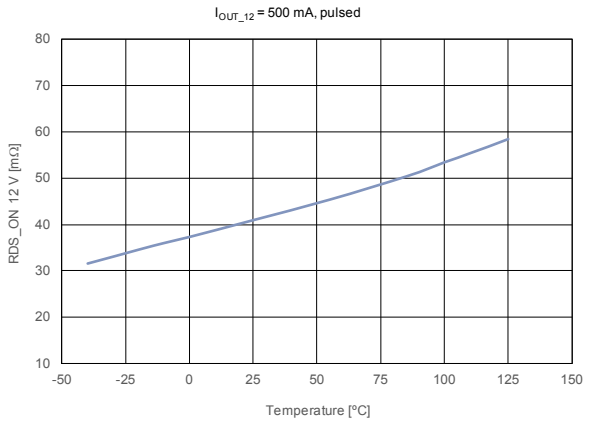


Figure 17. R_{DS_ON} 5 V vs. temperature

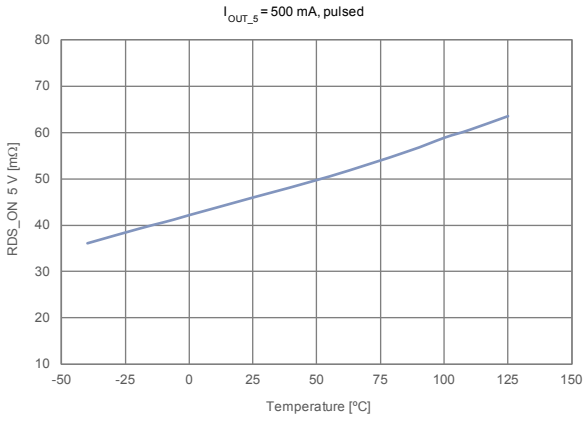


Figure 18. V_{CLAMP_5} vs. temperature

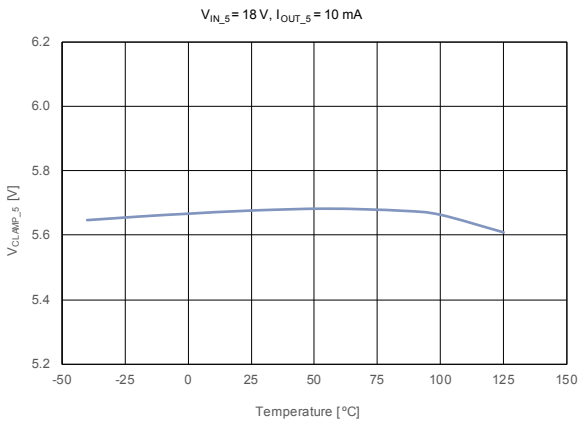


Figure 19. V_{CLAMP_12} vs. temperature

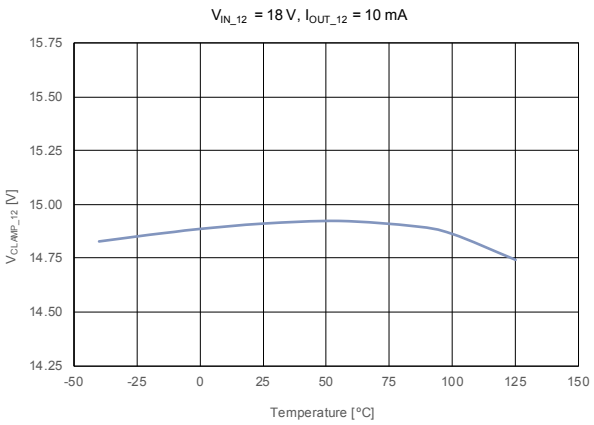


Figure 20. I_{HOLD_5} vs. temperature

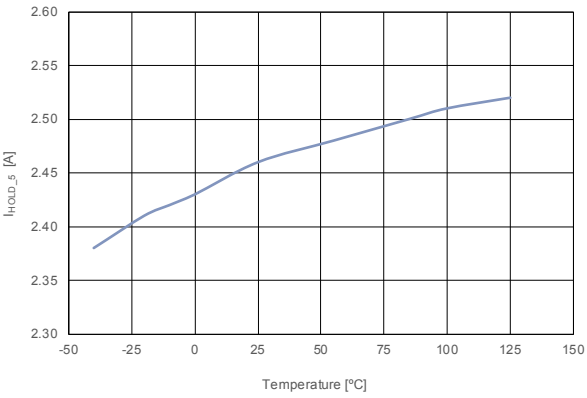


Figure 21. I_{HOLD_12} vs. temperature

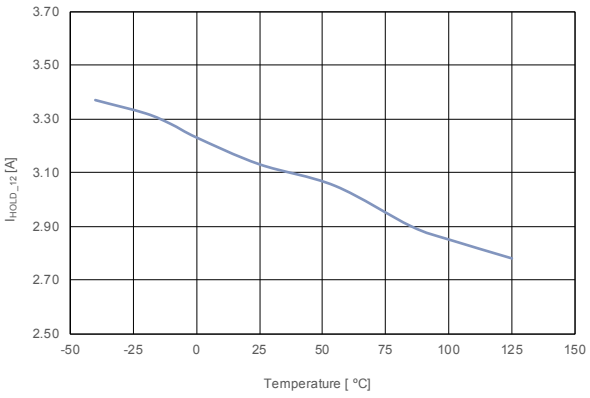


Figure 22. I_{SHORT_5} vs. temperature

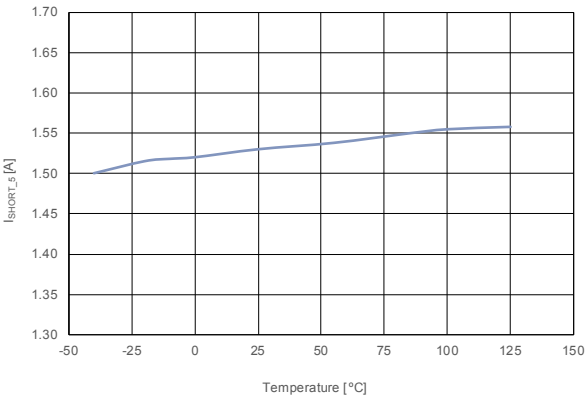


Figure 23. I_{SHORT_12} vs. temperature

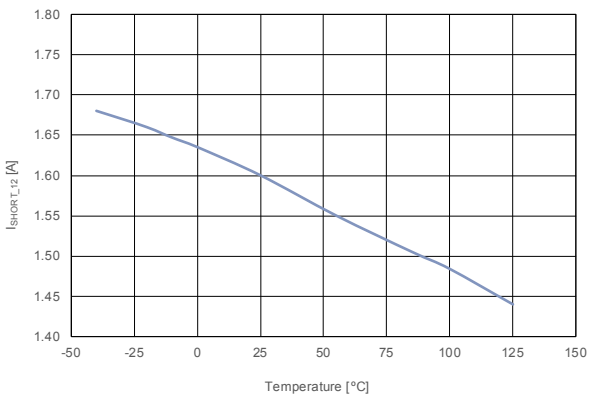


Figure 24. V_{UVLO_5} vs. temperature

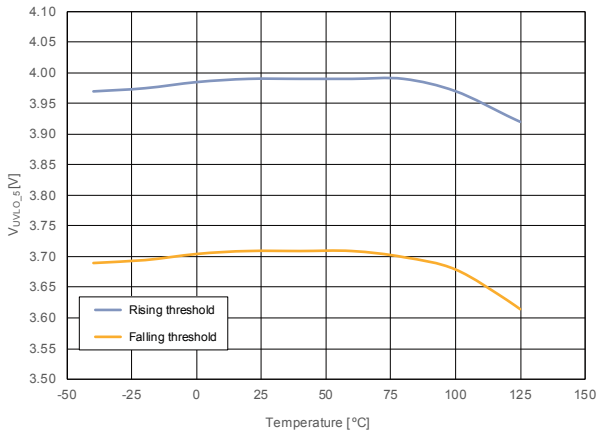


Figure 25. V_{UVLO_5} hysteresis vs. temperature

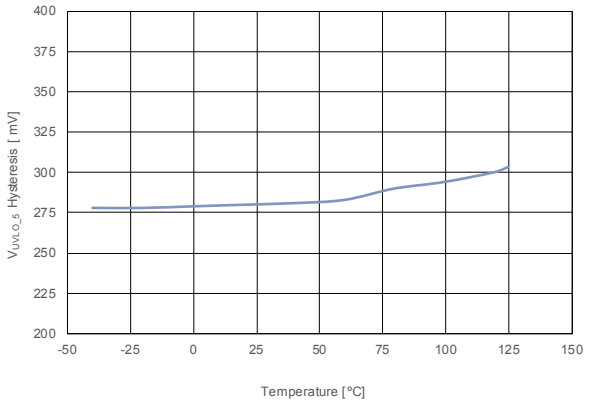


Figure 26. V_{UVLO_12} vs. temperature

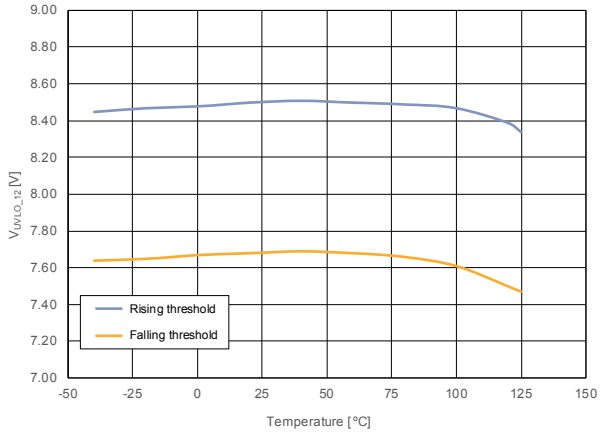


Figure 27. V_{UVLO_12} hysteresis vs. temperature

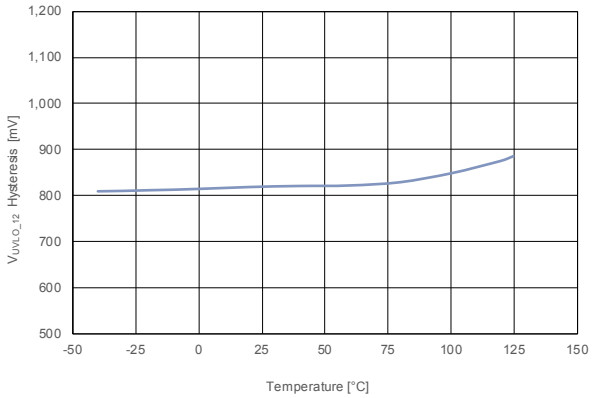


Figure 28. V_{LDO} vs. temperature

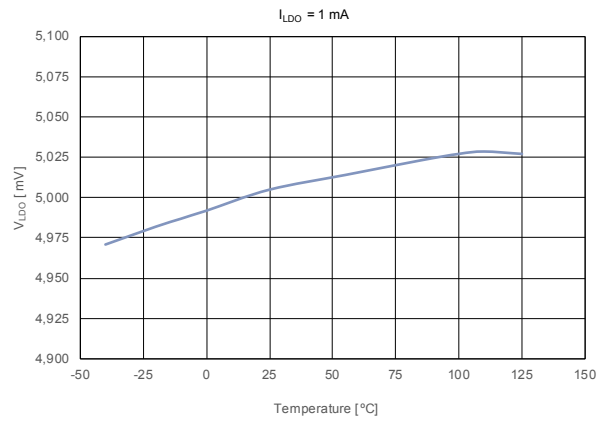


Figure 29. Soft-start time vs. temperature

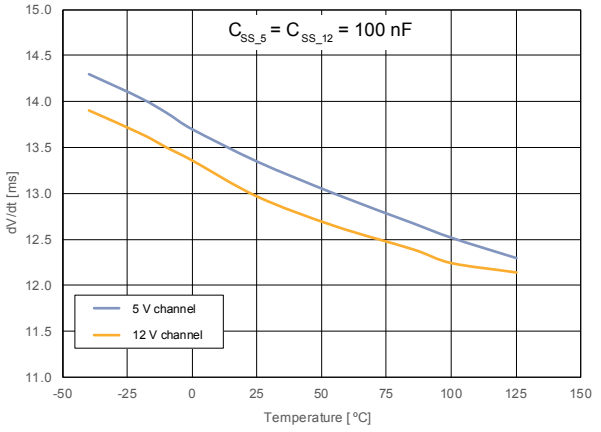
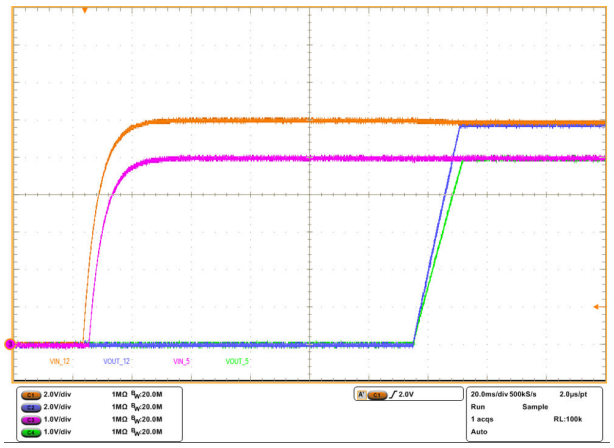
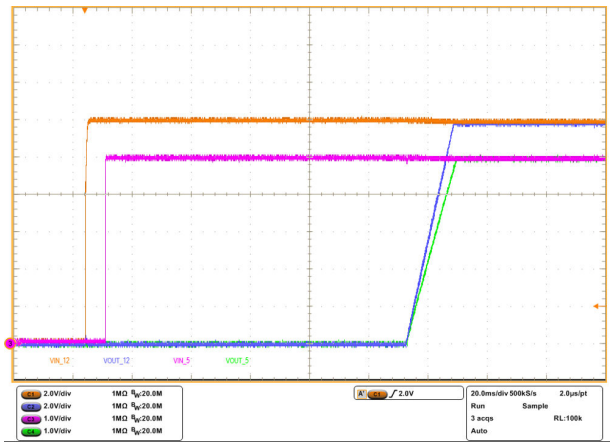


Figure 30. Startup via input voltage



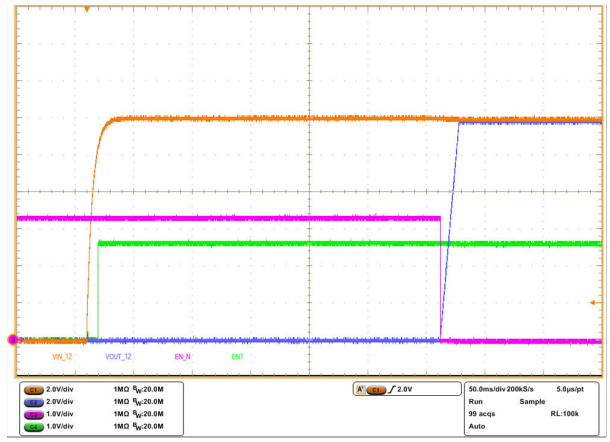
V_{IN_12} = from 0 V to 12 V, V_{IN_5} = from 0 V to 5 V, I_{OUT_12}= 0 mA, I_{OUT_5} = 0 mA

Figure 31. Startup via input voltage (Hot-plug)



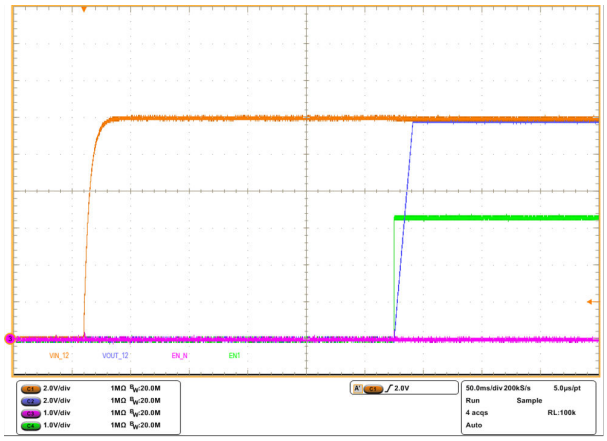
V_{IN_12} = from 0 V to 12 V, V_{IN_5} = from 0 V to 5 V, I_{OUT_12} = 0 mA, I_{OUT_5} = 0 mA

Figure 32. Startup via EN_N signal



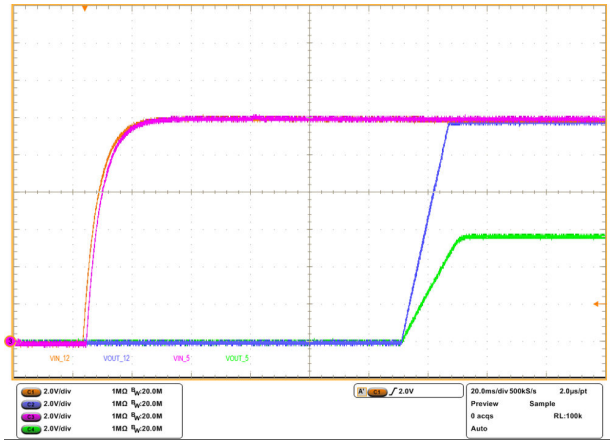
V_{IN_12}= from 0V to 12V, V_{IN_5}= from 0V to 5V, V_{EN_N}= from 3.3V to 0V, I_{OUT_12}= 0mA, I_{OUT_5}= 0mA

Figure 33. Startup via EN1 signal



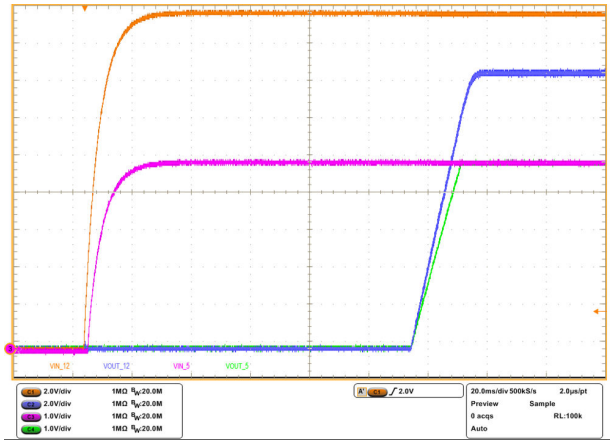
V_{IN_12}= from 0V to 12V, V_{IN_5}= from 0V to 5V, V_{EN1}= from 0V to floating, I_{OUT_12}= 0mA, I_{OUT_5}= 0mA

Figure 34. Startup into voltage clamp 5 V channel



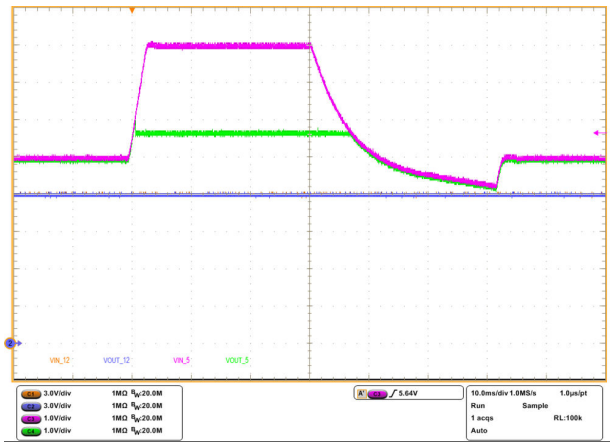
V_{IN_12}= from 0V to 12V, V_{IN_5}= from 0V to 12V, I_{OUT_12}= 0mA, I_{OUT_5}= 0mA

Figure 35. Startup into voltage clamp 12 V channel



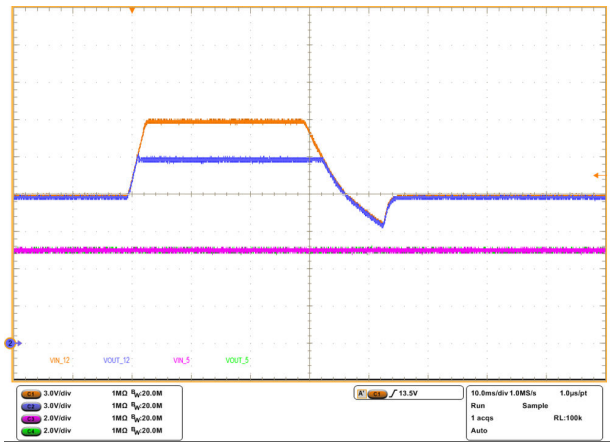
V_{IN_12}= from 0V to 18V, V_{IN_5}= from 0V to 5V, I_{OUT_12}= 0mA, I_{OUT_5}= 0mA

Figure 36. Voltage clamp during operation 5 V channel



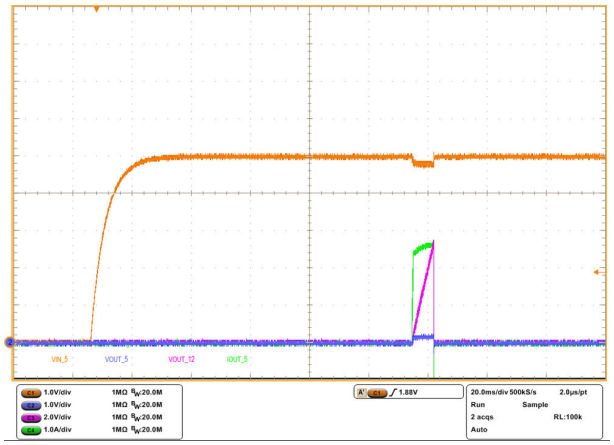
V_{IN_12}= 12V, V_{IN_5}= from 5V to 8V, I_{OUT_12}= 0mA, I_{OUT_5}= 400mA

Figure 37. Voltage clamp during operation 12 V channel



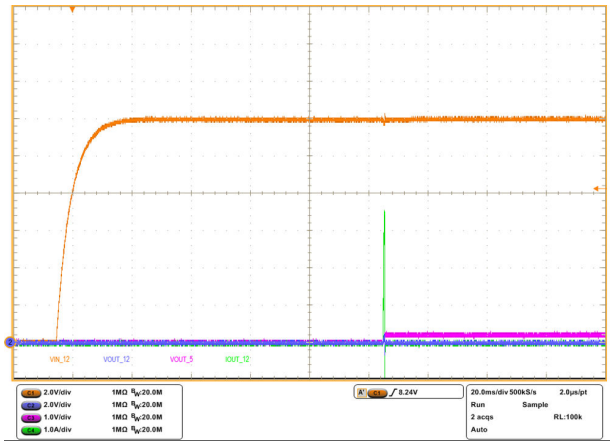
V_{IN_12}= from 12V to 18V, V_{IN_5}= 5V, I_{OUT_12}= 400mA, I_{OUT_5}= 0mA

Figure 38. Startup into output short-circuit 5 V channel



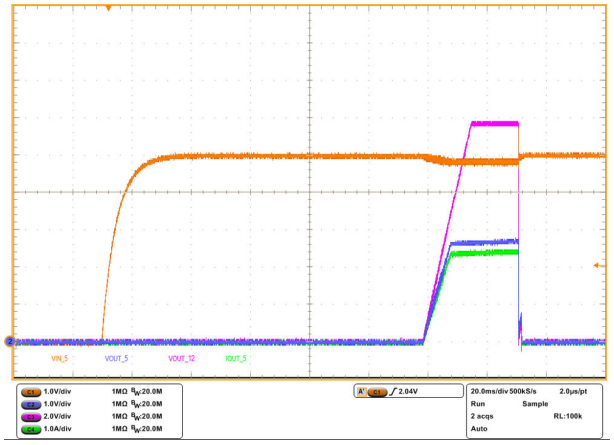
V_{IN_12}= from 0V to 12V, V_{IN_5}= from 0V to 5V, I_{OUT_12}= 0mA, V_{OUT_5}= shorted to GND

Figure 39. Startup into output short-circuit 12 V channel



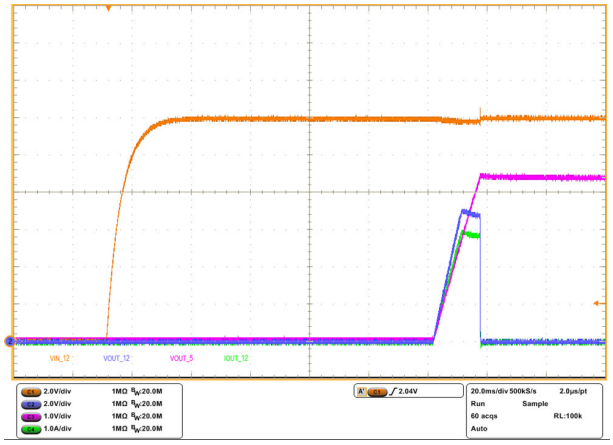
V_{IN_12} = from 0 V to 12 V, V_{IN_5} = from 0 V to 5 V, I_{OUT_5} = 0 mA, V_{OUT_12} = shorted to GND

Figure 40. Startup into overload 5 V channel



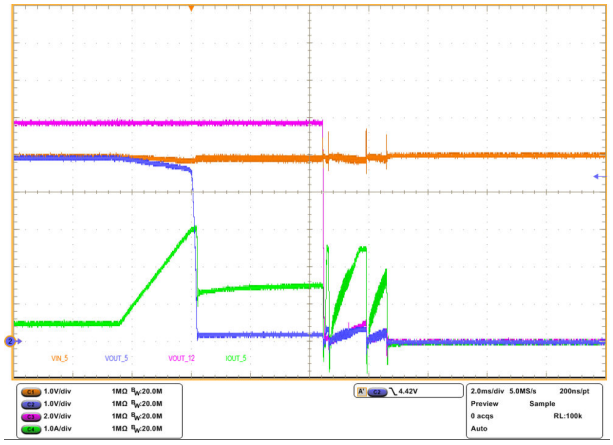
V_{IN_12} = from 0 V to 12 V, V_{IN_5} = from 0 V to 5 V, R_{OUT_5} = 1 Ω, I_{OUT_12} = 0 mA

Figure 41. Startup into overload 12 V channel



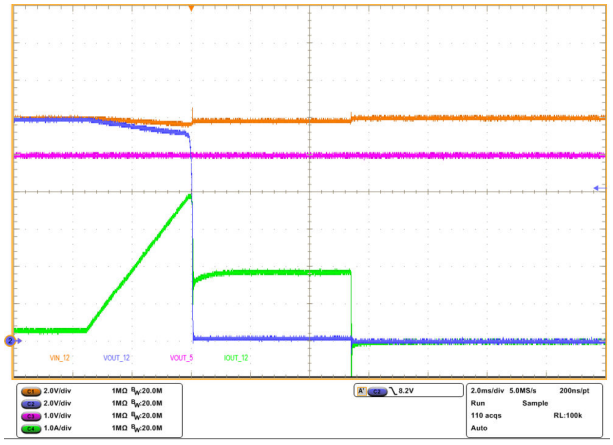
V_{IN_12}= from 0V to 12V, V_{IN_5}= from 0V to 5V, R_{OUT_12}= 2.2Ω, I_{OUT_5}= 0mA

Figure 42. Overcurrent protection during operation 5 V channel (Differential thermal protection)



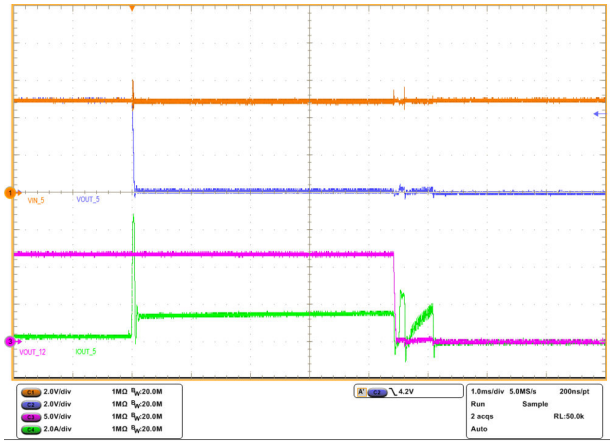
V_{IN_12}= 12V, V_{IN_5}= 5V, I_{OUT_12}= 2A, I_{OUT_5}= CC Load from 300mA to current limit

Figure 43. Overcurrent protection during operation 12 V channel



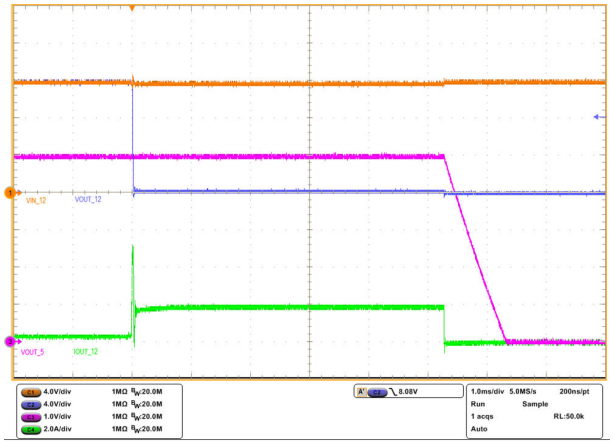
V_{IN_12}= 12V, V_{IN_5}= 5V, I_{OUT_5}= 1A, I_{OUT_12}= CC Load from 300mA to current limit

Figure 44. Output short-circuit during operation 5 V channel (Differential thermal protection)



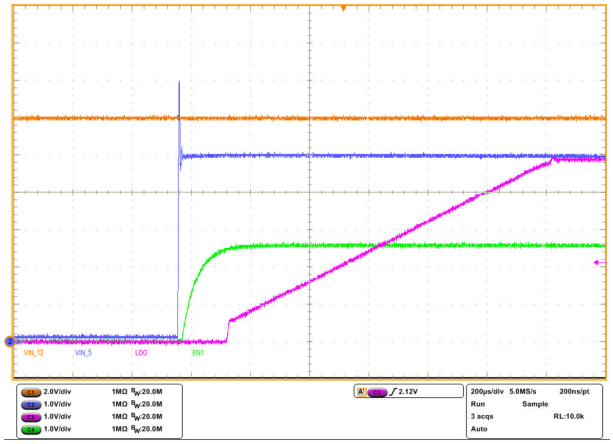
V_{IN_12}= 12V, V_{IN_5}= 5V, I_{OUT_12}= 2A, V_{OUT_5}= from 5V to GND

Figure 45. Output short-circuit during operation 12 V channel



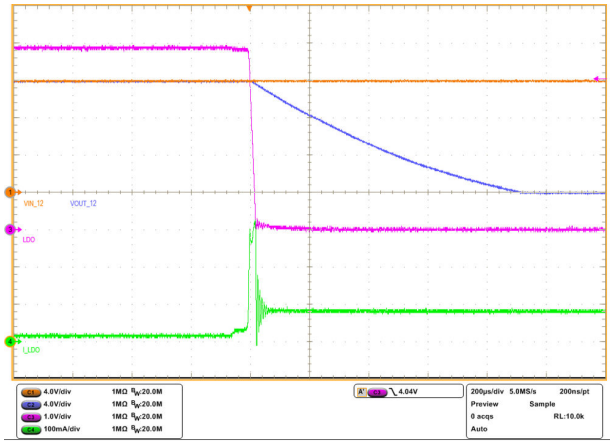
V_{IN_12}= 12V, V_{IN_5}= 5V, I_{OUT_5}= 200mA, V_{OUT_12}= from 12V to GND

Figure 46. LDO start-up time



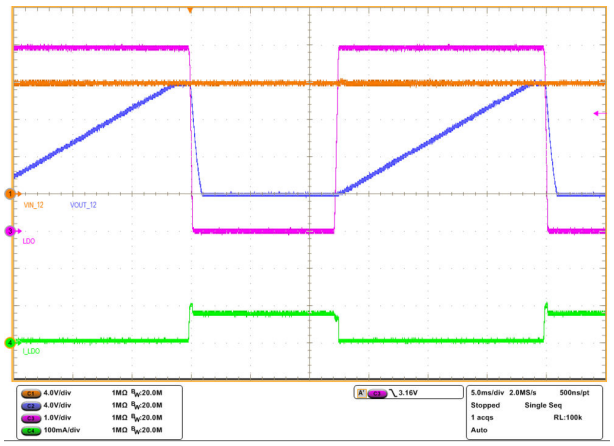
V_{IN_12}= from 0V to 12V, V_{IN_5}= from 0V to 5V, I_{OUT_12}= 0mA, I_{OUT_5}= 0mA, I_{LDO}= 10mA

Figure 47. LDO output short-circuit



V_{IN_12}= 12V, V_{IN_5}= 5V, I_{OUT_12}= 0mA, I_{OUT_5}= 0mA, I_{LDO}= from 10mA to short circuit

Figure 48. LDO overload



V_{IN_12}= 12V, V_{IN_5}= 5V, I_{OUT_12}= 0mA, I_{OUT_5}= 0mA, I_{LDO}= from 10mA to 150mA

Figure 49. LDO's PSRR vs. frequency

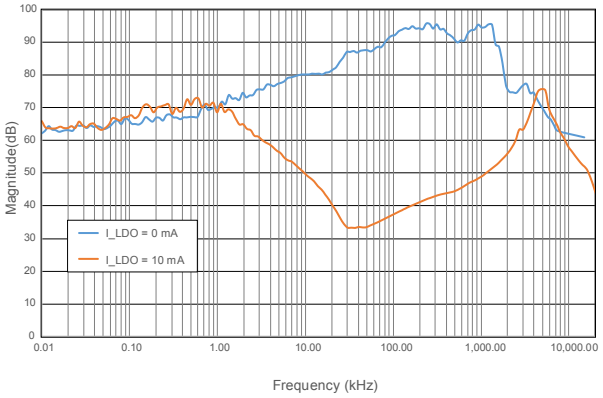
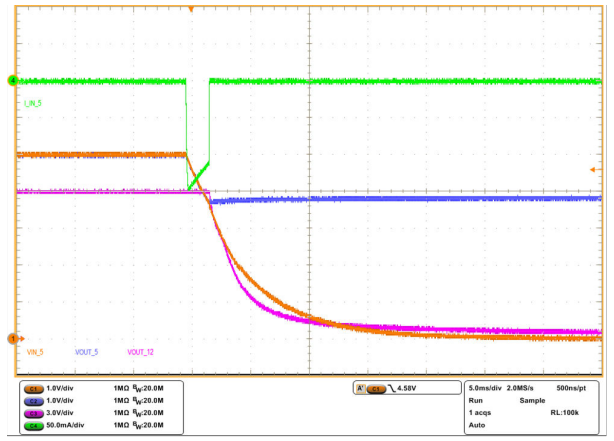
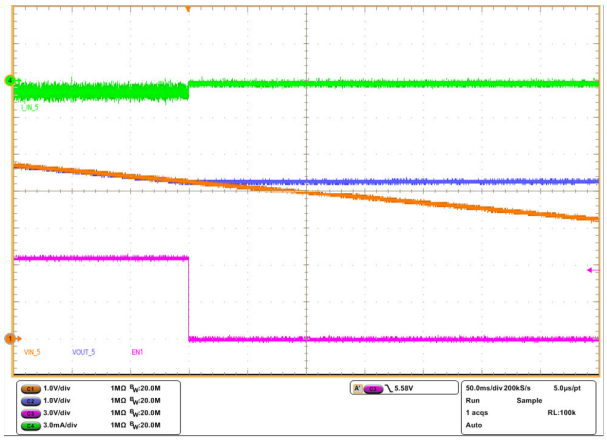


Figure 50. PLP protection though UVLO_5



V_{IN_12}= 12V, V_{IN_5}= from 5V to floating, I_{OUT_12}= 0mA, I_{OUT_5}= 0mA

Figure 51. PLP protection though EN1



V_{IN_12}= 12V, V_{IN_5}= from 5V to floating, V_{EN1}= from 3.3V to GND, I_{OUT_12}= 0mA, I_{OUT_5}= 0mA

8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

8.1 DFN10 (2 x 3 mm) package information

Figure 52. DFN10 (2 x 3 mm) package outline

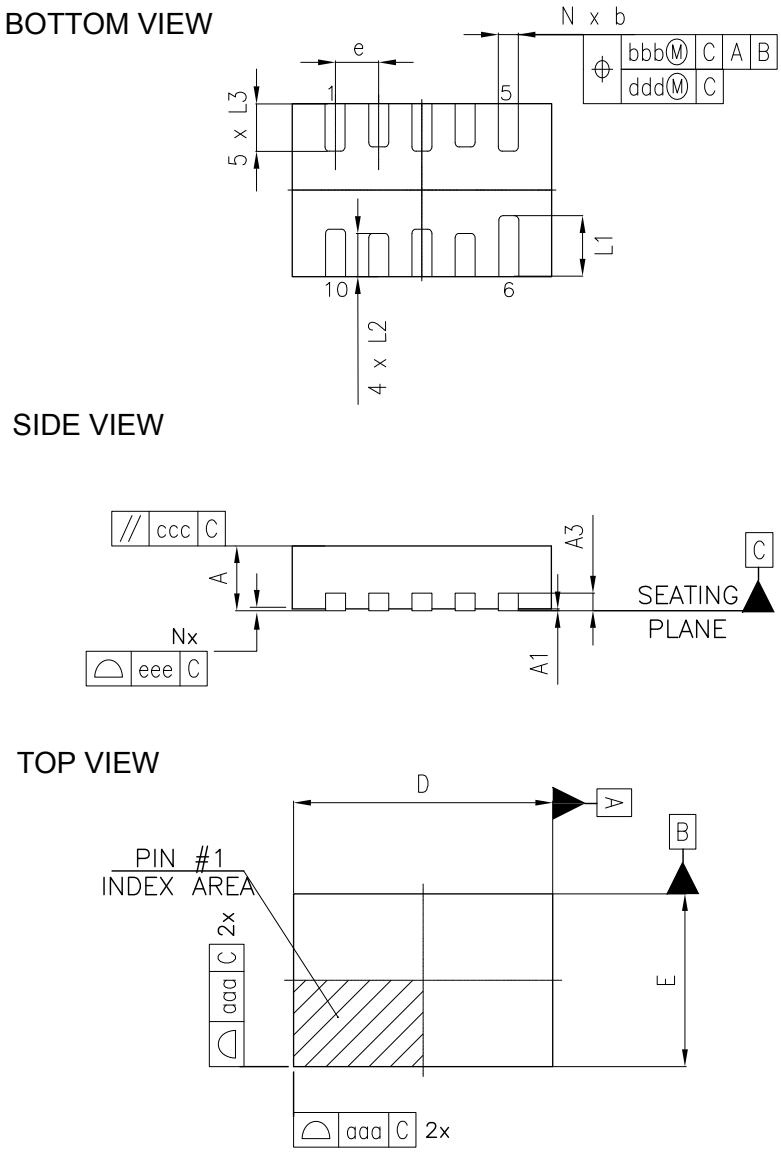
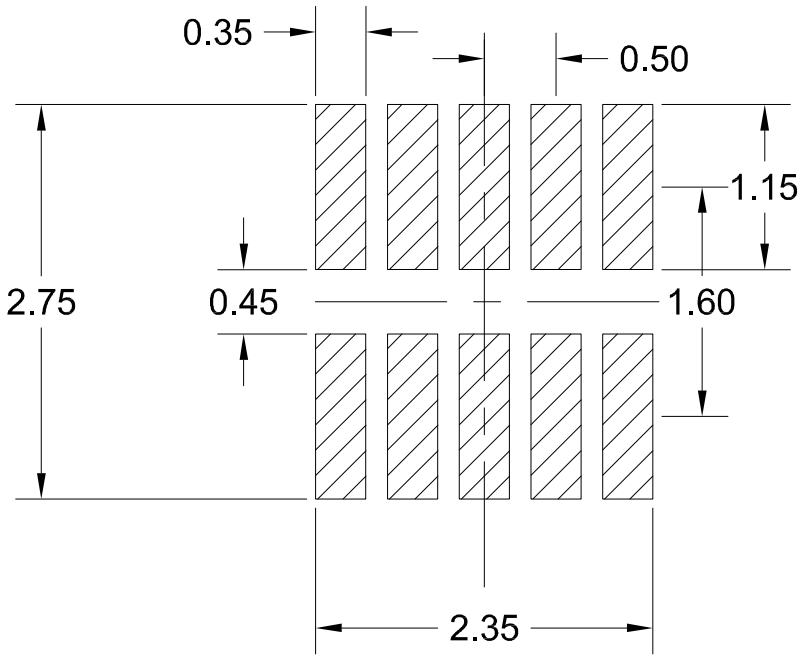


Table 8. **DFN10 (2 x 3 mm) mechanical data**

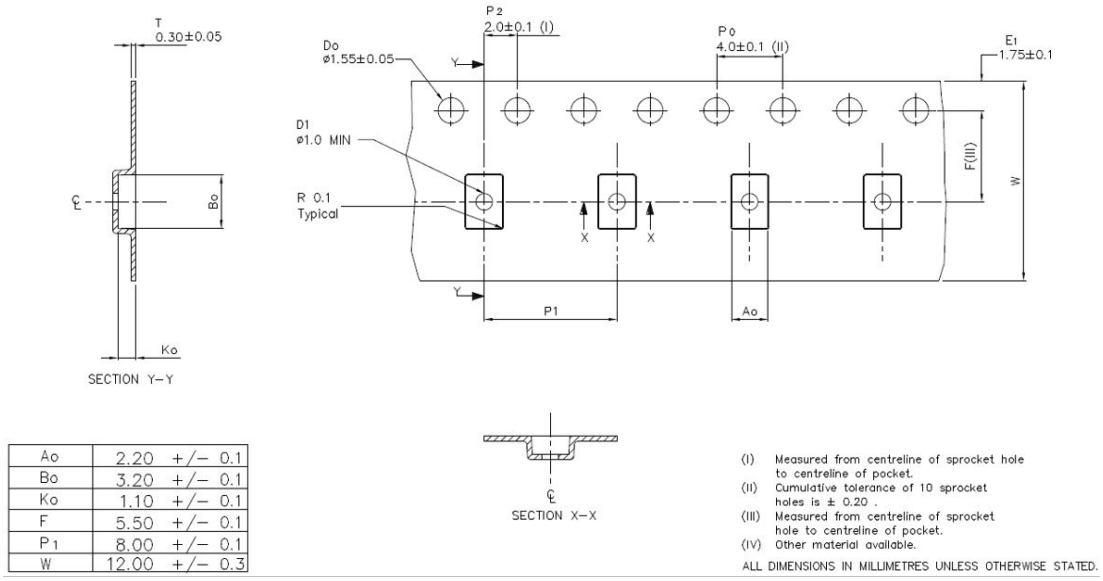
Dim.	mm		
	Min.	Typ.	Max.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.203 ref.	
b	0.180	0.230	0.280
D		3.00 BSC	
e		0.50 BSC	
E		2.00 BCS	
L1	0.60	0.70	0.80
L2	0.40	0.50	0.60
L3	0.45	0.55	0.65
K	0.20		
N		10	
aaa		0.05	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	

Figure 53. **DFN10 (2 x 3 mm) recommended footprint**



8.2 DFN10 (2 x 3) carrier tape information

Figure 54. Carrier tape information



Ao	2.20 +/– 0.1
Bo	3.20 +/– 0.1
Ko	1.10 +/– 0.1
F	5.50 +/– 0.1
P1	8.00 +/– 0.1
W	12.00 +/– 0.3

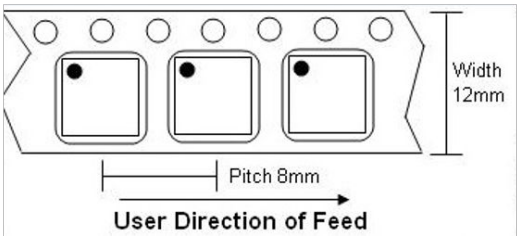


Figure 55. Marking information

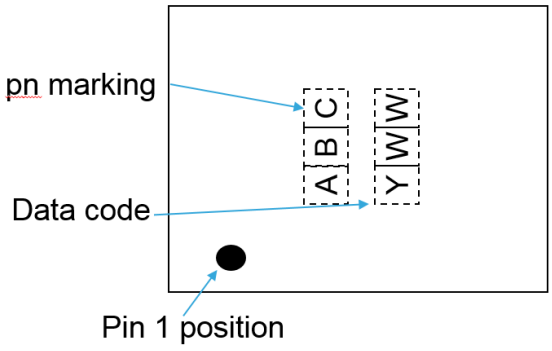
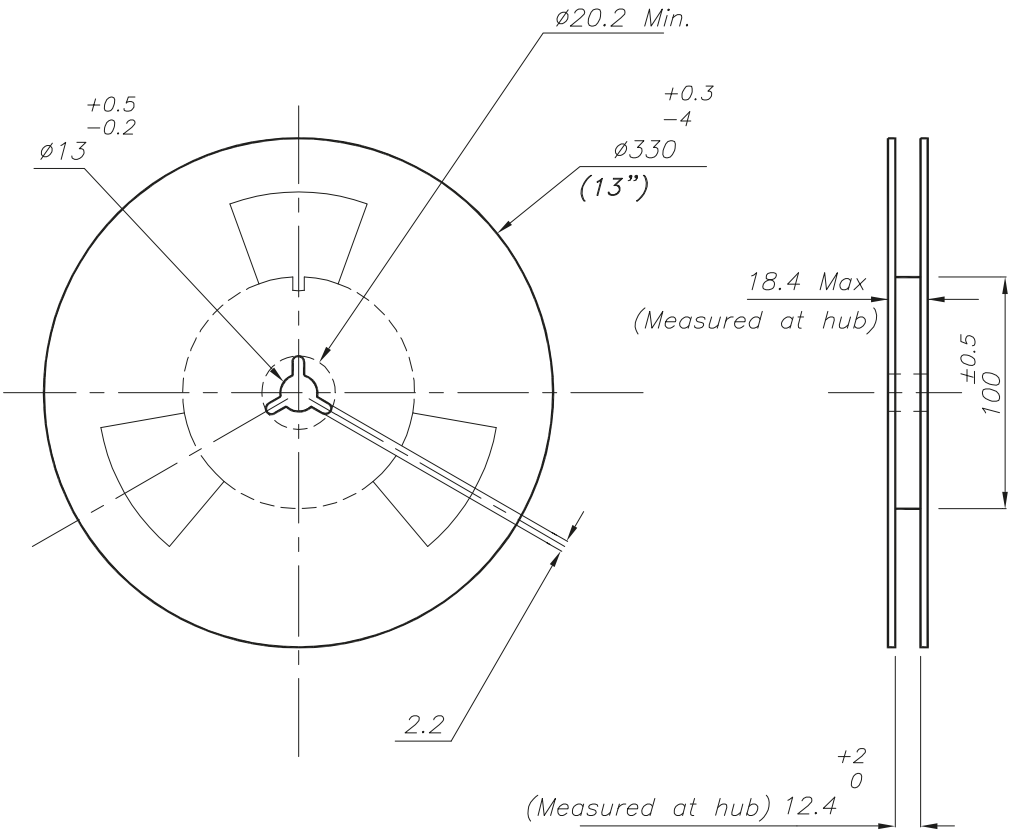


Figure 56. **Reel drawing**



9 Ordering information

Table 9. **Order codes**

Order code	Package	Marking	UVLO_5 [V]	UVLO_12 [V]	Trip point configuration	Note
STEF512SRDBPUR	DFN10 2x3	EDB	4	8.5	3 A on 5 V, 4.5 A on 12 V	5 V LDO + EN1

Revision history

Table 10. **Document revision history**

Date	Revision	Changes
23-Apr-2021	1	Initial release.
12-Apr-2023	2	Updated Section Features

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