

## N-channel 600 V, 0.27 $\Omega$ typ., 13 A MDmesh™ II Power MOSFET in a TO-220FP narrow leads package

Datasheet - production data

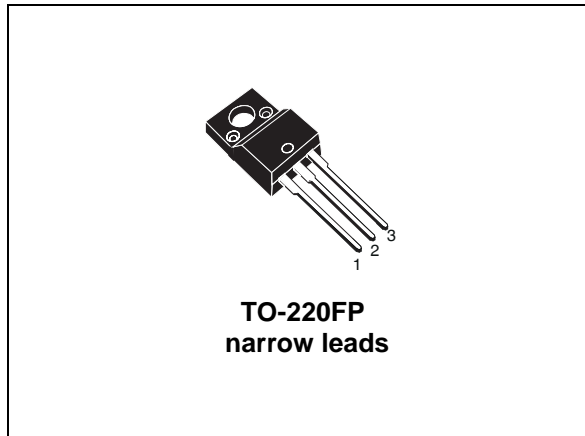
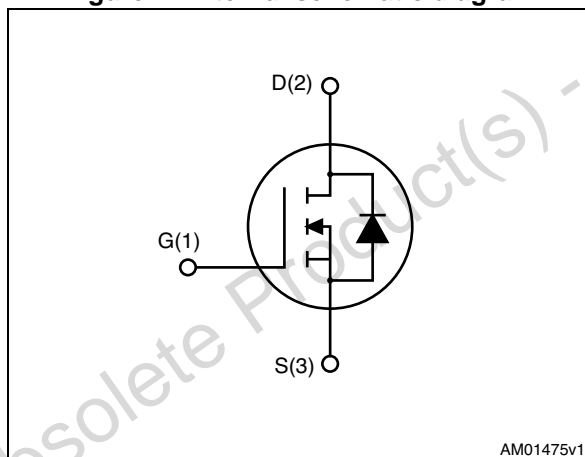


Figure 1. Internal schematic diagram



### Features

Order code	$V_{DS}$	$R_{DS(on) \max}$	$I_D$
STF18NM60N(045Y)	650 V	0.285 $\Omega$	13 A

- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance

### Applications

- Switching applications

### Description

This device is an N-channel Power MOSFET developed using the second generation of MDmesh™ technology. This revolutionary Power MOSFET associates a vertical structure to the company's strip layout to yield one of the world's lowest on-resistance and gate charge. It is therefore suitable for the most demanding high efficiency converters.

Table 1. Device summary

Order code	Marking	Packages	Packaging
STF18NM60N(045Y)	18NM60N	TO-220FP narrow leads	Tube

# Contents

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	600	V
$V_{GS}$	Gate- source voltage	$\pm 25$	
$I_D$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	13 <sup>(1)</sup>	A
$I_D$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	8.2 <sup>(1)</sup>	A
$I_{DM}$ <sup>(2)</sup>	Drain current (pulsed)	52 <sup>(1)</sup>	A
$P_{TOT}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	30	W
$I_{AR}$	Avalanche current, repetitive or not-repetitive (pulse width limited by $T_J$ max)	4.5	A
$E_{AS}$	Single pulse avalanche energy (starting $T_J = 25\text{ }^\circ\text{C}$ , $I_D = I_{AR}$ , $V_{DD} = 50\text{ V}$ )	350	mJ
$dv/dt$ <sup>(3)</sup>	Peak diode recovery voltage slope	15	V/ns
$V_{ISO}$	Insulation withstand voltage (RMS) from all three leads to external heat sink ( $t=1\text{ s}$ ; $T_C=25\text{ }^\circ\text{C}$ )	2500	V
$T_J$ $T_{stg}$	Operating junction temperature Storage temperature	-55 to 150	$^\circ\text{C}$

1. Limited only by maximum temperature allowed
2. Pulse width limited by safe operating area
3.  $I_{SD} \leq 13\text{ A}$ ,  $di/dt \leq 400\text{ A}/\mu\text{s}$ , peak  $V_{DS} \leq V_{(BR)DSS}$

**Table 3. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	4.17	$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-amb max	62.5	$^\circ\text{C}/\text{W}$

## 2 Electrical characteristics

( $T_{CASE}=25\text{ °C}$  unless otherwise specified)

**Table 4. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$ , $V_{GS} = 0$	600			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = 600\text{ V}$			1	$\mu\text{A}$
		$V_{DS} = 600\text{ V}$ , $T_J = 125\text{ °C}$			10	$\mu\text{A}$
$I_{GSS}$	Gate body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 25\text{ V}$ ; $V_{DS} = 0$			100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$ , $I_D = 6.5\text{ A}$		0.260	0.285	$\Omega$

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 50\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0$		1000		pF
$C_{oss}$	Output capacitance			60		pF
$C_{rss}$	Reverse capacitance			3		pF
$C_{osseq}^{(1)}$	Equivalent out. capacitance	$V_{DS} = 0\text{ V}$ to $480\text{ V}$ , $V_{GS} = 0$		225		pF
$R_g$	Intrinsic gate resistance	$f = 1\text{ MHz}$ open drain	3	3.5	6.5	$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 480\text{ V}$ , $I_D = 13\text{ A}$ , $V_{GS} = 10\text{ V}$ (see <a href="#">Figure 14</a> )		35		nC
$Q_{gs}$	Gate source charge			6		nC
$Q_{gd}$	Gate-drain charge			20		nC

1. Cross eq: defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$ .

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 300\text{ V}$ , $I_D = 13\text{ A}$ $R_G = 4.7\text{ }\Omega$ , $V_{GS} = 10\text{ V}$ (see <a href="#">Figure 13</a> )	-	20	-	ns
$t_r$	Rise time		-	822	-	ns
$t_{d(off)}$	Turn-off-delay time		-	50	-	ns
$t_f$	Fall time		-	40	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source drain current		-		12	A
$I_{SDM}^{(1)}$	Source drain current (pulsed)		-		48	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 13 \text{ A}$ , $V_{GS} = 0 \text{ V}$	-		1.6	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 13 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 60 \text{ V}$ (see <a href="#">Figure 15</a> )	-	428		ns
$Q_{rr}$	Reverse recovery charge		-	4.7		nC
$I_{RRM}$	Reverse recovery current		-	21.5		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 13 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 60 \text{ V}$ , $T_j = 150 \text{ }^\circ\text{C}$ (see <a href="#">Figure 15</a> )	-	570		ns
$Q_{rr}$	Reverse recovery charge		-	6.2		nC
$I_{RRM}$	Reverse recovery current		-	22		A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

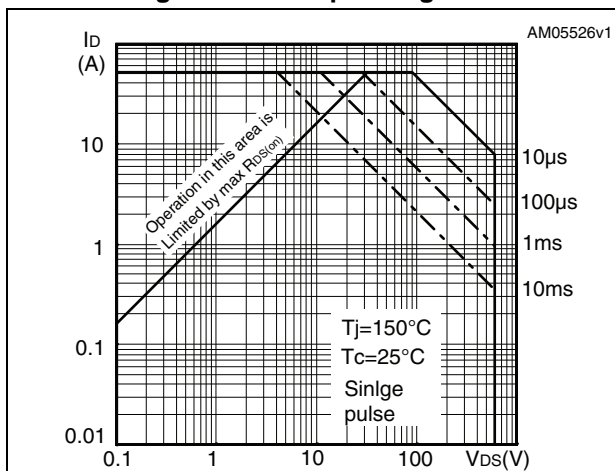


Figure 3. Thermal impedance

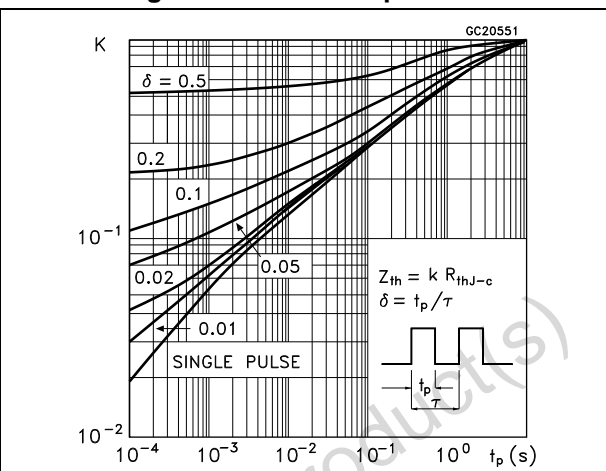


Figure 4. Output characteristics

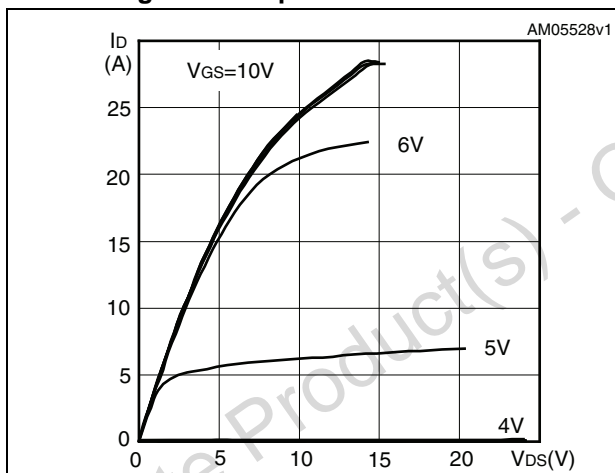


Figure 5. Transfer characteristics

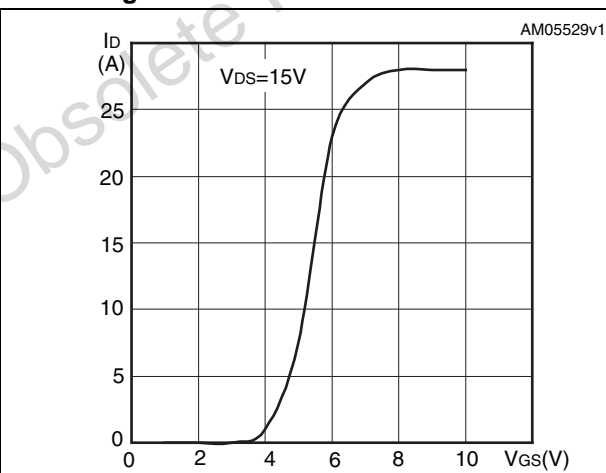


Figure 6. Static drain-source on-resistance

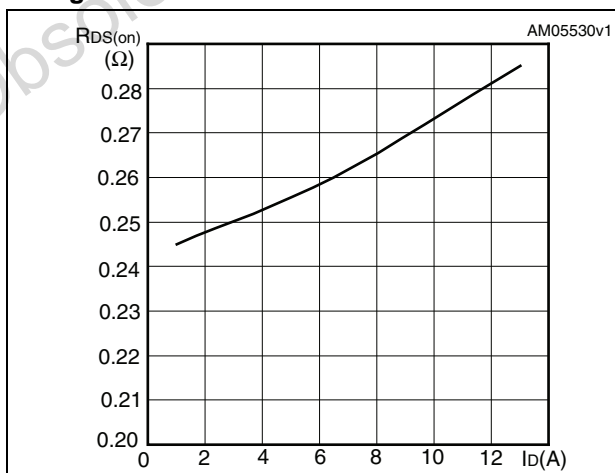


Figure 7. Gate charge vs gate-source voltage

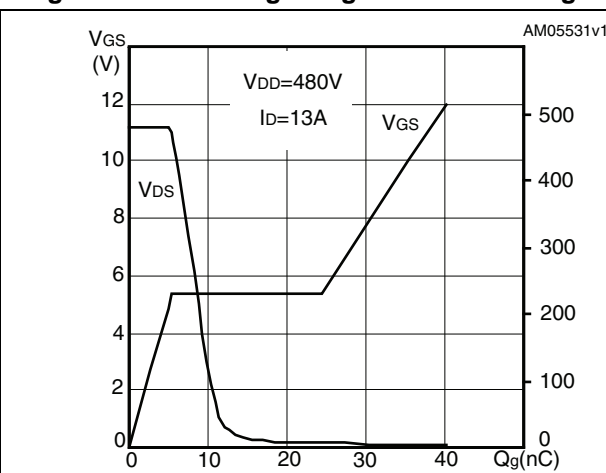


Figure 8. Capacitance variations

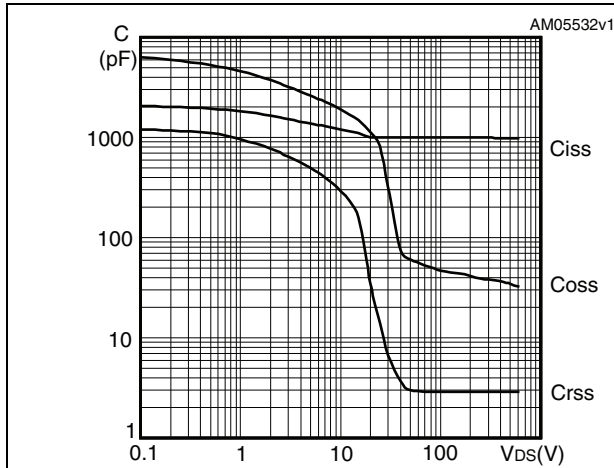


Figure 9. Output capacitance stored energy

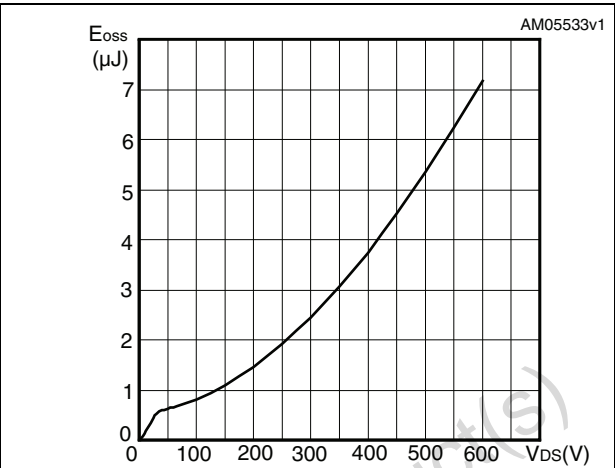


Figure 10. Normalized gate threshold voltage vs temperature

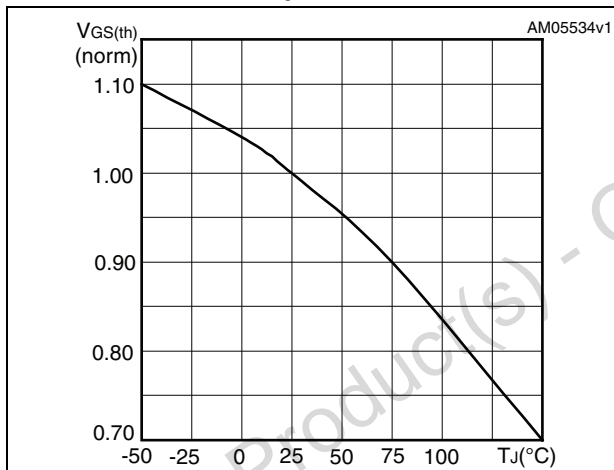


Figure 11. Normalized on-resistance vs temperature

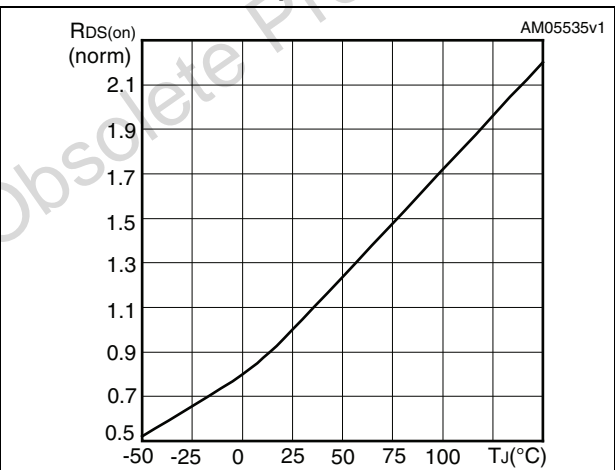
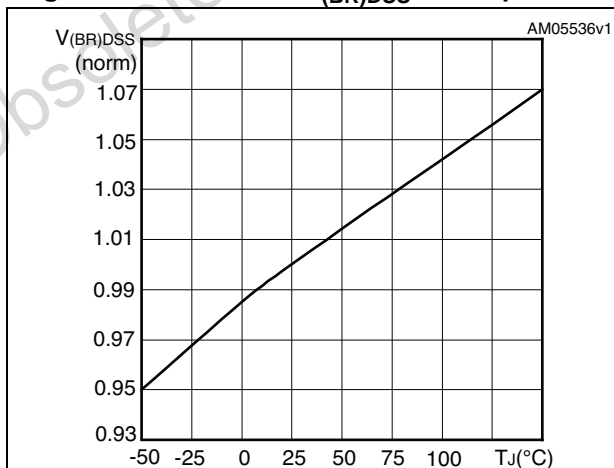


Figure 12. Normalized  $V_{(BR)DSS}$  vs temperature



### 3 Test circuits

Figure 13. Switching times test circuit for resistive load

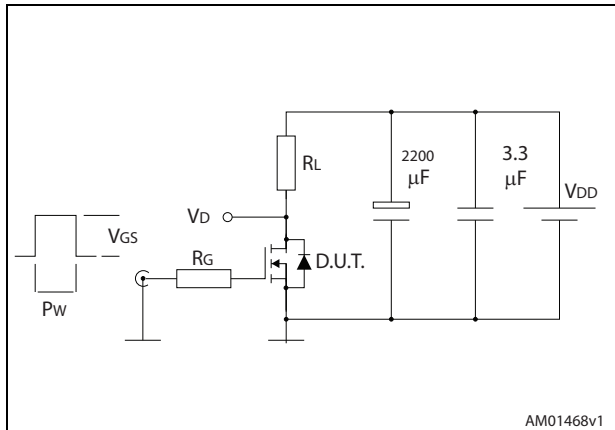


Figure 14. Gate charge test circuit

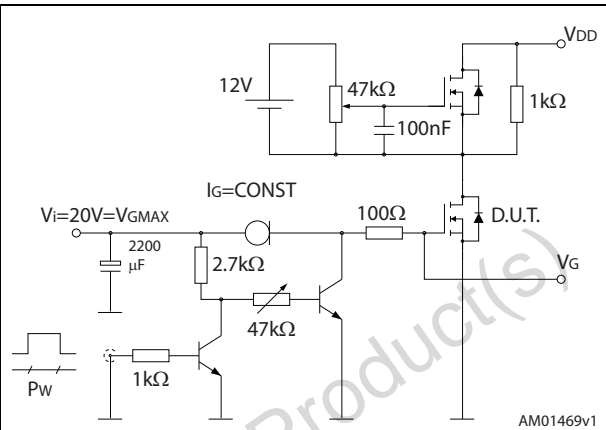


Figure 15. Test circuit for inductive load switching and diode recovery times

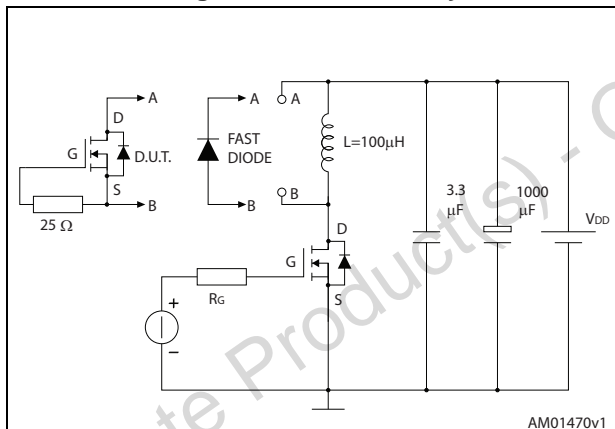


Figure 16. Unclamped inductive load test circuit

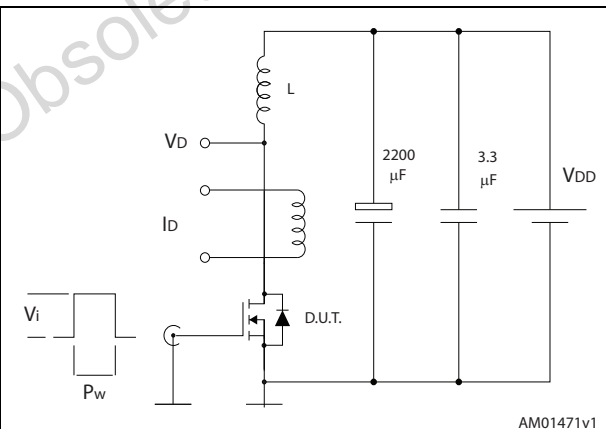


Figure 17. Unclamped inductive waveform

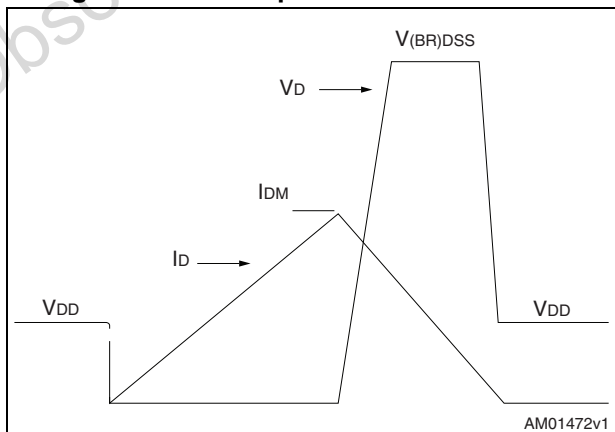
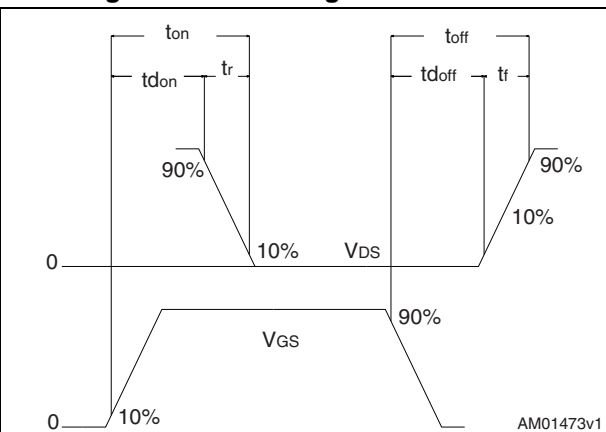


Figure 18. Switching time waveform



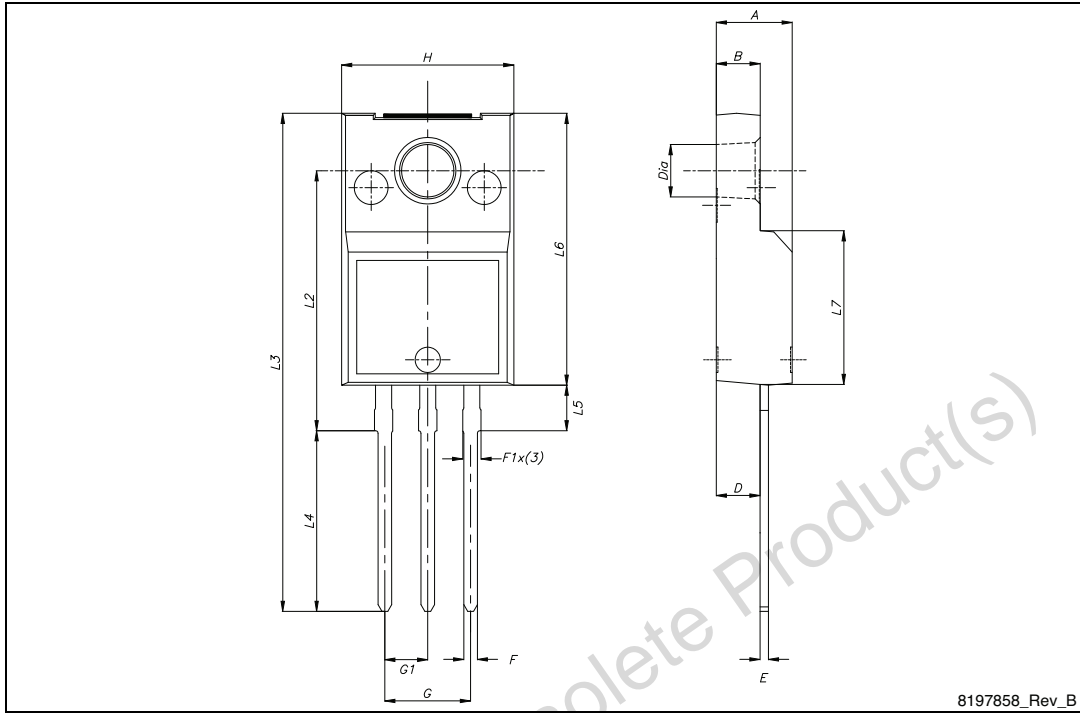


## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.

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Figure 19. TO-220FP narrow leads drawing



8197858\_Rev\_B

Table 8. TO-220FP narrow leads mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	0.95		1.20
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2	15.20		15.60
L3	28.6		30.6
L4	10.3		11.1
L5	2.60	2.70	2.90
L6	15.8	16.0	16.2
L7	9		9.3
$\varnothing$	3		3.2

## 5 Revision history

Table 9. Document revision history

Date	Revision	Changes
17-Feb-2012	1	First release.
22-May-2012	2	Updated $R_g$ with minimum and maximum values in <a href="#">Table 5: Dynamic</a> .
23-Apr-2014	3	<ul style="list-style-type: none"><li>– Updated: <a href="#">Figure 13, 14, 15</a> and <a href="#">16</a></li><li>– Updated: <a href="#">Section 4: Package mechanical data</a></li><li>– Minor text changes</li></ul>

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