STH36N60M6-7

N-channel 600 V, 0.085 Ω typ., 30 A MDmesh™ M6 Power MOSFET in a H²PAK-7 package

Datasheet - preliminary data

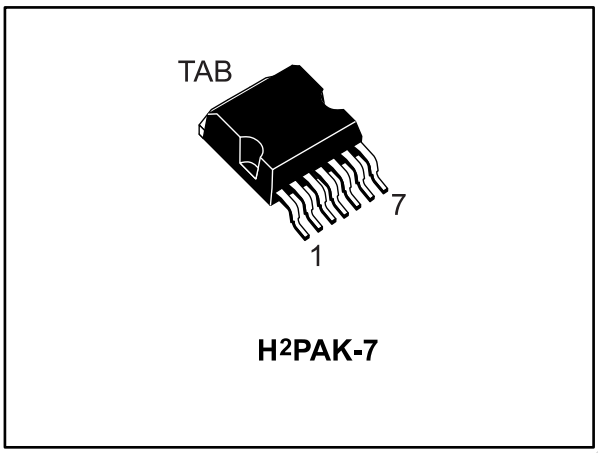
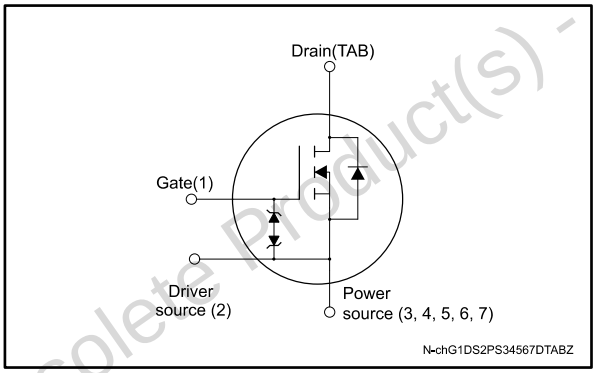


Figure 1: Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STH36N60M6-7	600 V	0.099 Ω	30 A

- Reduced switching losses
- Lower $R_{DS(on)}$ x area vs previous generation
- Low gate input resistance
- 100% avalanche tested
- Zener-protected
- High creepage package
- Excellent switching performance thanks to the extra driving source pin

Applications

- Switching applications

Description

The new MDmesh™ M6 technology incorporates the most recent advancements to the well-known and consolidated MDmesh family of SJ MOSFETs by STMicroelectronics. Compared with the previous MDmesh generation, M6 combines an excellent improvement to $R_{DS(on)}$ * area with one of the most effective switching behaviors available, and a user-friendly driving experience for maximum end-application efficiency.

Table 1: Device summary

Order code	Marking	Package	Packing
STH36N60M6-7	36N60M6	H²PAK-7	Tape & reel

Contents

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 25	V
I_D	Drain current (continuous) at T_C = 25 °C	30	A
I_D	Drain current (continuous) at T_C = 100 °C	19	A
I_D(1)	Drain current (pulsed)	120	A
P_{TOT}	Total dissipation at T_C = 25 °C	208	W
dv/dt(2)	Peak diode recovery voltage slope	15	V/ns
dv/dt(3)	MOSFET dv/dt ruggedness	50	
T_J	Operating junction temperature	-55 to 150	°C
T_{stg}	Storage temperature		

Notes:

(1)Pulse width limited by safe operating area

(2)I_{SD} ≤ 30 A, di/dt ≤ 400 A/µs; $V_{DS\ peak} < V_{(BR)DSS}$, V_{DD} = 400 V

(3)V_{DS} ≤ 480 V

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case max.	0.6	°C/W
$R_{thj\text{-}pcb}$	Thermal resistance junction-pcb max.(1)	30	

Notes:

(1)When mounted on 1 inch² FR-4, 2 Oz copper board.

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T_{jmax})	5	A
E_{AS}	Single pulse avalanche energy (starting T_j = 25°C, I_D = I_{AR}, V_{DD} = 50 V)	750	mJ

2 Electrical characteristics

T_C = 25 °C unless otherwise specified

Table 5: On/off-state

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS}= 0 V, I_D = 1 mA	600			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 600 V			1	µA
		V_{GS} = 0 V, V_{DS} = 600 V; T_C = 125 °C			100	µA
I_{GSS}	Gate body leakage current	V_{DS} = 0 V, V_{GS} = ±25 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 15 A		0.085	0.099	Ω

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0 V	-	1800	-	pF
C_{oss}	Output capacitance		-	140	-	pF
C_{rss}	Reverse transfer capacitance		-	2.8	-	pF
$C_{oss\ eq.}$ (1)	Equivalent output capacitance	V_{DS} = 0 to 480 V, V_{GS} = 0 V	-	317	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz open drain	-	1.4	-	Ω
Q_g	Total gate charge	V_{DD} = 480 V, I_D = 30 A, V_{GS}= 10 V, (See *Figure 3: "Test circuit for gate charge behavior"*)	-	48	-	nC
Q_{gs}	Gate-source charge		-	8	-	nC
Q_{gd}	Gate-drain charge		-	23	-	nC

Notes:

(1) $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD}= 300 V, I_D = 15 A, R_G = 4.7 Ω, V_{GS} = 10 V (See *Figure 2: "Test circuit for resistive load switching times"* and *Figure 7: "Switching time waveform"*)	-	16	-	ns
t_r	Rise time		-	10	-	ns
$t_{d(off)}$	Turn-off delay time		-	7	-	ns
t_f	Fall time		-	60	-	ns

Table 8: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		30	A
I_{SDM} (1)	Source-drain current (pulsed)		-		120	A
V_{SD} (2)	Forward on voltage	I_{SD} = 30 A, V_{GS} = 0 V	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 30 A, di/dt = 100 A/µs, V_{DD} = 60 V, (See *Figure 7: "Switching time waveform"*)	-	340		ns
Q_{rr}	Reverse recovery charge		-	5.3		µC
I_{RRM}	Reverse recovery current		-	31		A
t_{rr}	Reverse recovery time	I_{SD} = 30 A, di/dt = 100 A/µs, V_{DD} = 60 V, T_j = 150 °C (See *Figure 7: "Switching time waveform"*)	-	430		ns
Q_{rr}	Reverse recovery charge		-	7.7		µC
I_{RRM}	Reverse recovery current		-	36		A

Notes:

(1)Pulse width limited by safe operating area

(2)Pulsed: pulse duration = 300 µs, duty cycle 1.5%

3 Test circuits

Figure 2: Test circuit for resistive load switching times

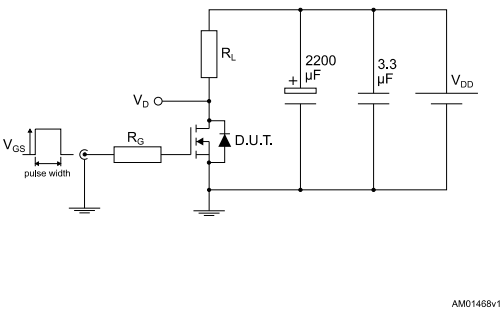


Figure 3: Test circuit for gate charge behavior

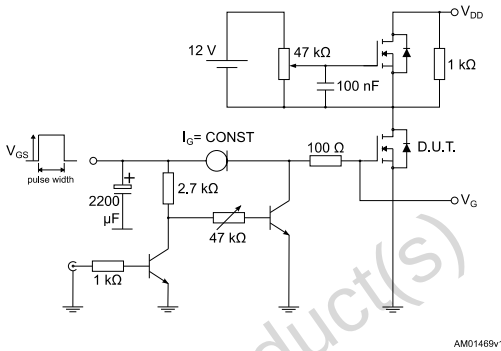


Figure 4: Test circuit for inductive load switching and diode recovery times

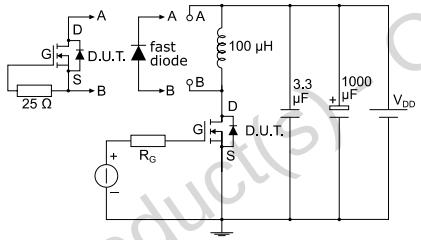


Figure 5: Unclamped inductive load test circuit

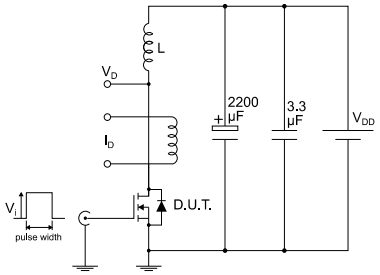


Figure 6: Unclamped inductive waveform

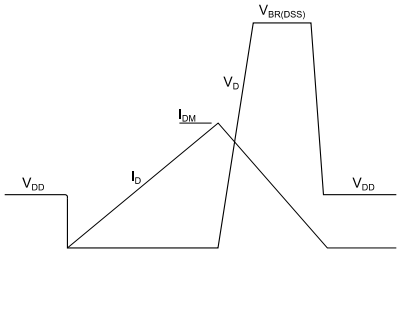
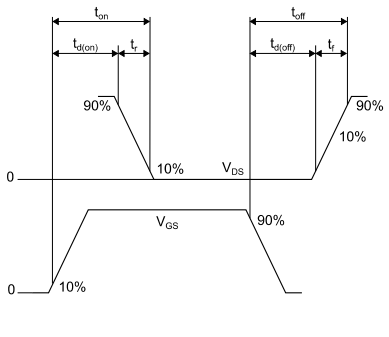


Figure 7: Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

4.1 H²PAK-7 package information

Figure 8: H²PAK-7 package outline

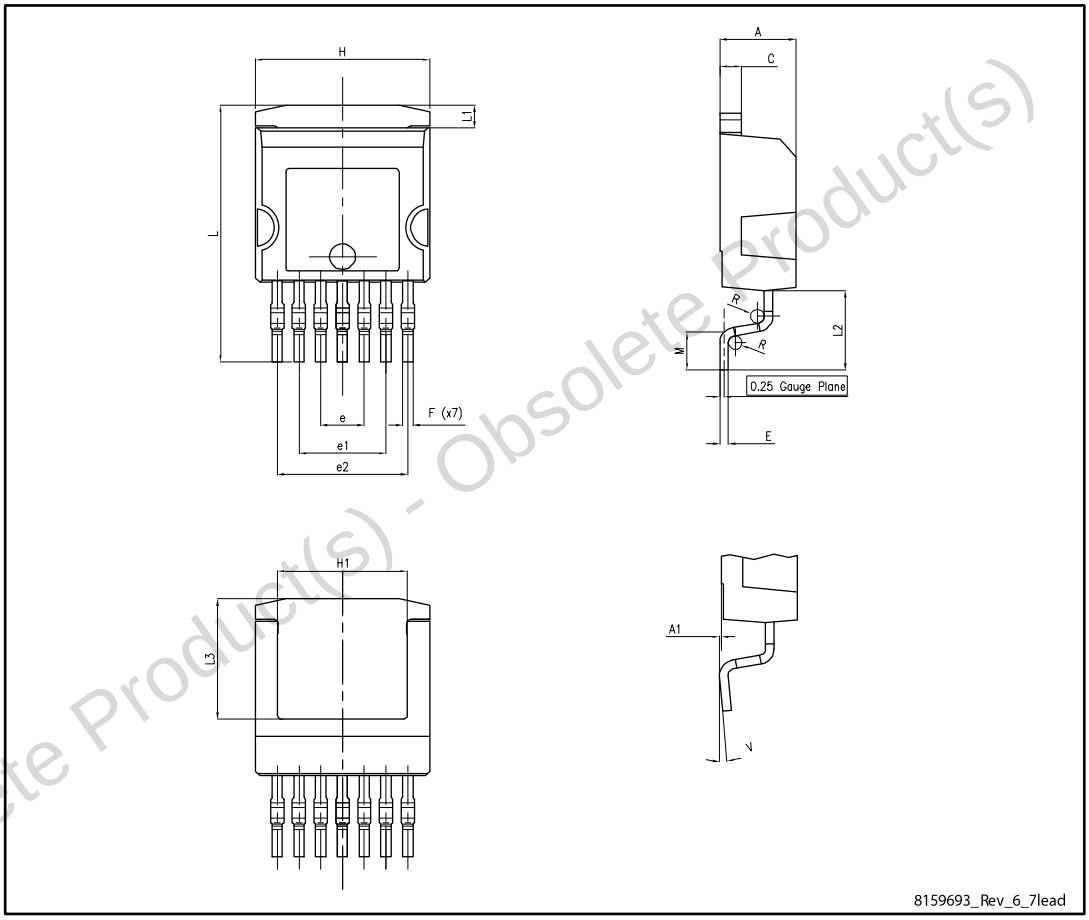
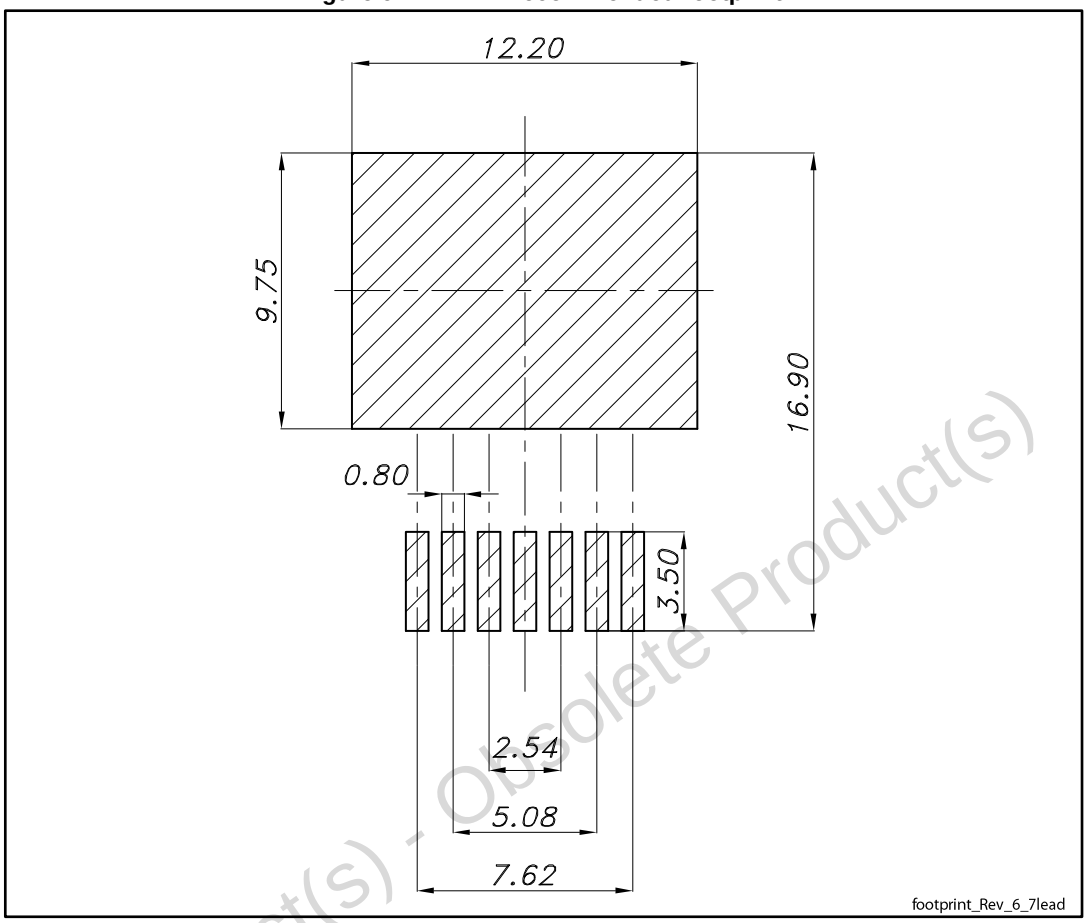


Table 9: H²PAK-7 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.30	-	4.80
A1	0.03		0.20
C	1.17		1.37
e	2.34		2.74
e1	4.88		5.28
e2	7.42		7.82
E	0.45		0.60
F	0.50		0.70
H	10.00		10.40
H1	7.40		7.60
L	14.75		15.25
L1	1.27		1.40
L2	4.35		4.95
L3	6.85		7.25
M	1.90		2.50
R	0.20		0.60
V	0°		8°

Figure 9: H²PAK-7 recommended footprint



Dimensions are in mm.

4.2 H²PAK-7 packaging information

Figure 10: Tape outline

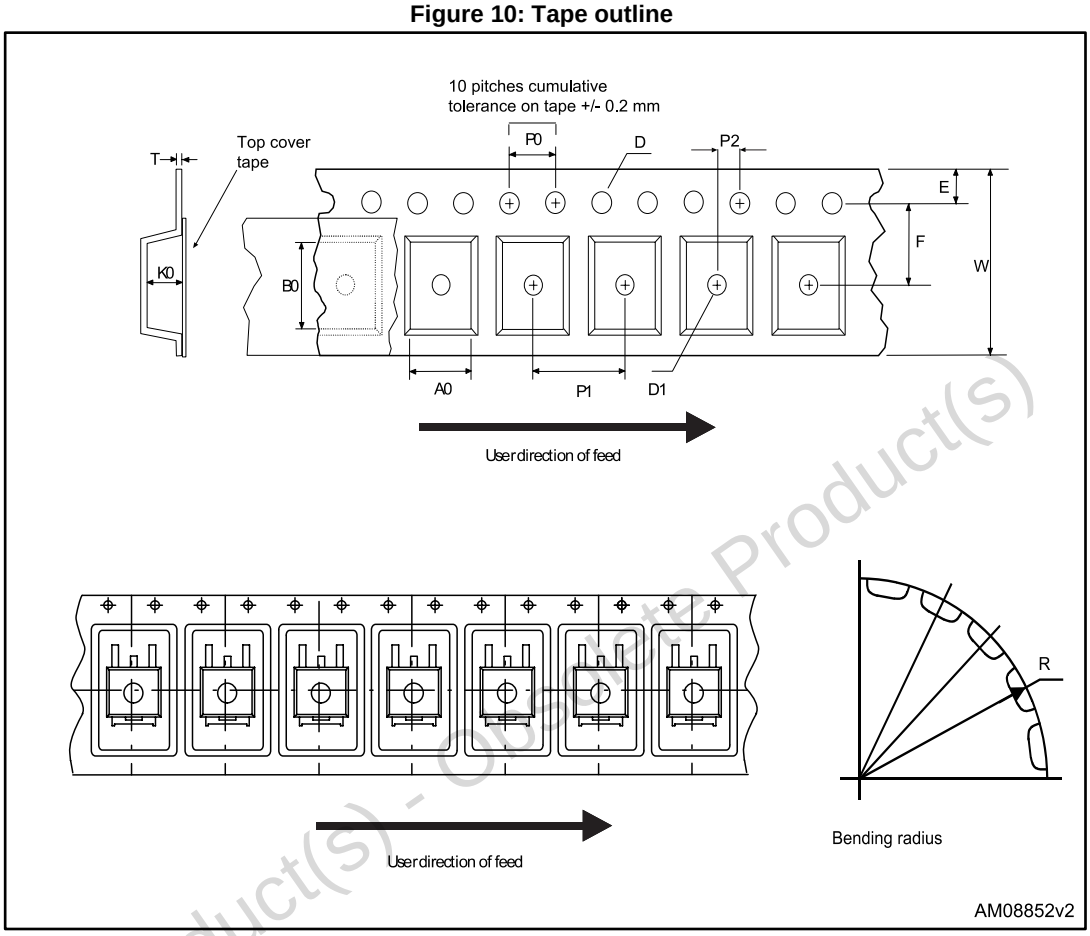


Figure 11: Reel outline

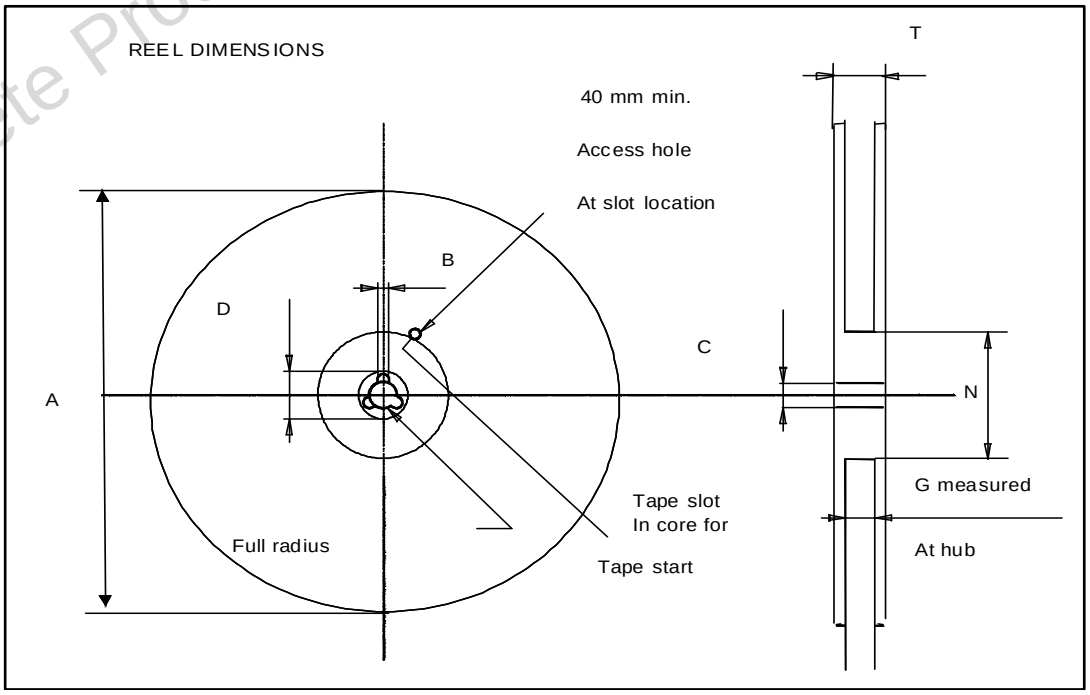


Table 10: Tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base quantity		1000
P2	1.9	2.1	Bulk quantity		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

5 Revision history

Table 11: Document revision history

Date	Revision	Changes
14-Dec-2015	1	Initial release.

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