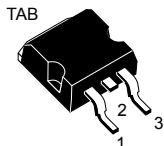
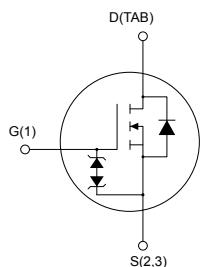


### Automotive-grade N-channel 1200 V, 1.65 $\Omega$ typ., 6 A MDmesh K5 Power MOSFET in an H<sup>2</sup>PAK-2 package

#### Features



H<sup>2</sup>PAK-2



NCHG1DTABS23T2

Order code	V <sub>DS</sub>	R <sub>DS(on)</sub> max.	I <sub>D</sub>
STH8N120K5-2AG	1200 V	2.00 $\Omega$	6 A



- AEC-Q101 qualified
- Industry's lowest R<sub>DS(on)</sub> x area
- Industry's best FoM (figure of merit)
- Ultra-low gate charge
- 100% avalanche tested
- Zener-protected

#### Applications

- Switching applications

#### Description

This very high voltage N-channel Power MOSFET is designed using MDmesh K5 technology based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance and ultra-low gate charge for applications requiring superior power density and high efficiency.



#### Product status link

[STH8N120K5-2AG](#)

#### Product summary<sup>(1)</sup>

Order code	STH8N120K5-2AG
Marking	8A120K5
Package	H <sup>2</sup> PAK-2
Packing	Tape and reel

1. HTRB test was performed at 80% of V<sub>(BR)DSS</sub> according to AEC-Q101 rev. C. All other tests were performed according to AEC-Q101 rev. D.

## 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{GS}$	Gate-source voltage	$\pm 30$	V
$I_D$	Drain current (continuous) at $T_C = 25^\circ\text{C}$	6	A
	Drain current (continuous) at $T_C = 100^\circ\text{C}$	3.5	
$I_{DM}^{(1)}$	Drain current (pulsed)	12	A
$P_{TOT}$	Total power dissipation at $T_C = 25^\circ\text{C}$	165	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	4.5	V/ns
$dv/dt^{(3)}$	MOSFET dv/dt ruggedness	50	V/ns
$T_{stg}$	Storage temperature range	-55 to 150	$^\circ\text{C}$
$T_J$	Operating junction temperature range		$^\circ\text{C}$

1. Pulse width limited by safe operating area.
2.  $I_{SD} \leq 6 \text{ A}$ ,  $di/dt \leq 100 \text{ A}/\mu\text{s}$ ,  $V_{DS}$  (peak)  $\leq V_{(BR)DSS}$ .
3.  $V_{DS} \leq 960 \text{ V}$ .

**Table 2. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thJC}$	Thermal resistance, junction-to-case	0.76	$^\circ\text{C}/\text{W}$
$R_{thJA}^{(1)}$	Thermal resistance, junction-to-ambient	30	$^\circ\text{C}/\text{W}$

1. When mounted on a standard 1 inch<sup>2</sup> area of FR-4 PCB with 2-oz copper.

**Table 3. Avalanche characteristics**

Symbol	Parameter	Value	Unit
$I_{AR}$	Avalanche current, repetitive or not repetitive (pulse width limited by $T_J$ max.)	1.3	A
$E_{AS}$	Single pulse avalanche energy (starting $T_J = 25^\circ\text{C}$ , $I_D = I_{AR}$ , $V_{DD} = 100 \text{ V}$ )	243	mJ

## 2 Electrical characteristics

$T_C = 25^\circ\text{C}$  unless otherwise specified.

**Table 4. On/off-state**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(\text{BR})\text{DSS}}$	Drain-source breakdown voltage	$V_{GS} = 0 \text{ V}, I_D = 1 \text{ mA}$	1200			V
$I_{\text{DSS}}$	Zero gate voltage drain current	$V_{GS} = 0 \text{ V}, V_{DS} = 1200 \text{ V}$			1	$\mu\text{A}$
		$V_{GS} = 0 \text{ V}, V_{DS} = 1200 \text{ V}, T_C = 125^\circ\text{C}$ <sup>(1)</sup>			50	
$I_{\text{GSS}}$	Gate body leakage current	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			$\pm 10$	$\mu\text{A}$
$V_{GS(\text{th})}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 100 \mu\text{A}$	3	4	5	V
$R_{\text{DS(on)}}$	Static drain-source on-resistance	$V_{GS} = 10 \text{ V}, I_D = 2.5 \text{ A}$		1.65	2.00	$\Omega$

1. Specified by design, not tested in production.

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{\text{iss}}$	Input capacitance	$V_{DS} = 100 \text{ V}, f = 1 \text{ MHz}, V_{GS} = 0 \text{ V}$	-	505	-	pF
$C_{\text{oss}}$	Output capacitance		-	35	-	pF
$C_{\text{rss}}$	Reverse transfer capacitance			0.6		pF
$C_{0(\text{er})}^{(1)}$	Equivalent capacitance energy related	$V_{DS} = 0 \text{ to } 960 \text{ V}, V_{GS} = 0 \text{ V}$	-	24	-	pF
$C_{0(\text{tr})}^{(2)}$	Equivalent capacitance time related		-	70	-	pF
$R_g$	Intrinsic gate resistance	$f = 1 \text{ MHz}, I_D = 0 \text{ A}$	-	8	-	$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 960 \text{ V}, I_D = 2.5 \text{ A}, V_{GS} = 0 \text{ to } 10 \text{ V}$ (see Figure 15. Test circuit for gate charge behavior)	-	14.4 <sup>(3)</sup>	-	nC
$Q_{gs}$	Gate-source charge		-	3.9 <sup>(3)</sup>	-	nC
$Q_{gd}$	Gate-drain charge		-	7.9 <sup>(3)</sup>	-	nC

1.  $C_{0(\text{er})}$  is a constant capacitance value that gives the same stored energy as  $C_{\text{oss}}$  while  $V_{DS}$  is rising from 0 V to the stated value.
2.  $C_{0(\text{tr})}$  is a constant capacitance value that gives the same charging time as  $C_{\text{oss}}$  while  $V_{DS}$  is rising from 0 V to the stated value.
3. Baseline values from simulations.

**Table 6. Switching times**

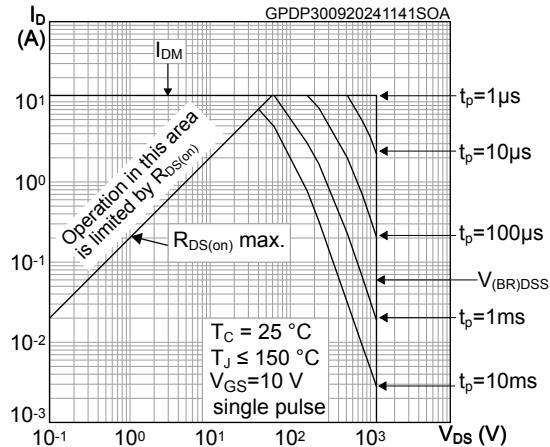
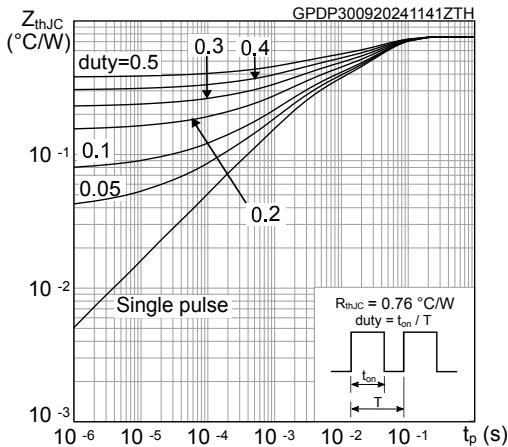
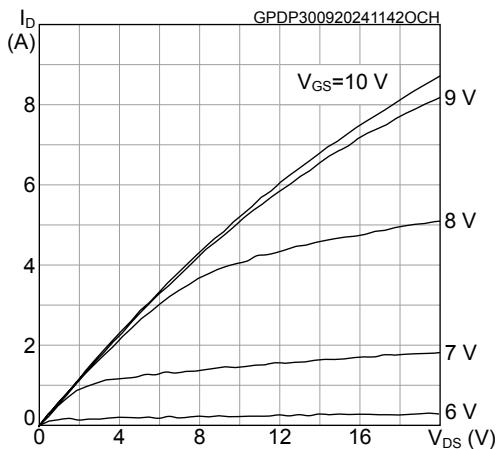
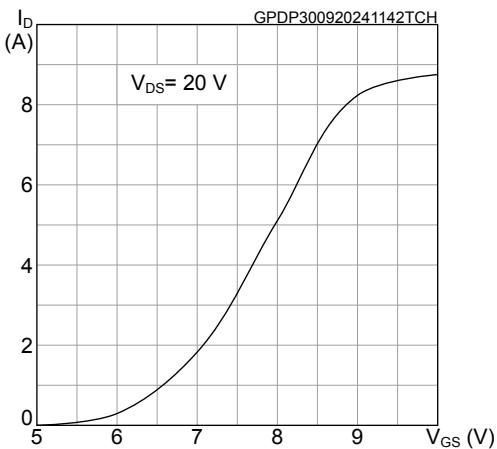
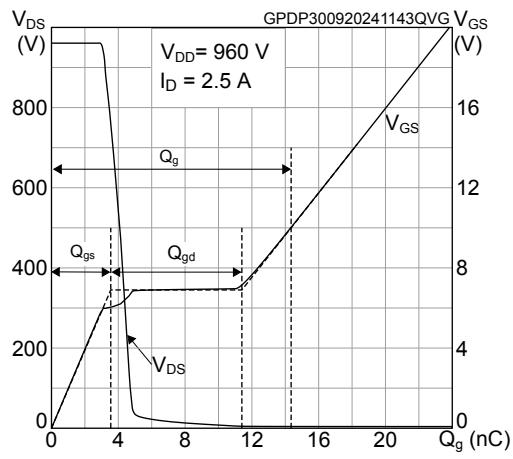
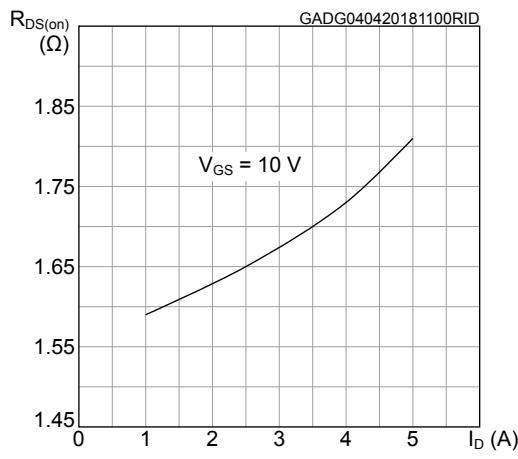
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(\text{on})}$	Turn-on delay time	$V_{DD} = 600 \text{ V}, I_D = 2.5 \text{ A}, R_G = 4.7 \Omega, V_{GS} = 10 \text{ V}$ (see Figure 14. Test circuit for resistive load switching times and Figure 19. Switching time waveform)	-	11	-	ns
$t_r$	Rise time		-	6	-	ns
$t_{d(\text{off})}$	Turn-off delay time		-	37	-	ns
$t_f$	Fall time		-	22	-	ns

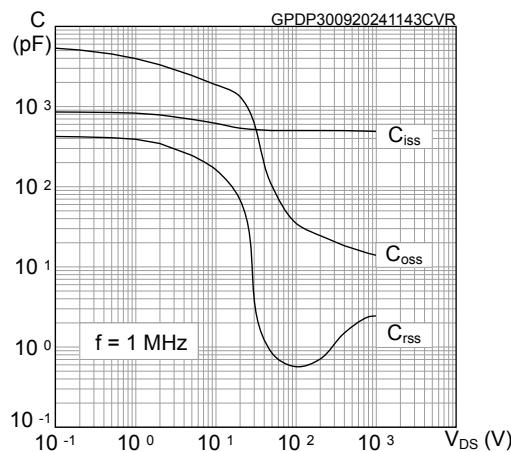
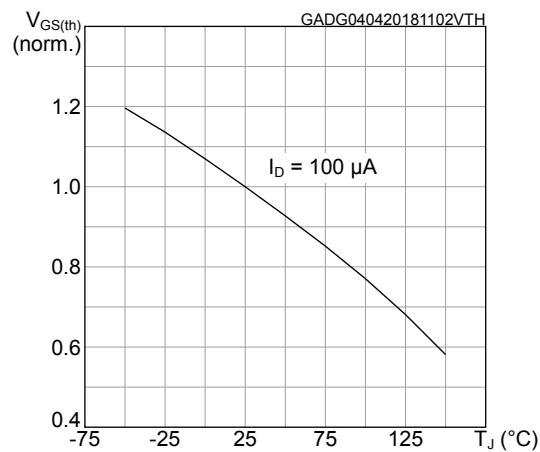
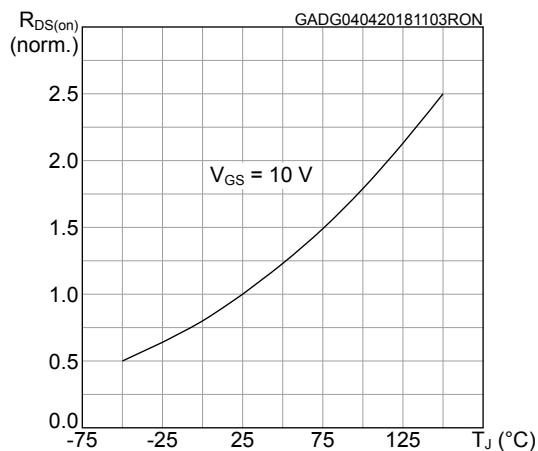
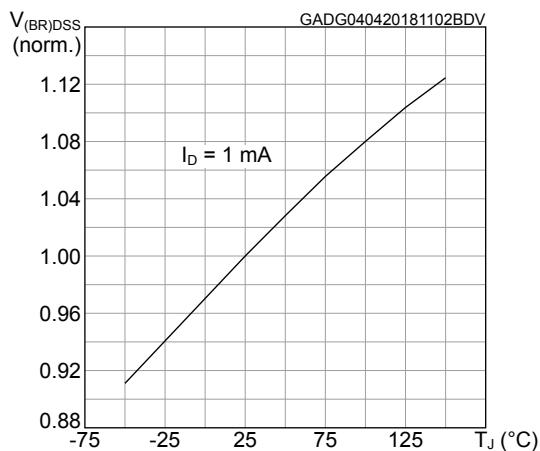
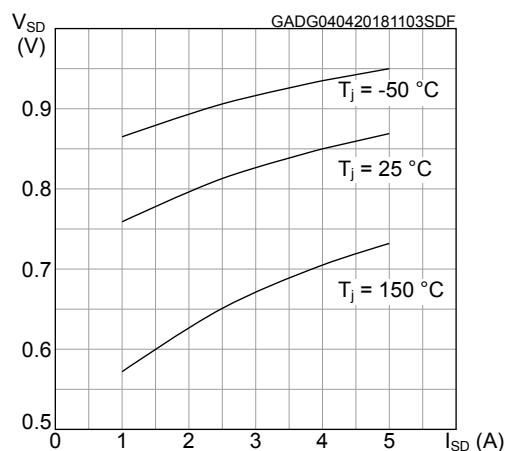
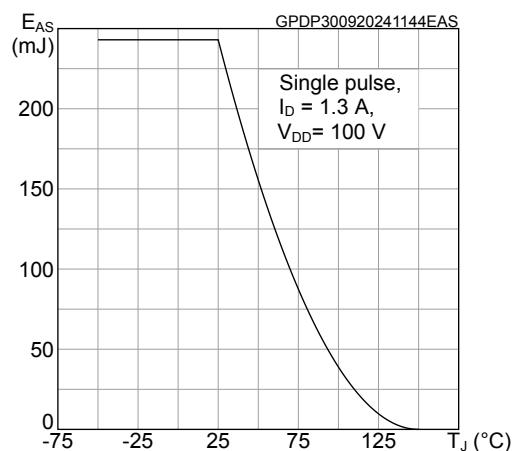
**Table 7. Source-drain diode**

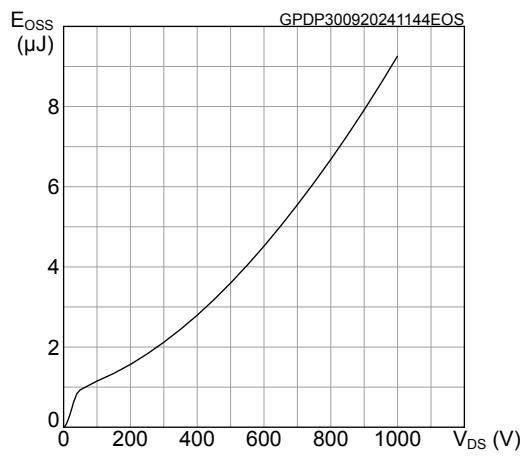
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		6	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		12	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 5 \text{ A}, V_{GS} = 0 \text{ V}$	-		1.5	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 5 \text{ A}, dI/dt = 100 \text{ A}/\mu\text{s}$ ,	-	553		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 60 \text{ V}$ (see Figure 16. Test circuit for inductive load switching and diode recovery times)	-	6		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current	$I_{SD} = 5 \text{ A}, dI/dt = 100 \text{ A}/\mu\text{s}$ , (see Figure 16. Test circuit for inductive load switching and diode recovery times)	-	16		A
$t_{rr}$	Reverse recovery time	$V_{DD} = 60 \text{ V}, T_J = 150 \text{ }^\circ\text{C}$	-	865		ns
$Q_{rr}$	Reverse recovery charge		-	8.2		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	15		A

1. Pulse width is limited by safe operating area.
2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%.

## 2.1 Electrical characteristics (curves)

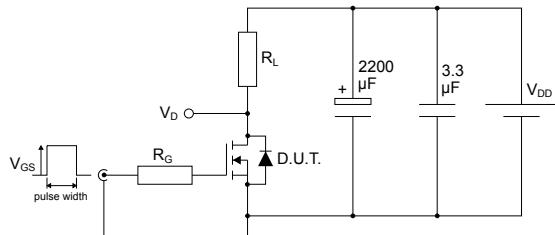
**Figure 1. Safe operating area**

**Figure 2. Maximum transient thermal impedance**

**Figure 3. Typical output characteristics**

**Figure 4. Typical transfer characteristics**

**Figure 5. Typical gate charge characteristics**

**Figure 6. Typical drain-source on-resistance**


**Figure 7. Typical capacitance characteristics**

**Figure 8. Normalized gate threshold vs temperature**

**Figure 9. Normalized on-resistance vs temperature**

**Figure 10. Normalized breakdown voltage vs temperature**

**Figure 11. Typical reverse diode forward characteristics**

**Figure 12. Maximum avalanche energy vs temperature**


**Figure 13. Typical output capacitance stored energy**

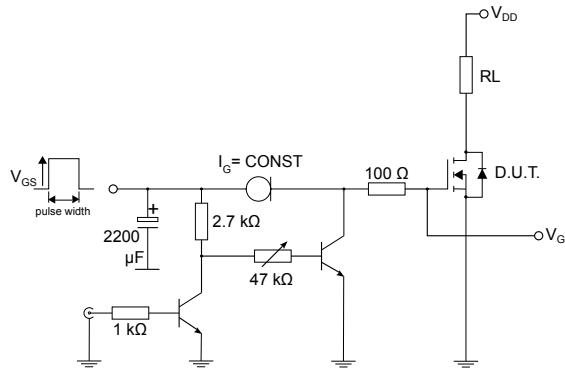
### 3 Test circuits

**Figure 14.** Test circuit for resistive load switching times



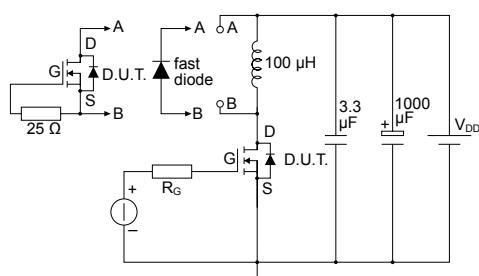
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**Figure 15.** Test circuit for gate charge behavior



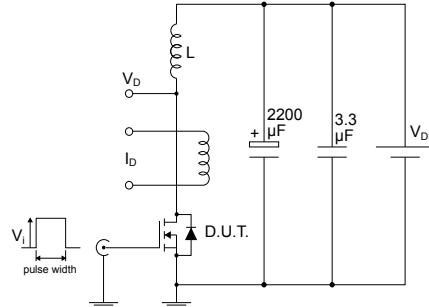
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**Figure 16.** Test circuit for inductive load switching and diode recovery times



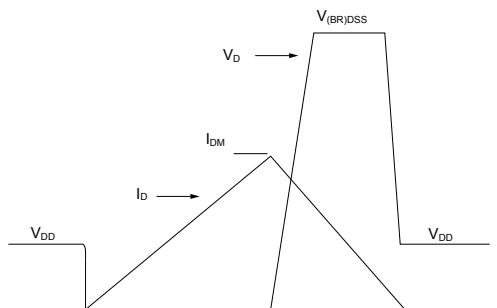
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**Figure 17.** Unclamped inductive load test circuit



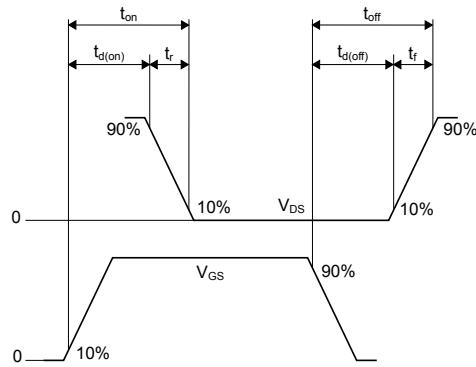
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**Figure 18.** Unclamped inductive waveform



AM01472v1

**Figure 19.** Switching time waveform



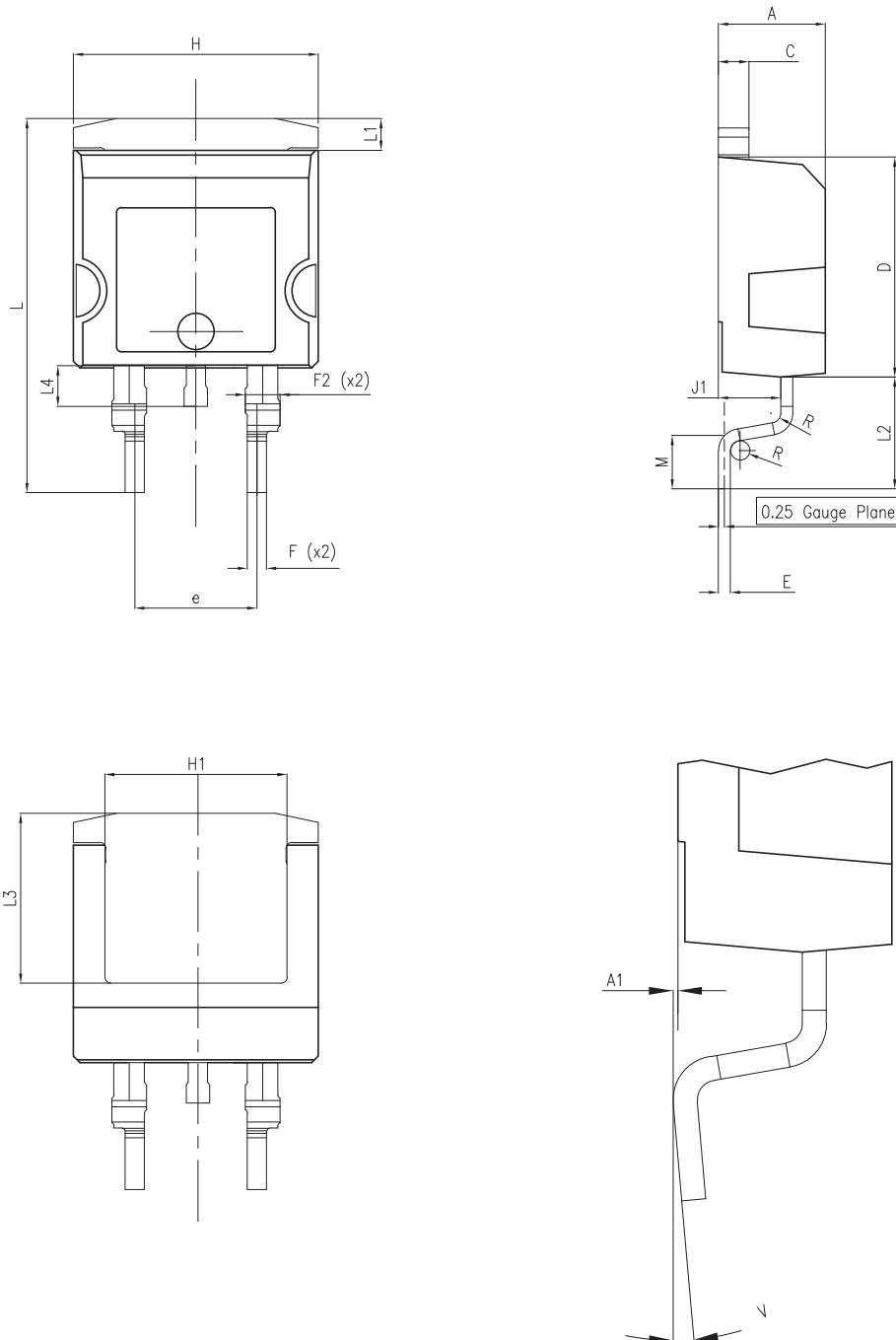
AM01473v1

## 4 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

### 4.1 H<sup>2</sup>PAK-2 package information

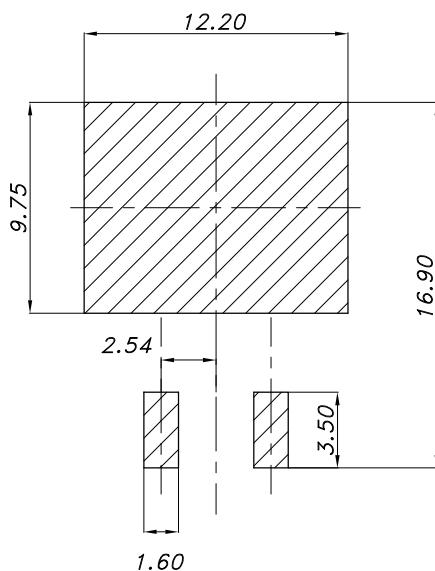
Figure 20. H<sup>2</sup>PAK-2 package outline



8159712\_10

**Table 8.** H<sup>2</sup>PAK-2 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.30		4.70
A1	0.03		0.20
C	1.17		1.37
D	8.95		9.35
e	4.98		5.18
E	0.50		0.90
F	0.78		0.85
F2	1.14		1.70
H	10.00		10.40
H1	7.40	-	7.80
J1	2.49		2.69
L	15.30		15.80
L1	1.27		1.40
L2	4.93		5.23
L3	6.85		7.25
L4	1.50		1.70
M	2.60		2.90
R	0.20		0.60
V	0°		8°

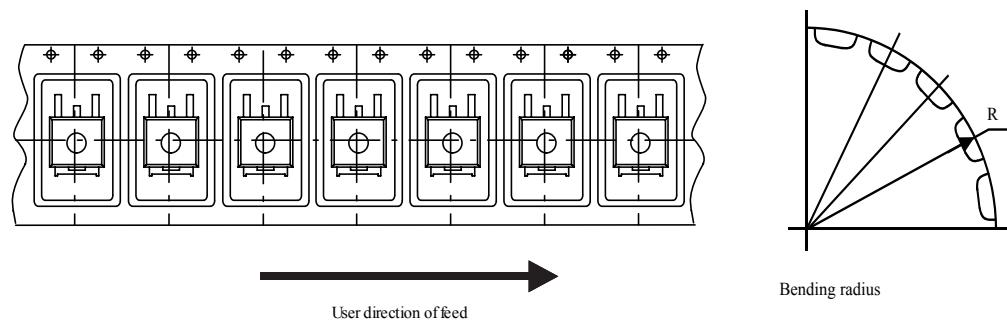
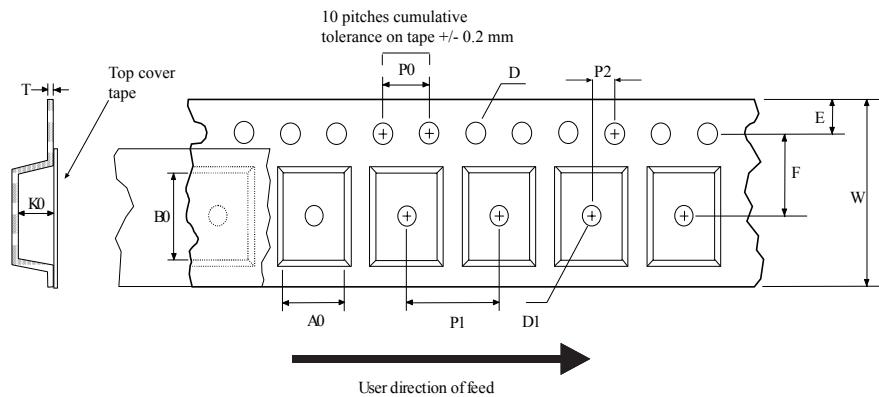
**Figure 21.** H<sup>2</sup>PAK-2 recommended footprint

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**Note:** Dimensions are in mm.

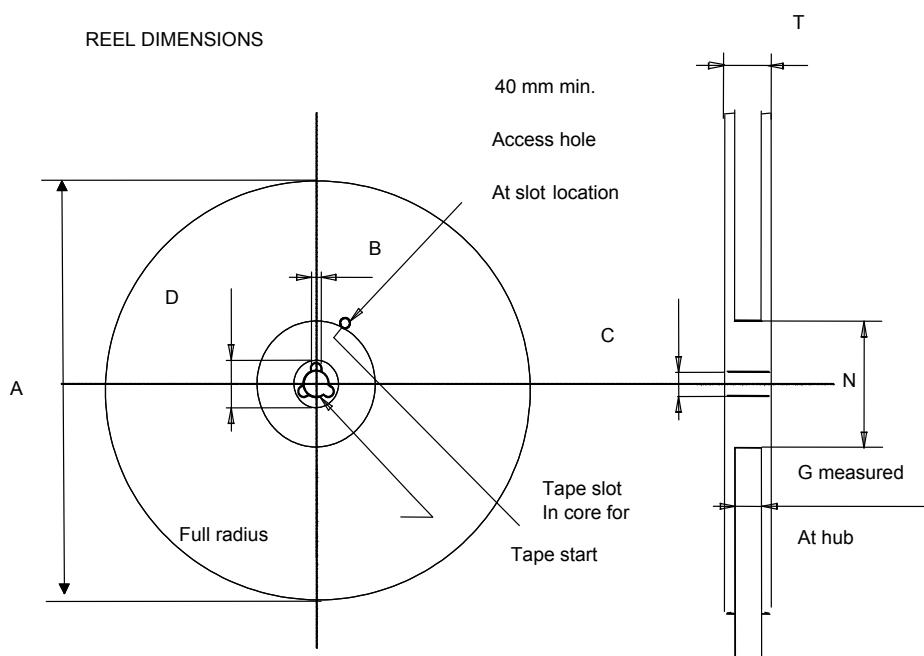
## 4.2 Packing information

**Figure 22. Tape outline**



AM08852v2

**Figure 23. Reel outline**



**Table 9. Tape and reel mechanical data**

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1		Base quantity	1000
P2	1.9	2.1		Bulk quantity	1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

## Revision history

**Table 10. Document revision history**

Date	Revision	Changes
07-Oct-2024	1	First release.

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