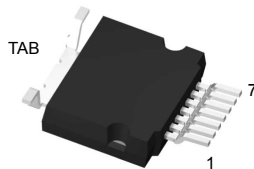
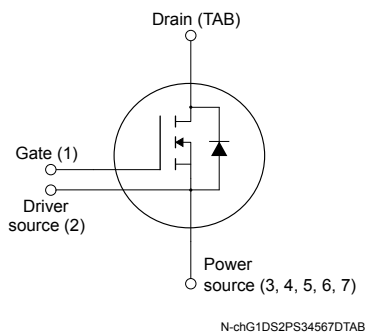


Automotive-grade N-channel 650 V, 38 mΩ typ., 51 A MDmesh DM9 Power MOSFET in an HU3PAK package




HU3PAK



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STHU65N050DM9AG	650 V	50 mΩ	51 A

- AEC-Q101 qualified 
- Fast-recovery body diode
- Very low FOM ($R_{DS(on)} \cdot Q_g$)
- Low gate charge, input capacitance and resistance
- 100% avalanche tested
- Extremely high dv/dt ruggedness
- Excellent switching performance thanks to the extra driving source pin

Applications

- High efficiency switching applications

Description

This N-channel Power MOSFET is based on the most innovative super-junction MDmesh DM9 technology, suitable for medium/high voltage MOSFETs featuring very low $R_{DS(on)}$ per area coupled with a fast-recovery diode. The silicon-based DM9 technology benefits from a multi-drain manufacturing process which allows an enhanced device structure. The fast-recovery diode featuring very low recovery charge (Q_{rr}), time (t_{rr}) and $R_{DS(on)}$ makes this fast-switching super-junction Power MOSFET tailored for the most demanding high-efficiency bridge topologies and ZVS phase-shift converters.

Product status link

[STHU65N050DM9AG](#)

Product summary

Order code	STHU65N050DM9AG
Marking	65A050DM9
Package	HU3PAK
Packing	Tape and reel

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 30	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	51	A
	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	32	
$I_{DM}^{(2)}$	Drain current (pulsed)	220	A
P_{TOT}	Total power dissipation at $T_C = 25\text{ }^\circ\text{C}$	245	W
$dv/dt^{(3)}$	Peak diode recovery voltage slope	120	V/ns
$di/dt^{(3)}$	Peak diode recovery current slope	1000	A/ μs
$dv/dt^{(4)}$	MOSFET dv/dt ruggedness	120	V/ns
T_{stg}	Storage temperature range	-55 to 150	$^\circ\text{C}$
T_J	Operating junction temperature range		$^\circ\text{C}$

1. Referred to TO-247 long leads package.
2. Pulse width limited by safe operating area.
3. $I_{SD} \leq 25.5\text{ A}$, $V_{DS} (\text{peak}) < V_{(BR)DSS}$, $V_{DD} = 400\text{ V}$.
4. $V_{DS} (\text{peak}) < V_{(BR)DSS}$, $V_{DD} = 400\text{ V}$.

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	0.51	$^\circ\text{C/W}$
$R_{thJA}^{(1)}$	Thermal resistance, junction-to-ambient	30	$^\circ\text{C/W}$

1. When mounted on a standard 1 inch² area of FR-4 PCB with 2-oz copper.

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T_J max.)	6	A
E_{AS}	Single pulse avalanche energy (starting $T_J = 25\text{ }^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	760	mJ

2 Electrical characteristics

$T_C = 25\text{ °C}$ unless otherwise specified.

Table 4. On/off-states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$, $I_D = 1\text{ mA}$	650			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = 650\text{ V}$			5	μA
I_{GSS}	Gate-body leakage current	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 25\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	3.5	4.0	4.5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 25.5\text{ A}$		38	50	m Ω

Table 5. Dynamic characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 400\text{ V}$, $f = 250\text{ kHz}$, $V_{GS} = 0\text{ V}$	-	4680	-	pF
C_{oss}	Output capacitance		-	76	-	pF
$C_{oss\ eq}^{(1)}$	Equivalent output capacitance	$V_{DS} = 0\text{ to }400\text{ V}$, $V_{GS} = 0\text{ V}$	-	1070	-	pF
R_g	Intrinsic gate resistance	$f = 250\text{ kHz}$, open drain	-	1	-	Ω
Q_g	Total gate charge	$V_{DD} = 400\text{ V}$, $I_D = 25.5\text{ A}$, $V_{GS} = 0\text{ to }10\text{ V}$ (see Figure 14. Test circuit for gate charge behavior)	-	100	-	nC
Q_{gs}	Gate-source charge		-	26	-	nC
Q_{gd}	Gate-drain charge		-	36	-	nC

1. $C_{oss\ eq}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to stated value.

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 400\text{ V}$, $I_D = 25.5\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$	-	29	-	ns
t_r	Rise time		-	7	-	ns
$t_{d(off)}$	Turn-off delay time	(see Figure 13. Switching times test circuit for resistive load and Figure 18. Switching time waveform)	-	80	-	ns
t_f	Fall time		-	5	-	ns

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}^{(1)}$	Source-drain current		-		51	A
$I_{SDM}^{(2)}$	Source-drain current (pulsed)		-		220	A
$V_{SD}^{(3)}$	Forward on voltage	$V_{GS} = 0\text{ V}$, $I_{SD} = 51\text{ A}$	-	1.1	1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 51\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$,	-	170		ns
Q_{rr}	Reverse recovery charge	$V_{DD} = 150\text{ V}$	-	1.2		μC
I_{RRM}	Reverse recovery current	(see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	12		A
t_{rr}	Reverse recovery time	$I_{SD} = 51\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$,	-	225		ns
Q_{rr}	Reverse recovery charge	$V_{DD} = 150\text{ V}$, $T_J = 150\text{ }^\circ\text{C}$	-	2.2		μC
I_{RRM}	Reverse recovery current	(see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	18		A

1. Referred to TO-247 long leads package.
2. Pulse width is limited by safe operating area.
3. Pulsed: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

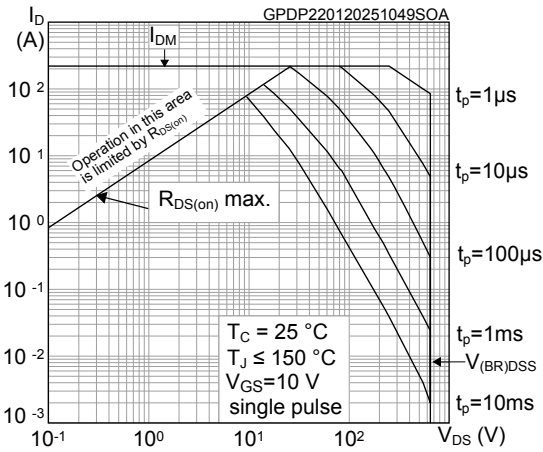


Figure 2. Maximum transient thermal impedance

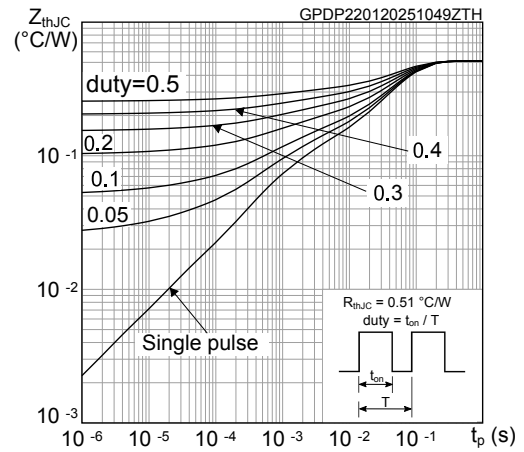


Figure 3. Typical output characteristics

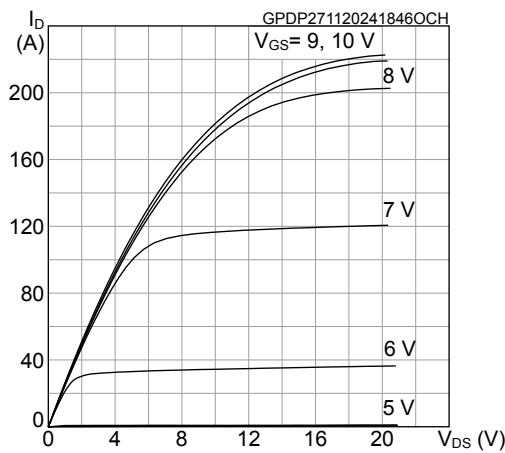


Figure 4. Typical transfer characteristics

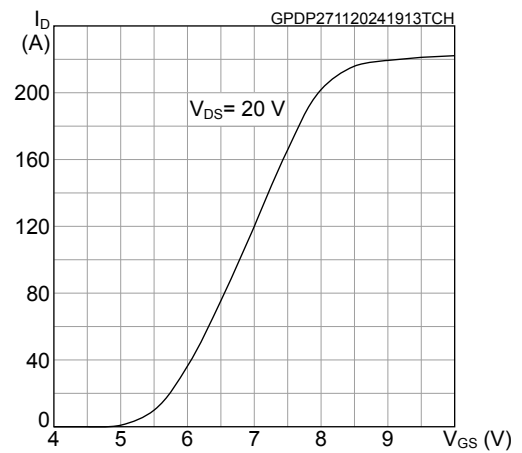


Figure 5. Typical gate charge characteristics

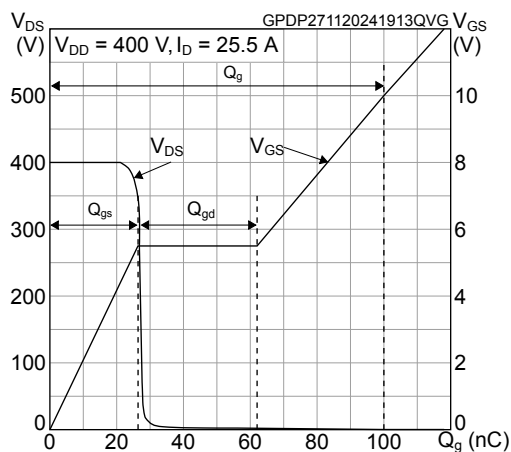


Figure 6. Typical capacitance characteristics

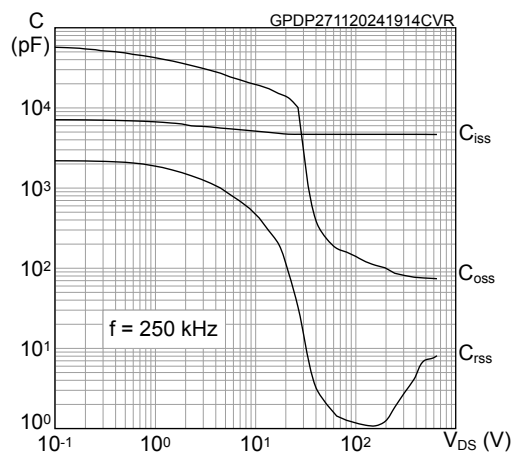


Figure 7. Typical drain-source on-resistance

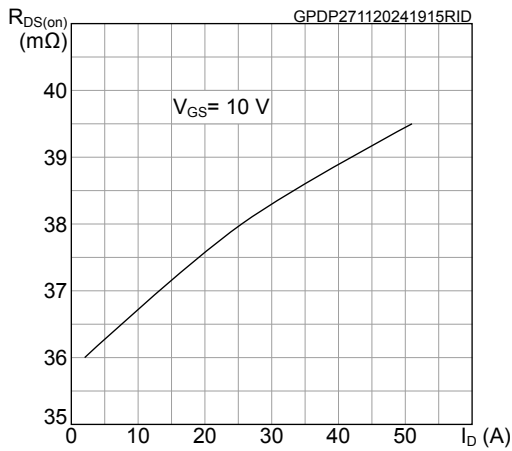


Figure 8. Normalized on-resistance vs temperature

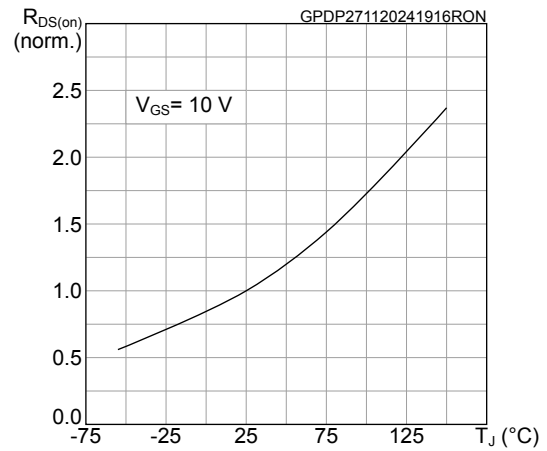


Figure 9. Normalized gate threshold vs temperature

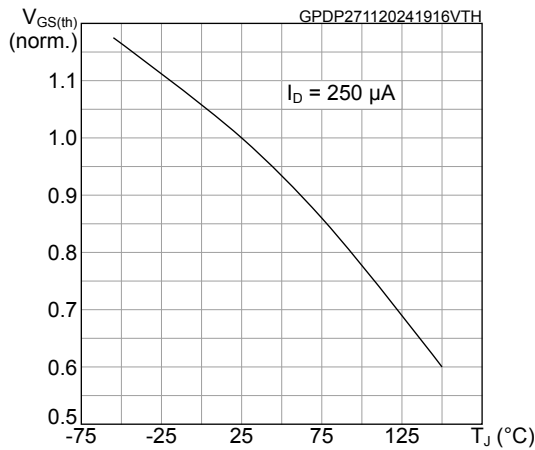


Figure 10. Normalized breakdown voltage vs temperature

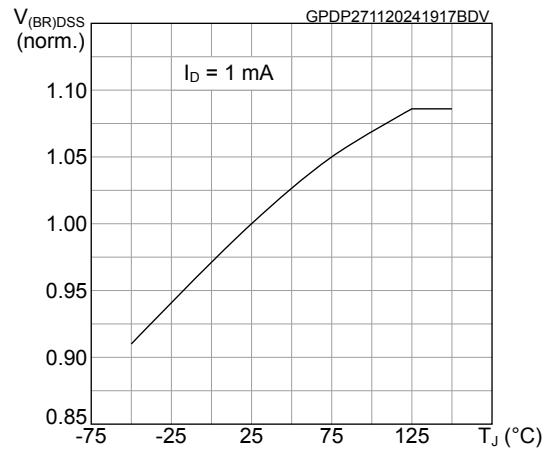


Figure 11. Typical reverse diode forward characteristics

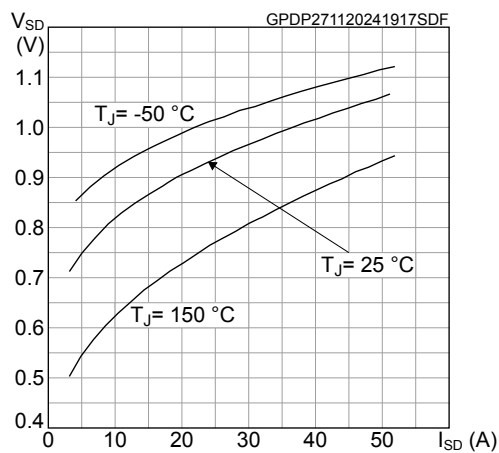
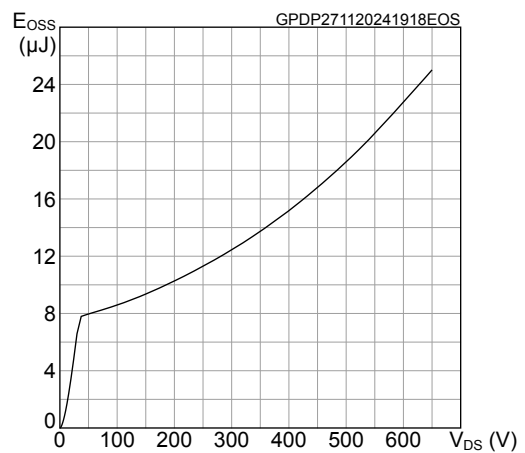
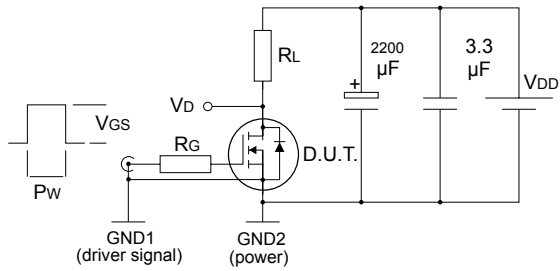


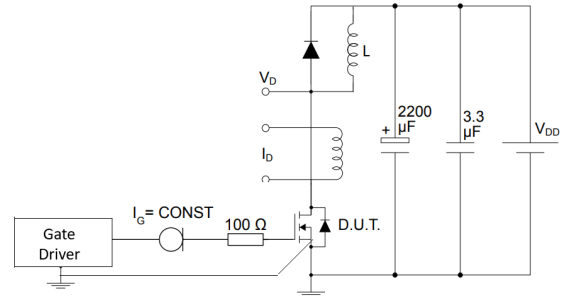
Figure 12. Typical output capacitance stored energy



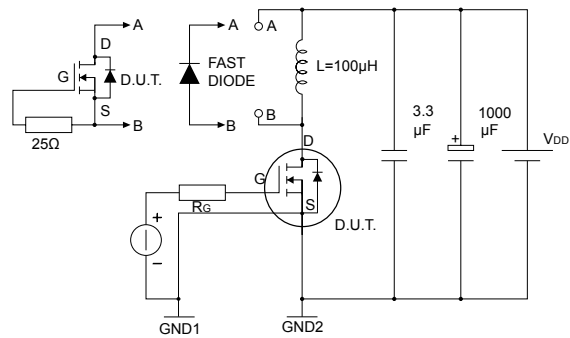
3 Test circuits

Figure 13. Switching times test circuit for resistive load


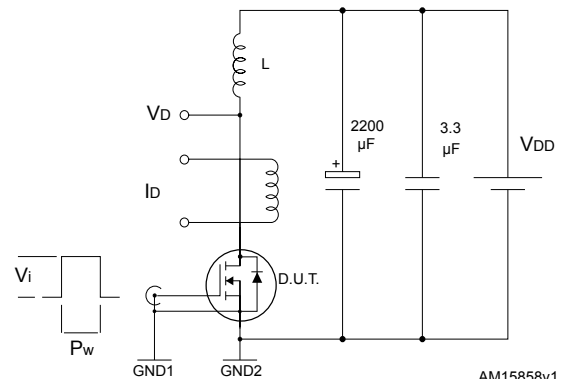
AM15855v1

Figure 14. Test circuit for gate charge behavior


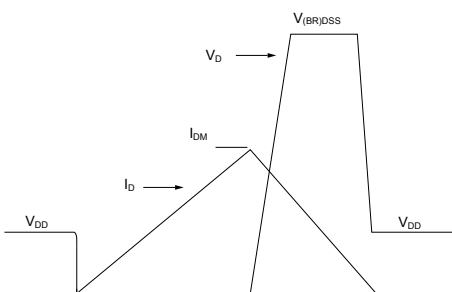
GDPDP191120241113SA

Figure 15. Test circuit for inductive load switching and diode recovery times


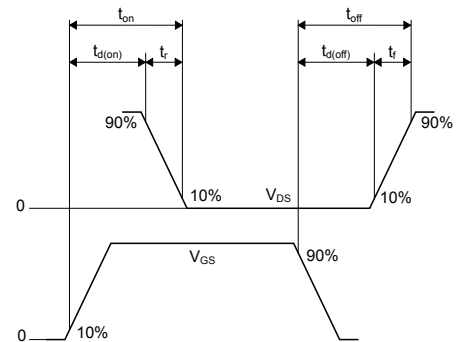
AM15857v1

Figure 16. Unclamped inductive load test circuit


AM15858v1

Figure 17. Unclamped inductive waveform


AM01472v1

Figure 18. Switching time waveform


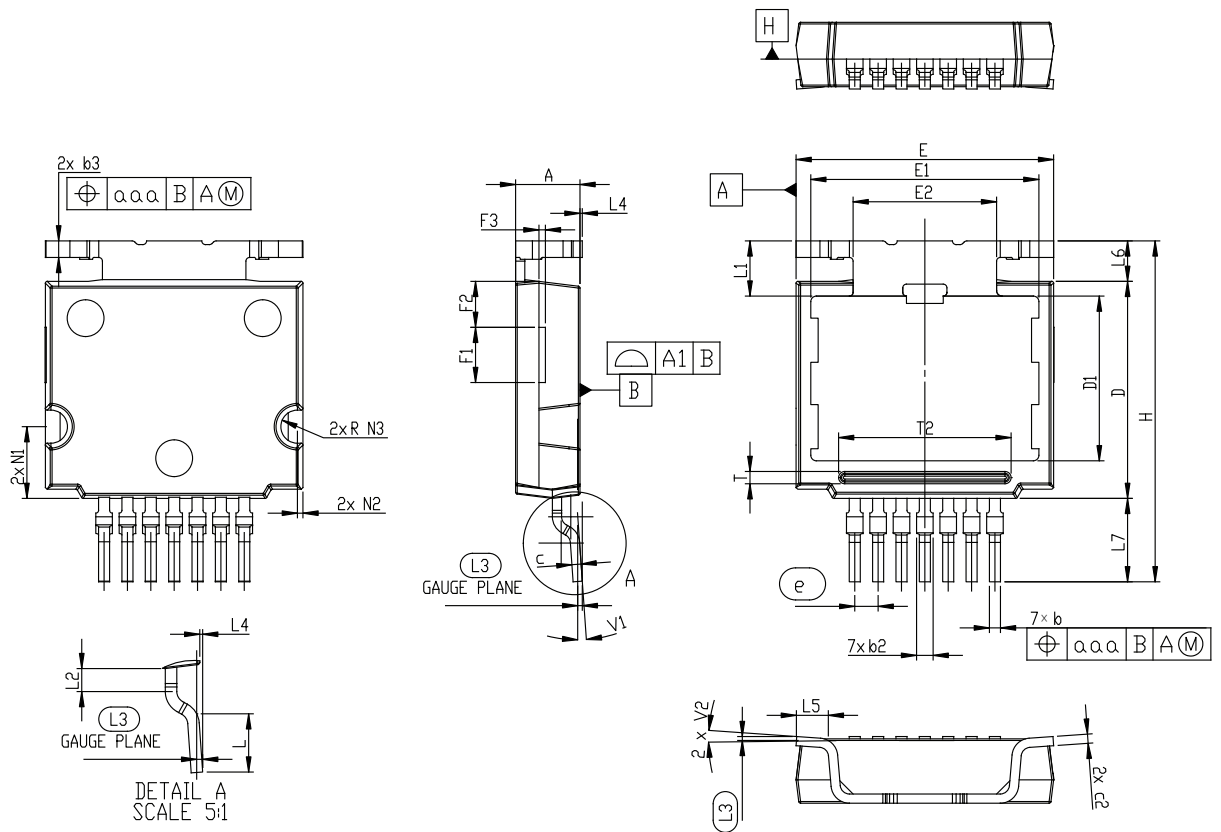
AM01473v1

4 Package information

To meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 HU3PAK package information

Figure 19. HU3PAK package outline

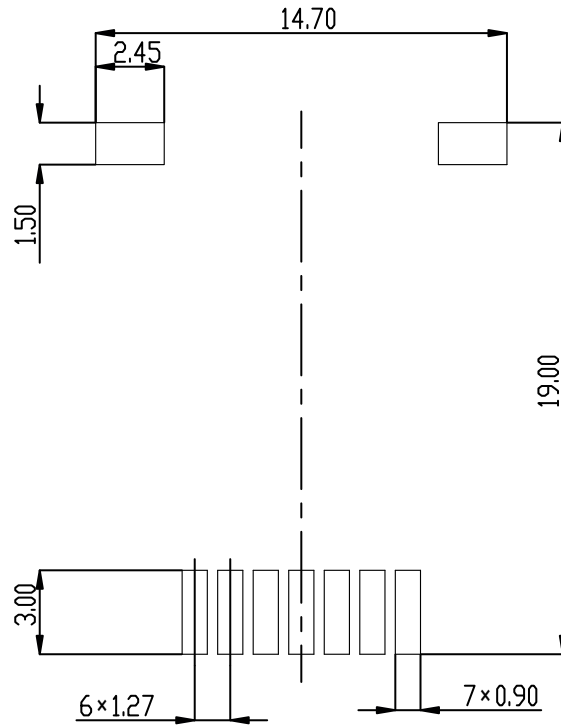


DM00674007_2

Table 8. HU3PAK package mechanical data

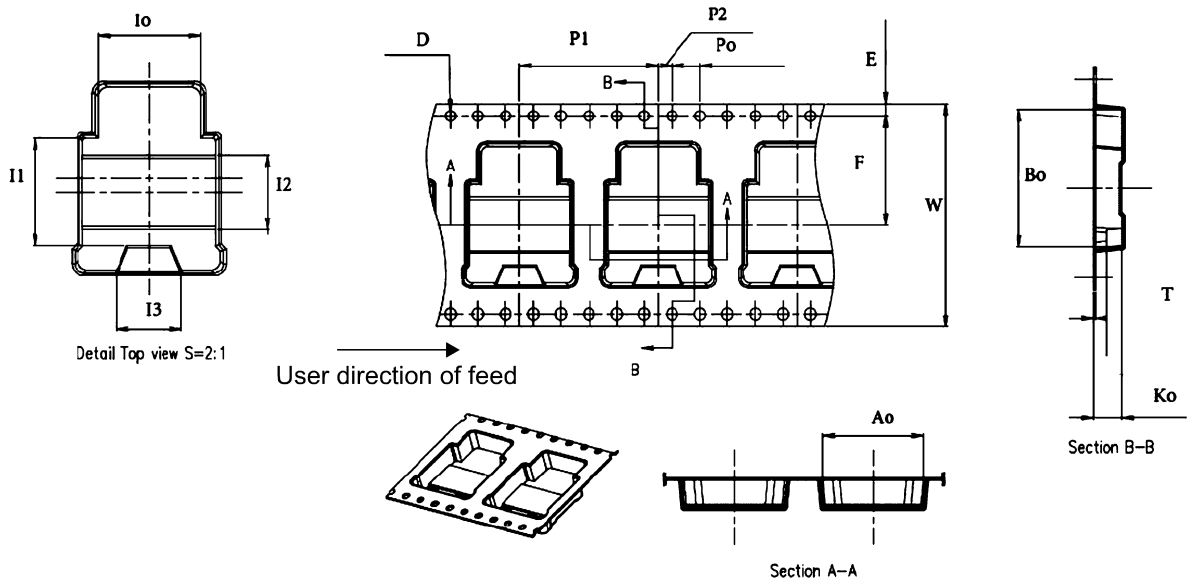
Ref.	Dimensions		
	mm		
	Min.	Typ.	Max.
A	3.40	3.50	3.60
A1		0.05	
b	0.50	0.60	0.70
b2	0.50	0.70	1.00
b3	0.80	0.90	1.00
c	0.40	0.50	0.60
c2	0.40	0.50	0.60
D	11.70	11.80	11.90
D1	8.80	8.955	9.10
E	13.90	14.00	14.10
E1	12.30	12.40	12.50
E2	7.75	7.80	7.85
e		1.27	
H	18.00	18.58	19.00
aaa		0.10	
L	2.40	2.52	2.60
L1		3.05	
L2	0.90	1.00	1.10
L3		0.26	
L4	0.075	0.125	0.175
L5	1.83	1.93	2.03
L6	2.14	2.24	2.34
L7	4.44	4.54	4.64
F1	2.90	3.00	3.10
F2	2.40	2.50	2.60
F3	0.25	0.35	0.45
N1	3.80	3.90	4.00
N2	0.25	0.30	0.45
N3	0.80	0.90	1.00
T	0.50	0.67	0.70
T2	9.18	9.38	9.43
V1		0°	8°
V2		0°	8°

Figure 20. HU3PAK recommended footprint (dimensions in mm)



4.2 HU3PAK packing information

Figure 21. HU3PAK carrier tape outline



DM00345054_3

Revision history

Table 10. Document revision history

Date	Revision	Changes
18-Jun-2024	1	First release.
23-Jan-2025	2	Updated Features. Updated Table 1. Absolute maximum ratings and added Table 3. Avalanche characteristics. Updated Section 2: Electrical characteristics. Updated Section 2.1: Electrical characteristics (curves).

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