STI175N4F6AG

Automotive-grade N-channel 40 V, 2.1 mΩ typ., 120 A STripFET™ F6 Power MOSFET in an I²PAK package

Datasheet - production data

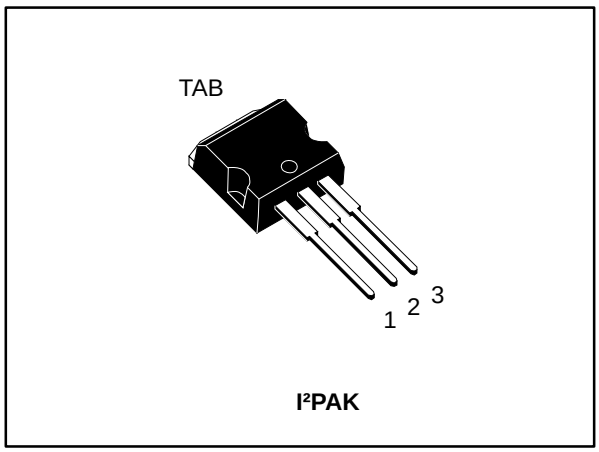
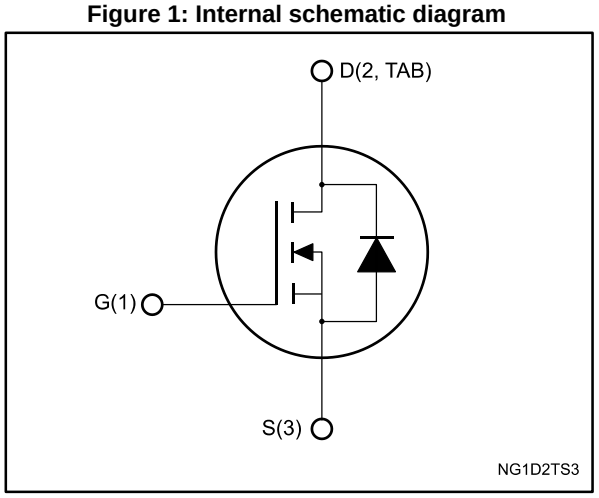


Figure 1: Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D	P_{TOT}
STI175N4F6AG	40 V	2.7 mΩ	120 A	190 W

- Designed for automotive applications and AEC-Q101 qualified
- Very low on-resistance
- Very low gate charge
- High avalanche ruggedness
- Low gate drive power loss

Applications

- Switching applications
- Power tools

Description

This device is an N-channel Power MOSFET developed using the STripFET™ F6 technology with a new trench gate structure. The resulting Power MOSFET exhibits very low $R_{DS(on)}$ in all packages.

Table 1: Device summary

Order code	Marking	Package	Packing
STI175N4F6AG	175N4F6	I²PAK	Tube

Contents

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	40	V
V_{GS}	Gate-source voltage	±20	V
I_D(1)	Drain current (continuous) at T_{case} = 25 °C	120	A
	Drain current (continuous) at T_{case} = 100 °C	120	
I_{DM}(2)	Drain current (pulsed)	480	A
P_{TOT}	Total dissipation at T_{case} = 25 °C	190	W
T_{stg}	Storage temperature range	-55 to 175	°C
T_j	Operating junction temperature range		

Notes:

(1) Limited by package

(2)Pulse width limited by safe operating area.

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case	0.79	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-amb	62.5	

2 Electrical characteristics

(T_{case} = 25 °C unless otherwise specified)

Table 4: Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	40			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 40 V			1	µA
		V_{GS} = 0 V, V_{DS} = 40 V, T_{case} = 125 °C			100	
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	3		4.5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 60 A		2.1	2.7	mΩ

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 20 V, f = 1 MHz, V_{GS} = 0 V	-	7735	-	pF
C_{oss}	Output capacitance		-	745	-	
C_{rss}	Reverse transfer capacitance		-	560	-	
Q_g	Total gate charge	V_{DD} = 20 V, I_D = 120 A, V_{GS} = 10 V (see *Figure 14: "Test circuit for gate charge behavior"*)	-	130	-	nC
Q_{gs}	Gate-source charge		-	36	-	
Q_{gd}	Gate-drain charge		-	42	-	

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 20 V, I_D = 60 A R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 13: "Test circuit for resistive load switching times"* and *Figure 18: "Switching time waveform"*)	-	24	-	ns
t_r	Rise time		-	150	-	
$t_{d(off)}$	Turn-off delay time		-	106	-	
t_f	Fall time		-	57	-	

Table 7: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}(1)	Source-drain current		-		120	A
I_{SDM}(2)	Source-drain current (pulsed)		-		480	A
V_{SD}(2)	Forward on voltage	V_{GS} = 0 V, I_{SD} = 120 A	-		1.3	V
t_{rr}	Reverse recovery time	I_{SD} = 120 A, di/dt = 100 A/µs, V_{DD} = 32 V (see *Figure 15: "Test circuit for inductive load switching and diode recovery times"*)	-	36		ns
Q_{rr}	Reverse recovery charge		-	40		nC
I_{RRM}	Reverse recovery current		-	2.3		A

Notes:

(1) Limited by package.

(2) Pulse test: pulse duration = 300 µs, duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 2: Safe operating area

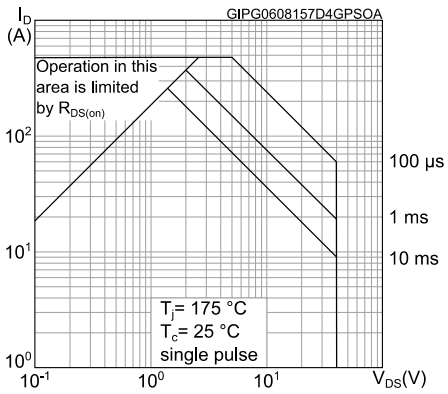


Figure 3: Thermal impedance

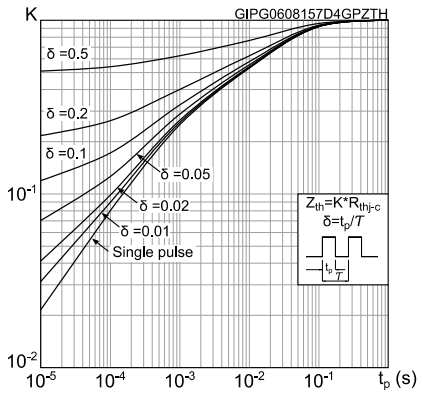


Figure 4: Output characteristics

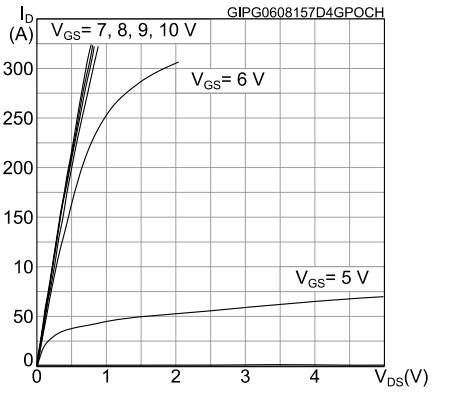


Figure 5: Transfer characteristics

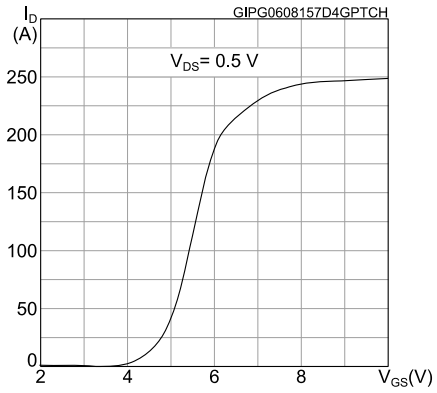


Figure 6: Gate charge vs gate-source voltage

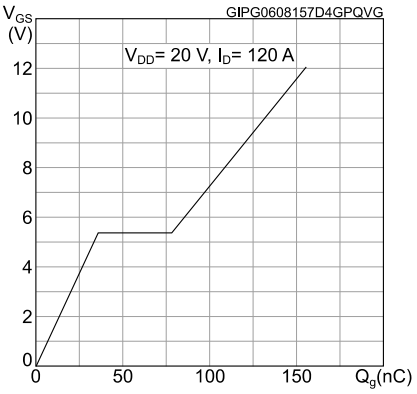


Figure 7: Static drain-source on-resistance

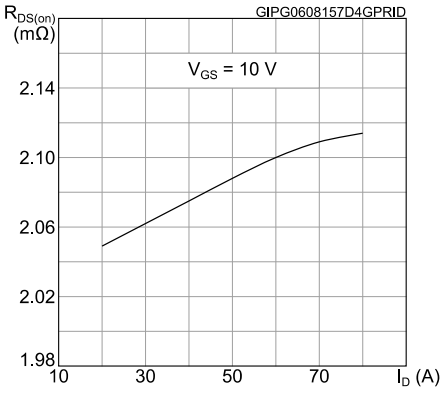


Figure 8: Capacitance variations

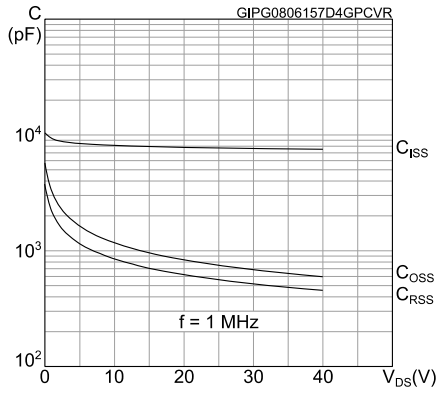


Figure 9: Normalized gate threshold voltage vs temperature

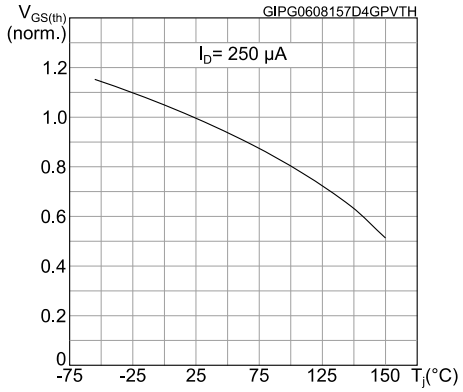


Figure 10: Normalized on-resistance vs temperature

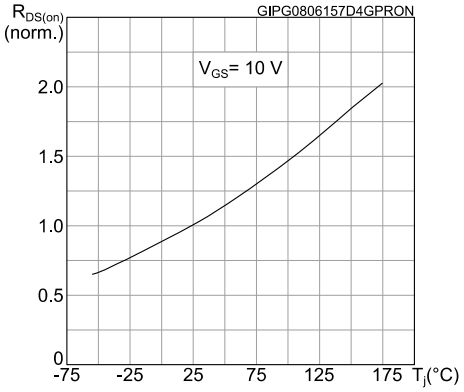


Figure 11: Normalized V(BR)DSS vs temperature

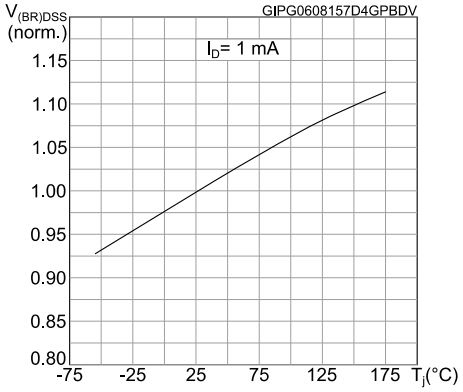
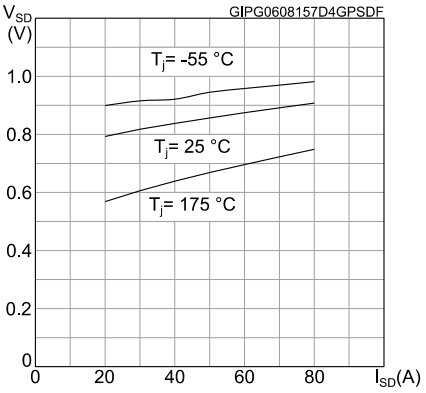


Figure 12: Source-drain diode forward characteristics



3 Test circuits

Figure 13: Test circuit for resistive load switching times

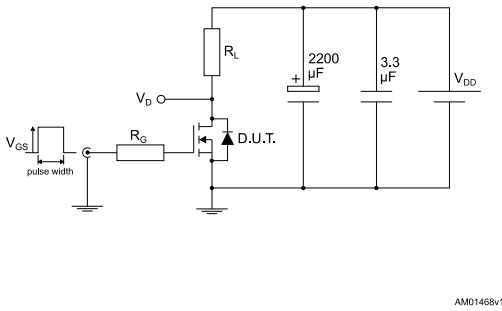


Figure 14: Test circuit for gate charge behavior

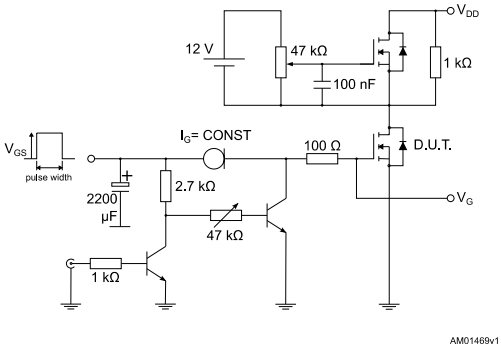


Figure 15: Test circuit for inductive load switching and diode recovery times

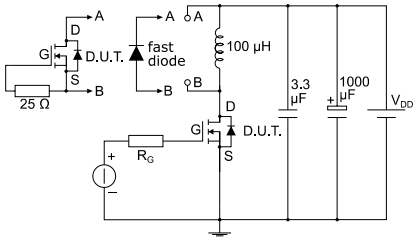


Figure 16: Unclamped inductive load test circuit

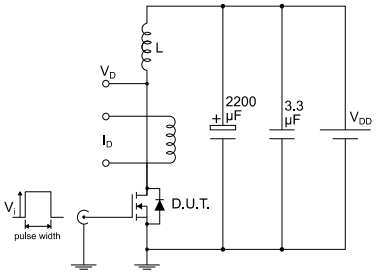


Figure 17: Unclamped inductive waveform

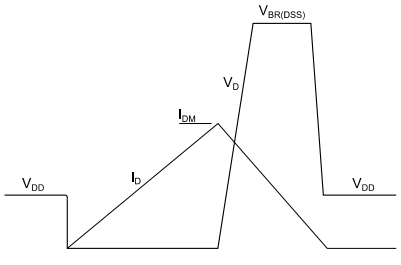
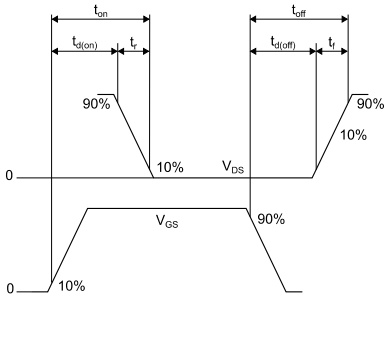


Figure 18: Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

4.1 I²PAK package information

Figure 19: I²PAK package outline

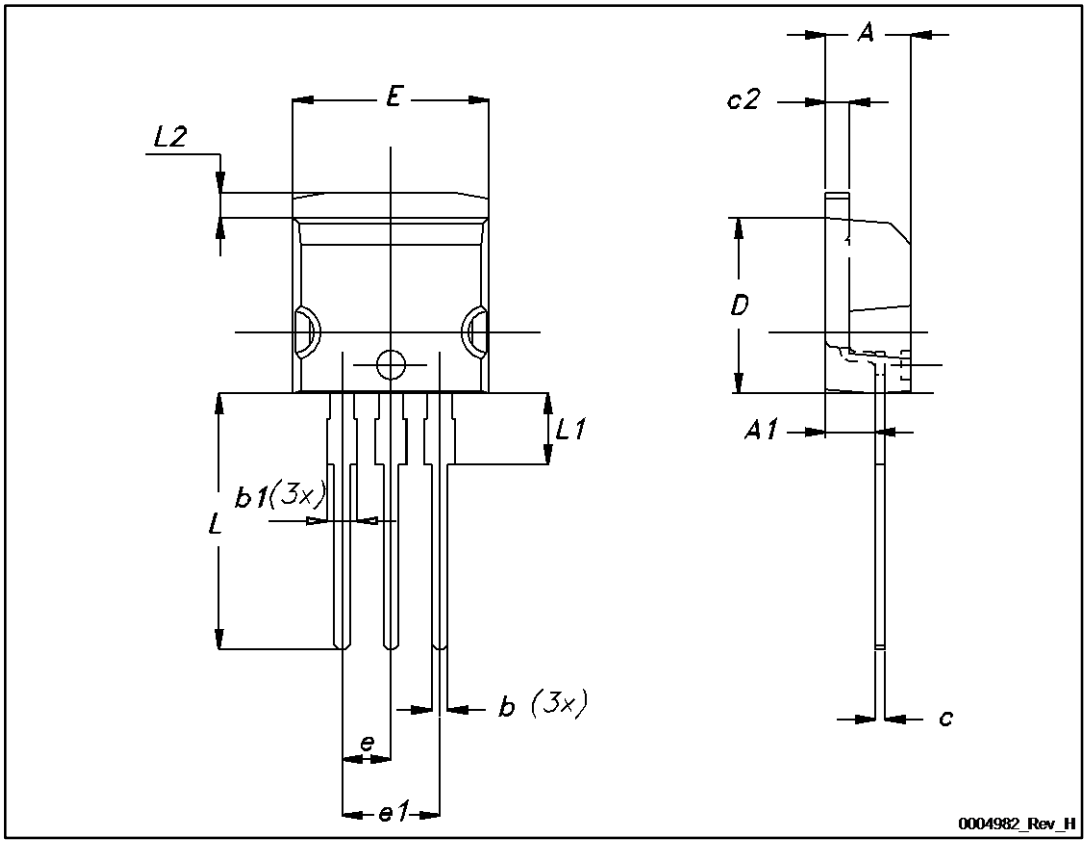


Table 8: I²PAK package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40	–	4.60
A1	2.40	–	2.72
b	0.61	–	0.88
b1	1.14	–	1.70
c	0.49	–	0.70
c2	1.23	–	1.32
D	8.95	–	9.35
e	2.40	–	2.70
e1	4.95	–	5.15
E	10	–	10.40
L	13	–	14
L1	3.50	–	3.93
L2	1.27	–	1.40

5 Revision history

Table 9: Document revision history

Date	Revision	Changes
26-Jan-2016	1	First release.

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