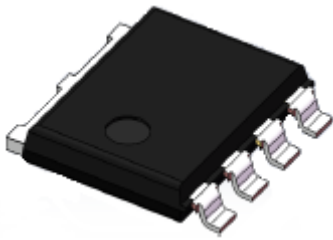
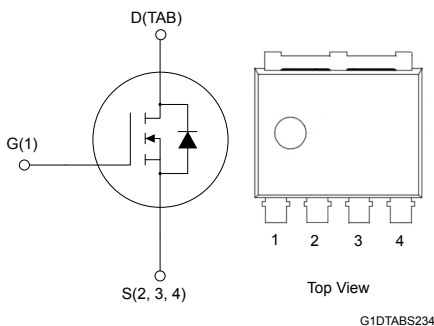


## Automotive N-channel 40 V, 0.48 mΩ max., 672 A STripFET F8 Power MOSFET in a PowerLeaded 8x8 package




PowerLeaded 8x8



### Features

Order code	$V_{DS}$	$R_{DS(on)}$ max.	$I_D$
STK615N4F8AG	40 V	0.48 mΩ at 10 V	672 A

- AEC-Q101 qualified 
- MSL1 grade
- 175 °C maximum operating junction temperature
- 100% avalanche tested
- Low gate charge  $Q_g$

### Applications

- Automotive motor control
- Body and convenience
- Chassis and safety
- Power train for ICE

### Description

The **STK615N4F8AG** is a 40 V N-channel enhancement mode Power MOSFET designed in STripFET F8 technology featuring an enhanced trench gate structure.

It ensures a state-of-the-art of figure of merit for very low on-state resistance while reducing internal capacitances and gate charge for faster and more efficient switching.



#### Product status link

[STK615N4F8AG](#)

#### Product summary

Order code	STK615N4F8AG
Marking <sup>(1)</sup>	615N4F8
Package	PowerLeaded 8x8
Packing	Tape and reel

1. Engineering samples are clearly identified with a dedicated special symbol in the marking of each unit.

# 1 Electrical ratings

**Table 1. Absolute maximum ratings (at  $T_C = 25\text{ °C}$  unless otherwise specified)**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	40	V
$V_{GS}$	Gate-source voltage	$\pm 20$	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ °C}^{(2)}$	672	A
	Drain current (continuous) at $T_C = 100\text{ °C}^{(2)}$	475	
	Drain current (continuous) at $T_C = 25\text{ °C}^{(3)}$	200	
$I_{DM}^{(1)(2)(4)}$	Drain current (pulsed), $t_p = 10\text{ }\mu\text{s}$	2688	A
$P_{TOT}$	Total power dissipation at $T_C = 25\text{ °C}$	390	W
$I_{AS}$	Single pulse avalanche current (pulse width limited by $T_J$ max.)	90	A
$E_{AS}$	Single pulse avalanche energy (starting $T_J = 25\text{ °C}$ , $I_D = 90\text{ A}$ , $R_{Gmin} = 25\text{ }\Omega$ )	1779	mJ
$T_J$	Operating junction temperature range	-55 to 175	$^{\circ}\text{C}$
$T_{stg}$	Storage temperature range		$^{\circ}\text{C}$

1. Specified by design, not tested in production.
2. This is the theoretical current value only related to the silicon.
3. This current value is limited by package.
4. Pulse width is limited by safe operating area.

**Table 2. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thJA}^{(1)}$	Thermal resistance, junction-to-ambient (on 2s2p FR-4 board vertical in still area)	13.8	$^{\circ}\text{C/W}$
$R_{thJC}$	Thermal resistance, junction-to-case	0.39	$^{\circ}\text{C/W}$

1. Defined according to JEDEC standards (JESD51-5, -7).

## 2 Electrical characteristics

$T_J = 25\text{ °C}$  unless otherwise specified.

**Table 3. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}$	40			V
$I_{DSS}$	Zero gate voltage drain current	$V_{DS} = 40\text{ V}, V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
		$V_{DS} = 40\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ °C}^{(1)}$			100	
$I_{GSS}$	Gate-body leakage current	$V_{GS} = 20\text{ V}, V_{DS} = 0\text{ V}$			100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2		4	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}, I_D = 90\text{ A}$		0.35	0.48	m $\Omega$

1. Specified by design and evaluated by characterization, not tested in production.

**Table 4. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}^{(1)}$	Input capacitance	$V_{DS} = 25\text{ V}, f = 1\text{ MHz}, V_{GS} = 0\text{ V}$	-	13000	-	pF
$C_{oss}^{(1)}$	Output capacitance		-	3400	-	pF
$C_{rss}^{(1)}$	Reverse transfer capacitance		-	85	-	pF
$Q_g^{(1)}$	Total gate charge	$V_{DD} = 20\text{ V}, I_D = 180\text{ A}, V_{GS} = 0\text{ to }10\text{ V}$	-	162	-	nC
$Q_{gs}^{(1)}$	Gate-source charge		-	62	-	nC
$Q_{gd}^{(1)}$	Gate-drain charge		-	20	-	nC

1. Specified by design and evaluated by characterization, not tested in production.

**Table 5. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}^{(1)}$	Turn-on delay time	$V_{DD} = 20\text{ V}, I_D = 90\text{ A}, R_G = 4.7\text{ }\Omega, V_{GS} = 10\text{ V}$	-	36	-	ns
$t_r^{(1)}$	Rise time		-	21	-	ns
$t_{d(off)}^{(1)}$	Turn-off delay time		-	93	-	ns
$t_f^{(1)}$	Fall time		-	30	-	ns

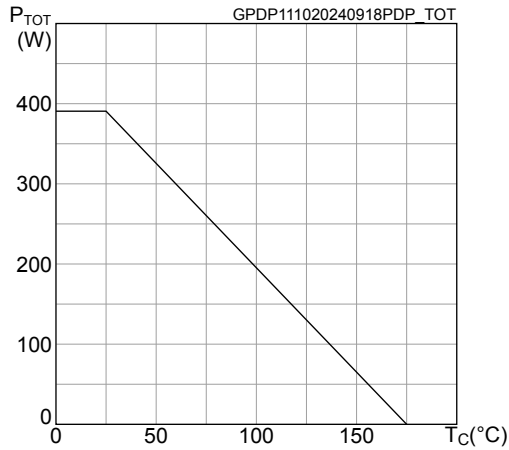
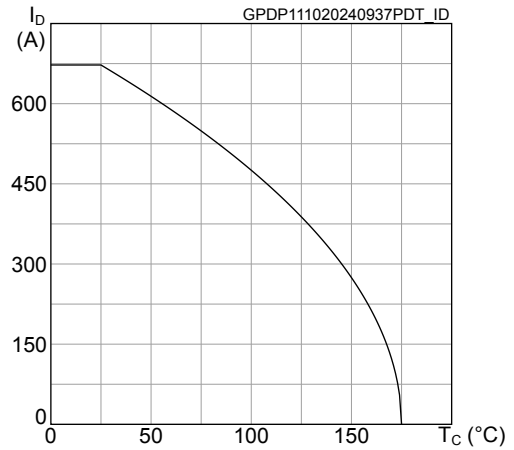
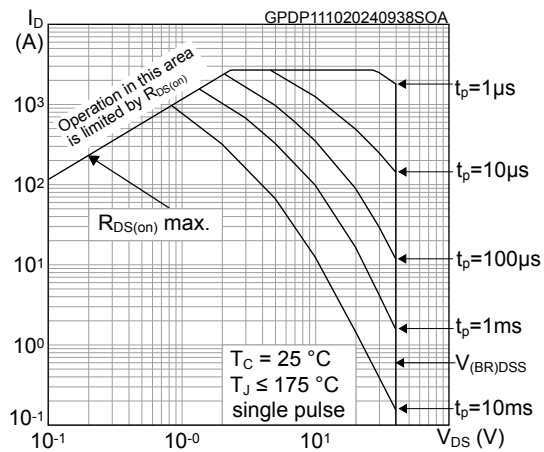
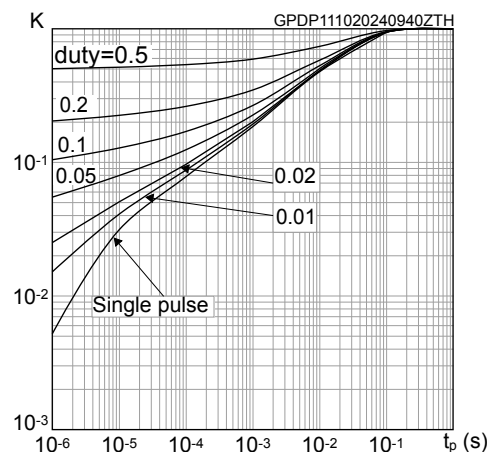
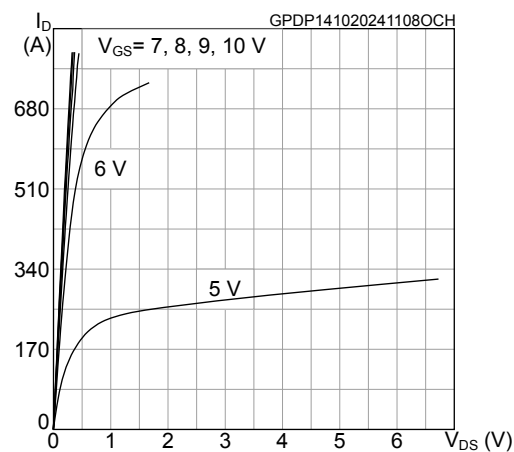
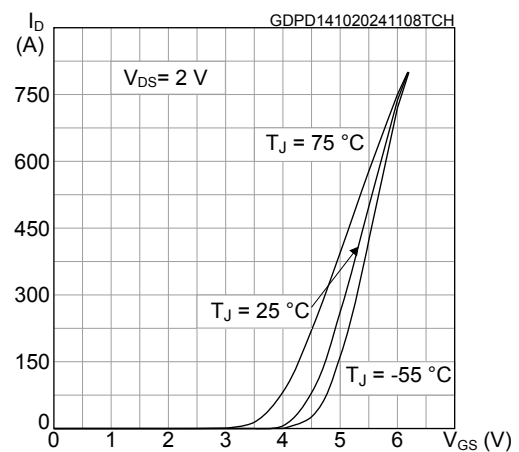
1. Specified by design and evaluated by characterization, not tested in production.

**Table 6. Source-drain diode**

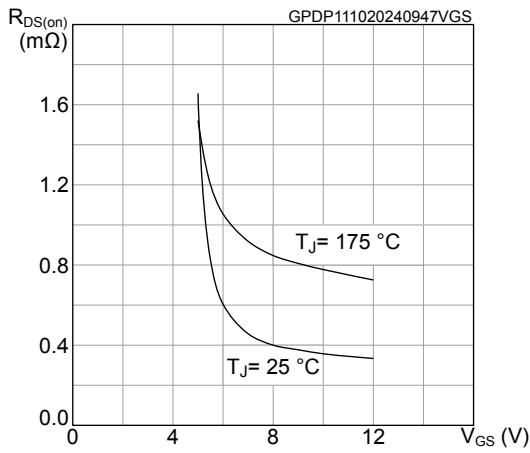
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}^{(1)}$	Forward on current (continuous)	$T_C = 25\text{ }^\circ\text{C}$	-		240	A
$V_{SD}$	Forward on voltage	$I_{SD} = 90\text{ A}, V_{GS} = 0\text{ V}$	-		1.1	V
$t_{rr}^{(1)}$	Reverse recovery time	$I_D = 90\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, V_{DD} = 32\text{ V}$	-	84		ns
$Q_{rr}^{(1)}$	Reverse recovery charge		-	143		nC
$I_{RRM}^{(1)}$	Reverse recovery current		-	3.4		A

1. Specified by design and evaluated by characterization, not tested in production.

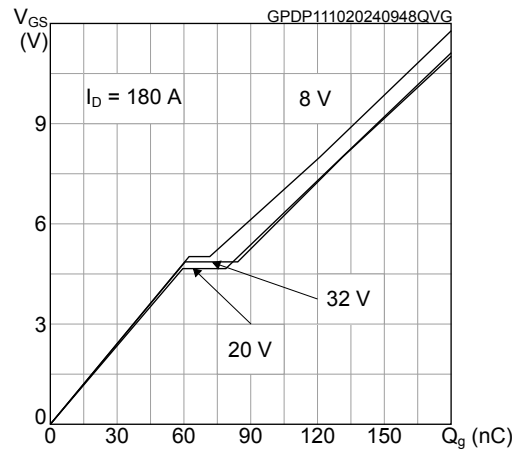
## 2.1 Electrical characteristics (curves)

**Figure 1. Total power dissipation**

**Figure 2. Drain current vs case temperature**

**Figure 3. Safe operating area**

**Figure 4. Normalized transient thermal impedance**

**Figure 5. Typical output characteristics**

**Figure 6. Typical transfer characteristics**


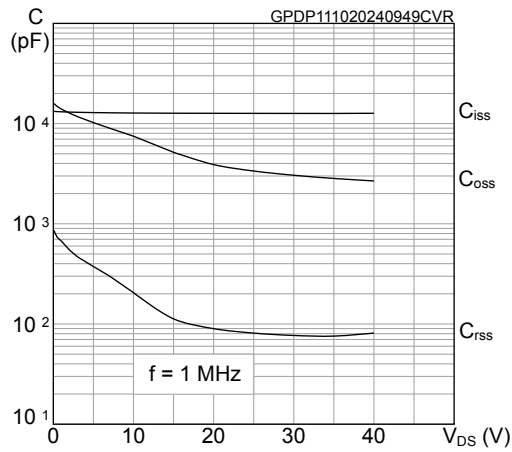
**Figure 7. Typical on-resistance vs gate-source voltage**



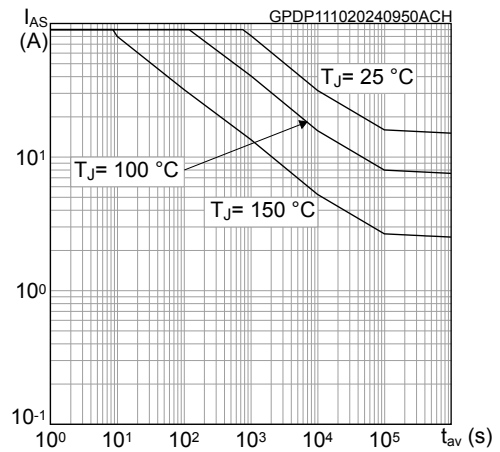
**Figure 8. Typical gate charge characteristics**



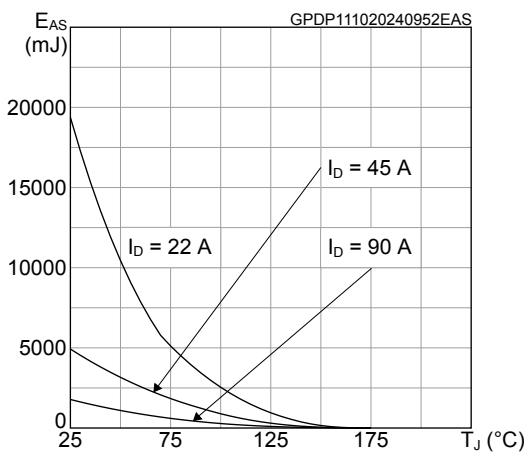
**Figure 9. Typical capacitance characteristics**



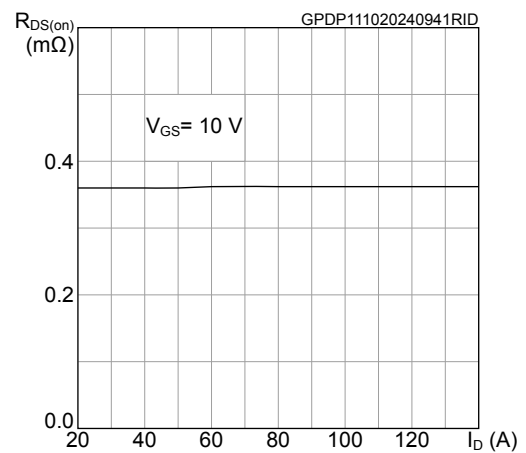
**Figure 10. Avalanche characteristics**



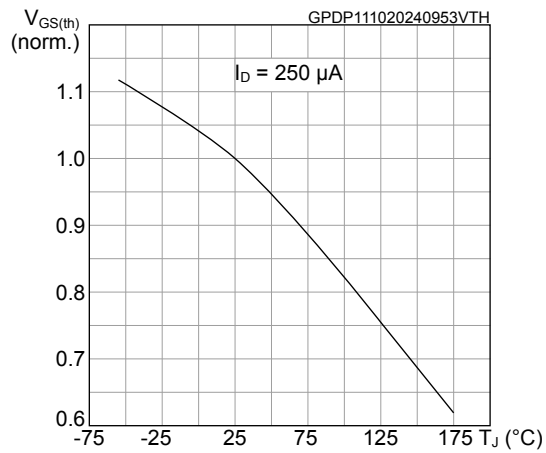
**Figure 11. Avalanche energy**



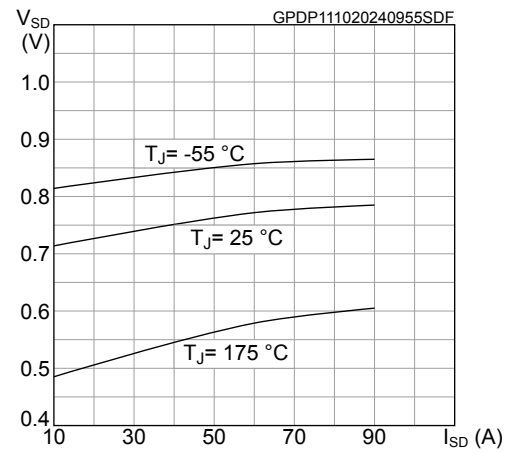
**Figure 12. Typical drain-source on-resistance**



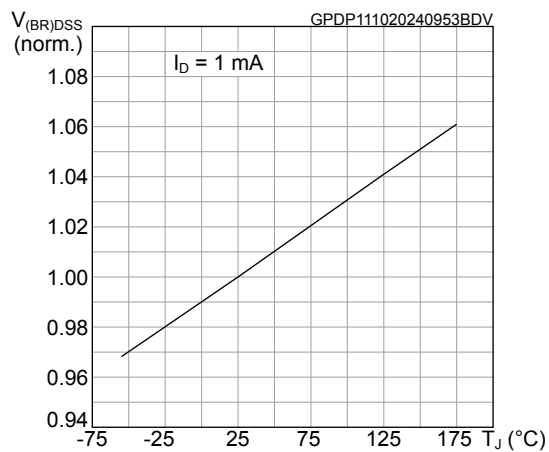
**Figure 13. Normalized gate threshold voltage vs temperature**



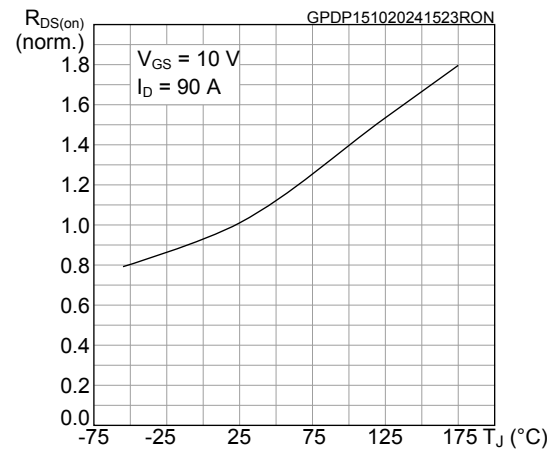
**Figure 14. Typical reverse diode forward characteristics**



**Figure 15. Normalized  $V_{(BR)DSS}$  vs temperature**



**Figure 16. Normalized on-resistance vs temperature**

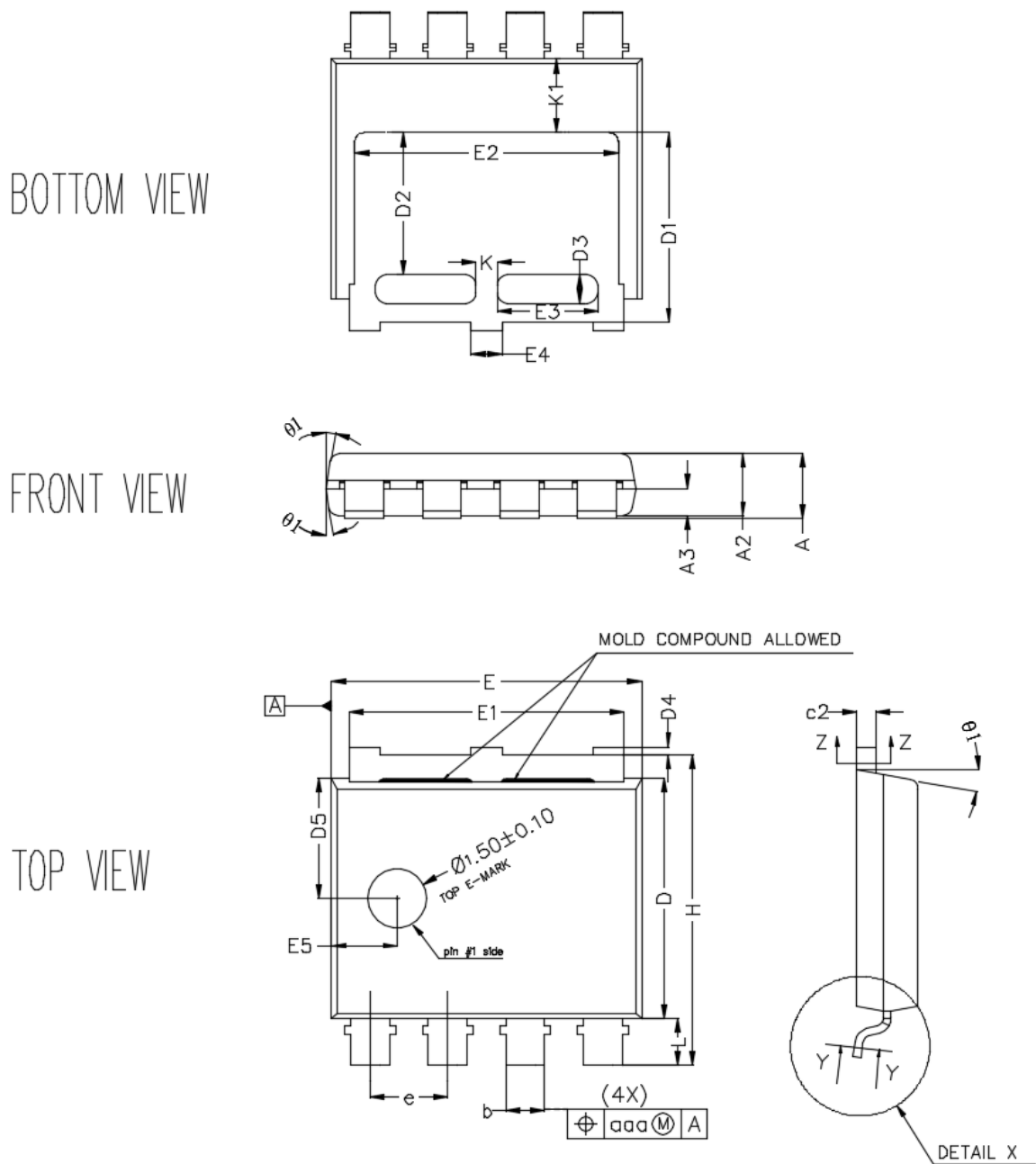


### 3 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

#### 3.1 PowerLeaded 8x8 package information

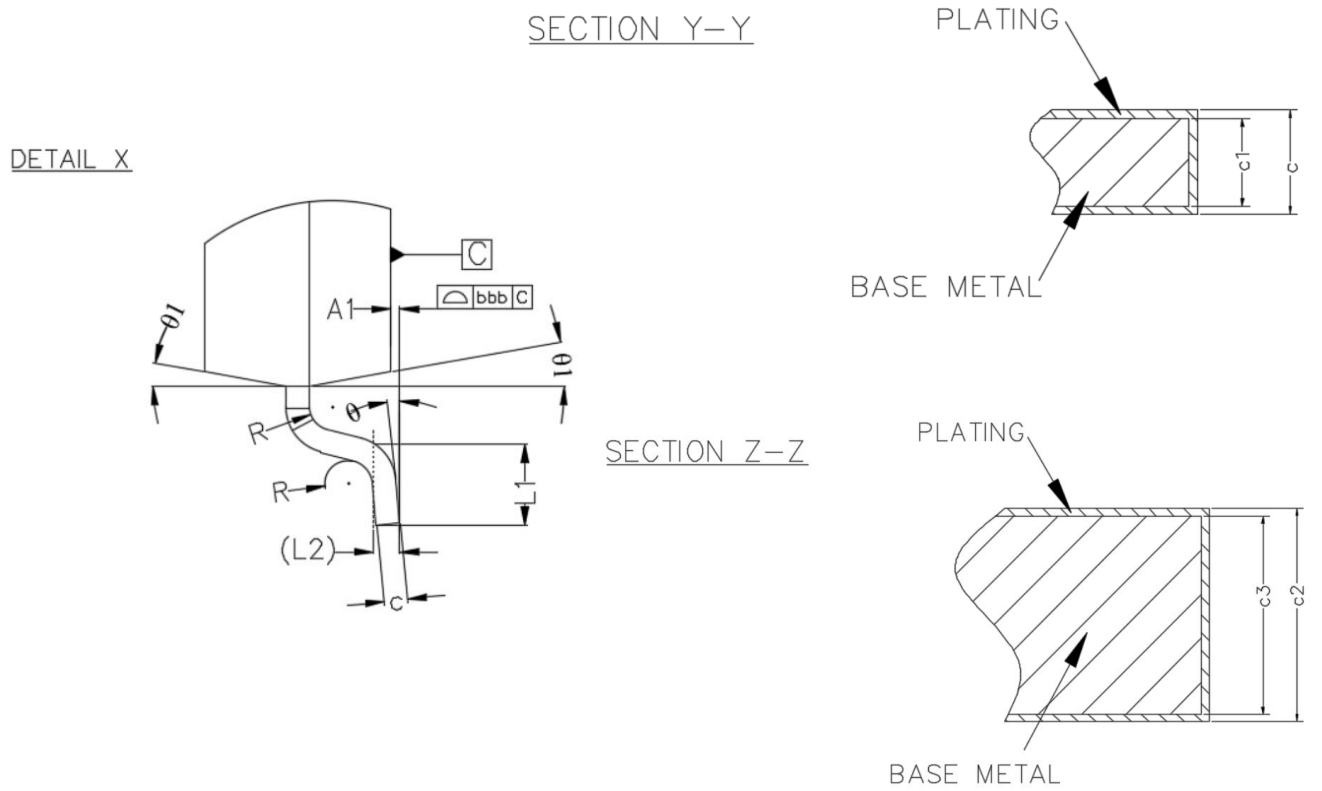
Figure 17. PowerLeaded 8x8 package outline



DM00548355\_Rev\_4



Figure 18. Section details

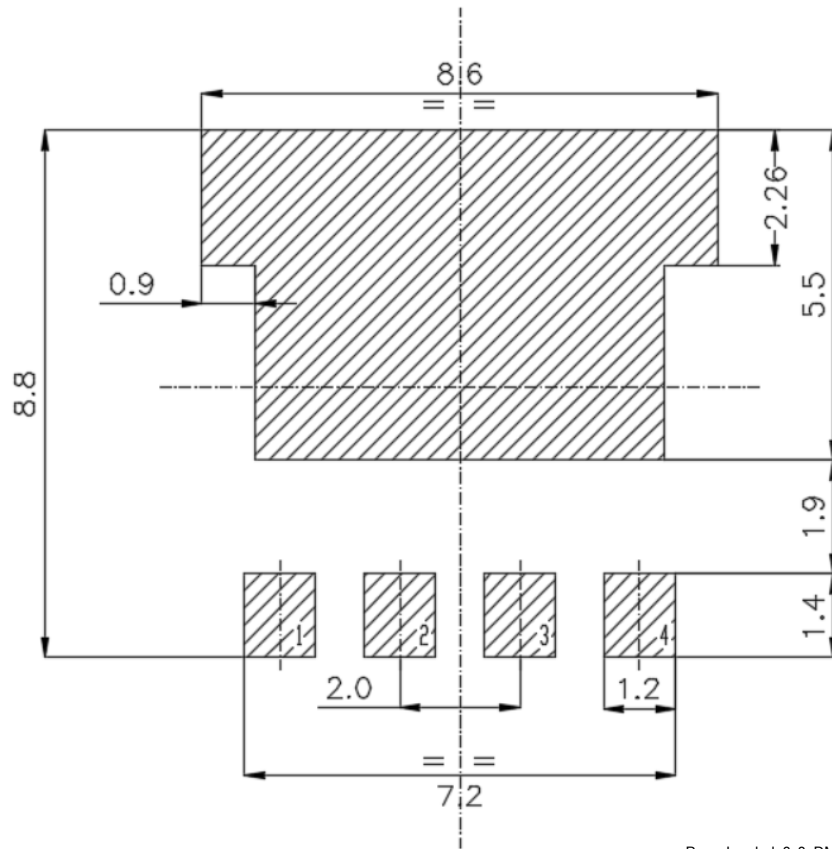


PowerLeaded\_8x8\_DM00548355\_details

**Table 7. PowerLeaded 8x8 mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A			1.85
A1	0.00	0.08	0.15
A2	1.50	1.60	1.70
A3	0.60	0.70	0.80
b	0.90	1.00	1.10
c	0.20		0.25
c1	0.19	0.20	0.21
c2	0.49		0.56
c3	0.48	0.50	0.52
D	6.10	6.20	6.30
D1	4.75	4.90	5.05
D2	3.50	3.65	3.80
D3	0.65	0.75	0.85
D4			0.20
D5	2.90	3.10	3.30
E	7.90	8.00	8.10
E1	6.95	7.10	7.25
E2	6.70	6.80	6.90
E3	2.50	2.60	2.70
E4	0.65	0.80	0.95
E5	1.50	1.70	1.90
e	1.90	2.00	2.10
H	7.85	8.00	8.15
K	0.45	0.55	0.65
K1	1.75	1.90	2.05
L	1.00	1.20	1.30
L1	0.60	0.70	0.80
L2	0.23BSC		
R	0.20REF		
θ	0°		8°
θ1	6°	10°	14°

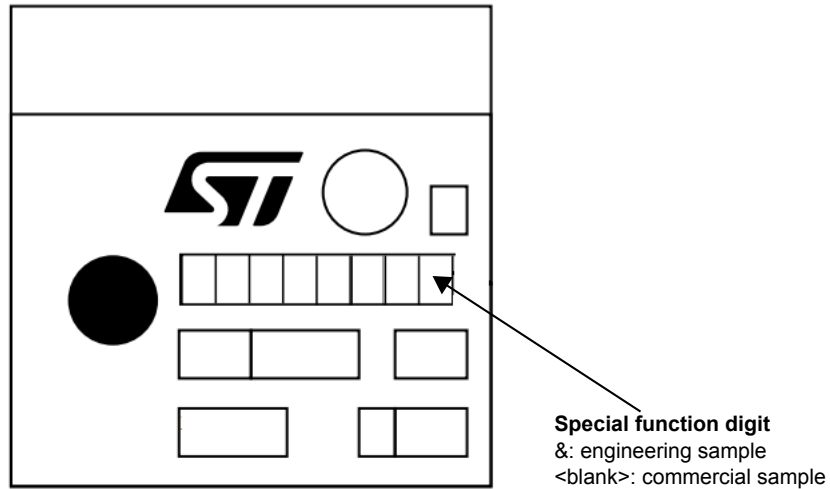
Figure 19. PowerLeaded 8x8 recommended footprint (dimensions are in mm)



PowerLeaded\_8x8\_DM00548355\_footprint

### 3.1.1 PowerLeaded 8x8 marking information

Figure 20. PowerLeaded 8x8 marking information



**Note:** *Engineering Samples: these samples can be clearly identified by a dedicated special symbol in the marking of each unit. These samples are intended to be used for electrical compatibility evaluation only; usage for any other purpose may be agreed only upon written authorization by ST. ST is not liable for any customer usage in production and/or in reliability qualification trials.*

Commercial Samples: fully qualified parts from ST standard production with no usage restrictions.

## Revision history

**Table 8. Document revision history**

Date	Revision	Changes
17-Jan-2023	1	Initial release.
16-Oct-2024	2	Modified title, <i>Features, Applications and Description</i> . Added schematic on cover page. Modified <i>Section 1: Electrical ratings, Section 2: Electrical characteristics</i> . Added <i>Section 2.1: Electrical characteristics (curves)</i> . Added <i>Section 3.1.1: PowerLeaded 8x8 marking information</i> . Minor text changes
08-Nov-2024	3	Document classification changed from ST restricted to public. Modified <i>Figure 3. Safe operating area</i> and <i>Figure 7. Typical on-resistance vs gate-source voltage</i> .
09-Jan-2025	4	Updated <a href="#">Figure 6. Typical transfer characteristics</a> . Minor text changes.

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