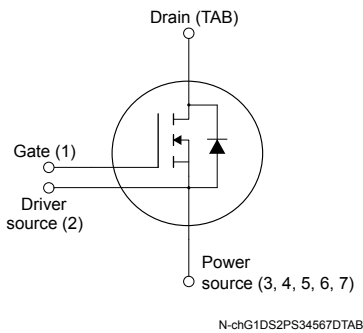
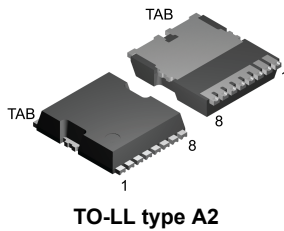


N-channel 650 V, 37 mΩ typ., 54 A, MDmesh M9 Power MOSFET in a TO-LL package



Product status link

[STO65N045M9](#)

Product summary

Order code	STO65N045M9
Marking	65N045M9
Package	TO-LL type A2
Packing	Tape and reel

Features

Order code	V _{DS}	R _{DS(on)} max.	I _D
STO65N045M9	650 V	45 mΩ	54 A

- Very low FOM ($R_{DS(on)} \cdot Q_g$)
- Higher dv/dt capability
- Excellent switching performance
- Easy to drive
- 100% avalanche tested
- Excellent switching performance thanks to the extra driving source pin

Application

- AC-DC converters
- DC-DC converters
- Microinverter

Description

This N-channel Power MOSFET is based on the most innovative super-junction MDmesh M9 technology, suitable for medium/high voltage MOSFETs featuring very low $R_{DS(on)}$ per area. The silicon based M9 technology benefits from a multi-drain manufacturing process which allows an enhanced device structure. The resulting product has one of the lower on-resistance and reduced gate charge values, among all silicon based fast switching super-junction Power MOSFETs, making it particularly suitable for applications that require superior power density and outstanding efficiency.

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 30	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	54	A
	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	34	
$I_{DM}^{(2)}$	Drain current (pulsed)	220	A
P_{TOT}	Total power dissipation at $T_C = 25\text{ }^\circ\text{C}$	245	W
dv/dt^3	Peak diode recovery voltage slope	50	V/ns
di/dt^3	Peak diode recovery current slope	900	A/ μs
$dv/dt^{(4)}$	MOSFET dv/dt ruggedness	120	V/ns
T_{stg}	Storage temperature range	-55 to 150	$^\circ\text{C}$
T_J	Operating junction temperature range		$^\circ\text{C}$

1. Referred to TO-247 long leads package.
2. Pulse width limited by safe operating area.
3. $I_{SD} \leq 28\text{ A}$, $V_{DS} (\text{peak}) < V_{(BR)DSS}$, $V_{DD} = 400\text{ V}$.
4. $V_{DS} (\text{peak}) < V_{(BR)DSS}$, $V_{DD} = 400\text{ V}$.

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	0.51	$^\circ\text{C/W}$
R_{thJA}	Thermal resistance, junction-to-ambient ⁽¹⁾	43	$^\circ\text{C/W}$
	Thermal resistance, junction-to-ambient ⁽²⁾	22	

1. When mounted on a standard 1 inch² area of FR-4 PCB with 2-oz copper.
2. When mounted on 40x40 mm area of FR-4 PCB with 2-oz copper.

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T_J max.)	6	A
E_{AS}	Single pulse avalanche energy (starting $T_J = 25\text{ }^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	775	mJ

2 Electrical characteristics

$T_C = 25\text{ °C}$ unless otherwise specified.

Table 4. On/off-states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$, $I_D = 1\text{ mA}$	650			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = 650\text{ V}$			1	μA
		$V_{GS} = 0\text{ V}$, $V_{DS} = 650\text{ V}$, $T_C = 125\text{ °C}$ ⁽¹⁾			200	
I_{GSS}	Gate-body leakage current	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 25\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	3.2	3.7	4.2	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 28\text{ A}$		37	45	m Ω

1. Specified by design, not tested in production.

Table 5. Dynamic characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 400\text{ V}$, $f = 250\text{ kHz}$, $V_{GS} = 0\text{ V}$	-	4560	-	pF
C_{oss}	Output capacitance		-	82	-	pF
$C_{oss\ eq.}^{(1)}$	Equivalent output capacitance	$V_{DS} = 0\text{ to }400\text{ V}$, $V_{GS} = 0\text{ V}$	-	1000	-	pF
R_g	Intrinsic gate resistance	$f = 250\text{ kHz}$, open drain	-	1	-	Ω
Q_g	Total gate charge	$V_{DD} = 400\text{ V}$, $I_D = 28\text{ A}$, $V_{GS} = 0\text{ to }10\text{ V}$ (see Figure 14. Test circuit for gate charge behavior)	-	94	-	nC
Q_{gs}	Gate-source charge		-	24	-	nC
Q_{gd}	Gate-drain charge		-	34	-	nC

1. $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to stated value.

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 325\text{ V}$, $I_D = 28\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$ (see Figure 13. Switching times test circuit for resistive load and Figure 18. Switching time waveform)	-	28	-	ns
t_r	Rise time		-	10	-	ns
$t_{d(off)}$	Turn-off delay time		-	85	-	ns
t_f	Fall time		-	4	-	ns

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}^{(1)}$	Source-drain current		-		54	A
$I_{SDM}^{(2)}$	Source-drain current (pulsed)		-		220	A
$V_{SD}^{(3)}$	Forward on voltage	$V_{GS} = 0\text{ V}$, $I_{SD} = 55\text{ A}$	-		1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 55\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 100\text{ V}$	-	288		ns
Q_{rr}	Reverse recovery charge	(see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	4		μC
I_{RRM}	Reverse recovery current	(see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	26		A
t_{rr}	Reverse recovery time	$I_{SD} = 55\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$,	-	400		ns
Q_{rr}	Reverse recovery charge	$V_{DD} = 100\text{ V}$, $T_J = 150\text{ }^\circ\text{C}$	-	7.5		μC
I_{RRM}	Reverse recovery current	(see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	34		A

1. Referred to TO-247 long leads package.
2. Pulse width is limited by safe operating area.
3. Pulsed: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

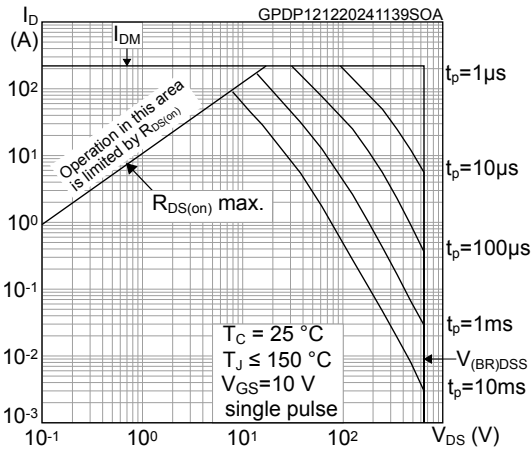


Figure 2. Maximum transient thermal impedance

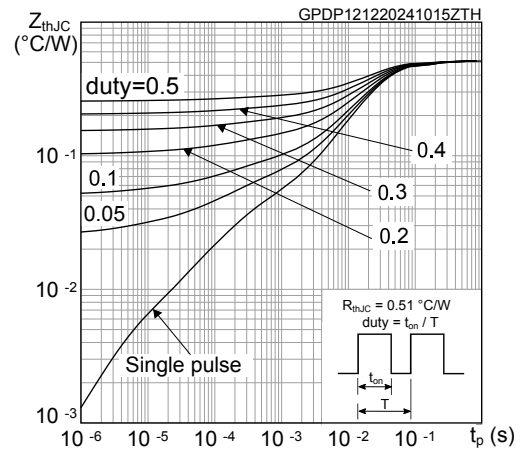


Figure 3. Typical output characteristics

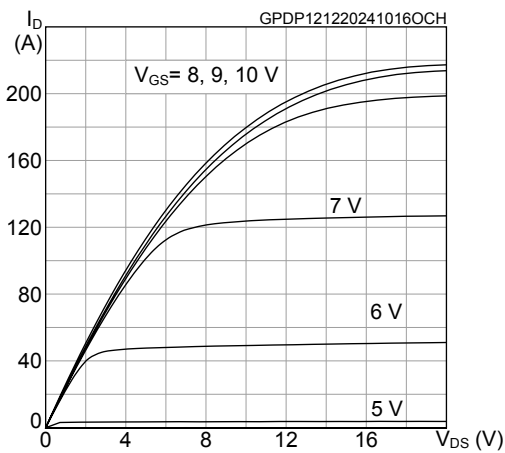


Figure 4. Typical transfer characteristics

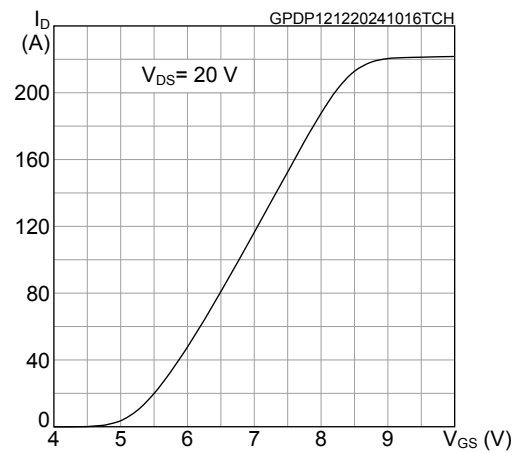


Figure 5. Typical gate charge characteristics

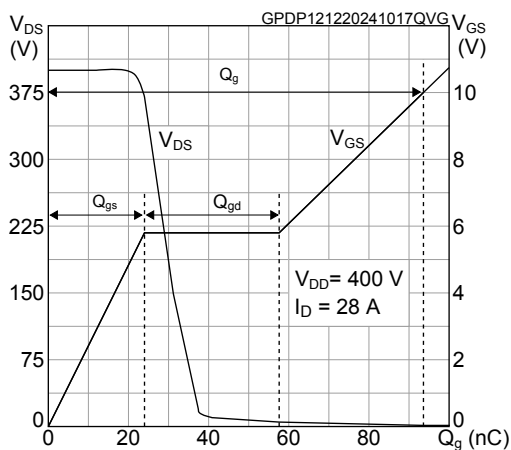


Figure 6. Typical drain-source on-resistance

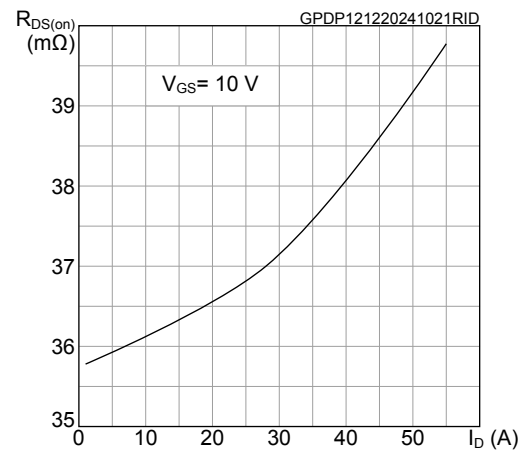


Figure 7. Typical capacitance characteristics

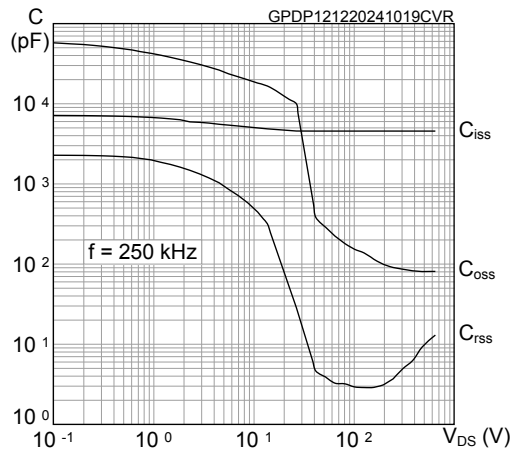


Figure 8. Typical output capacitance stored energy

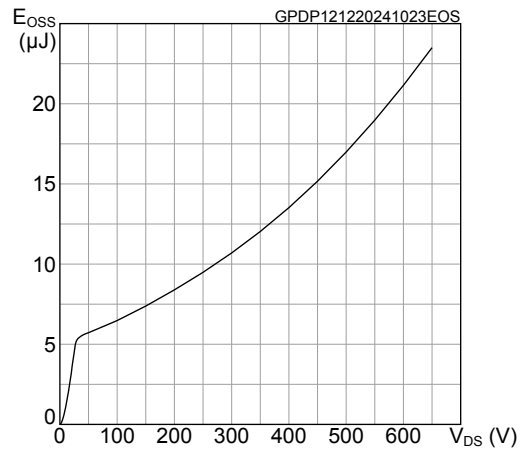


Figure 9. Normalized gate threshold vs temperature

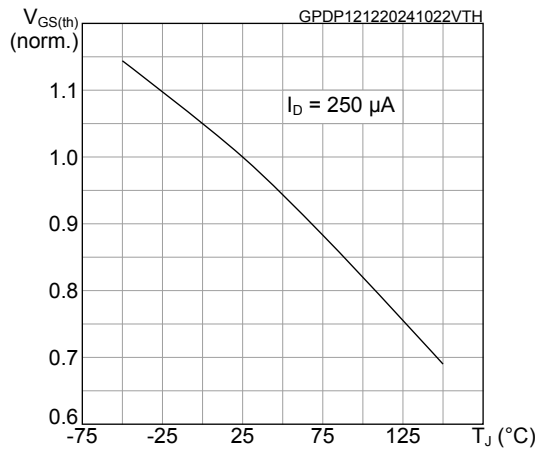


Figure 10. Normalized on-resistance vs temperature

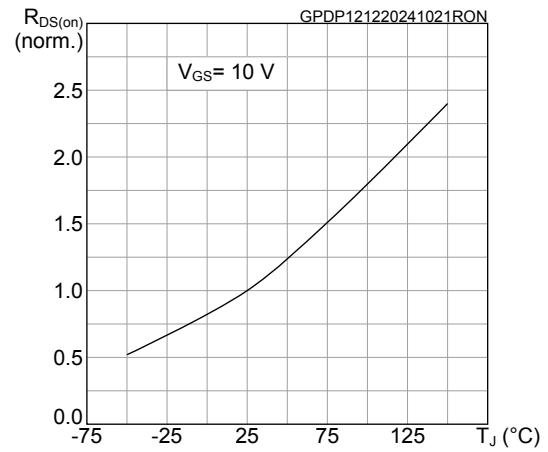


Figure 11. Normalized breakdown voltage vs temperature

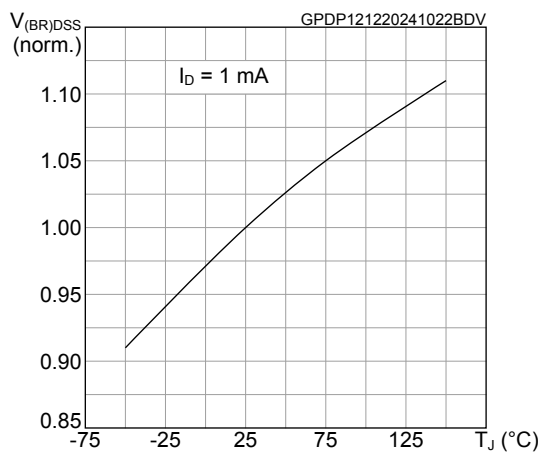
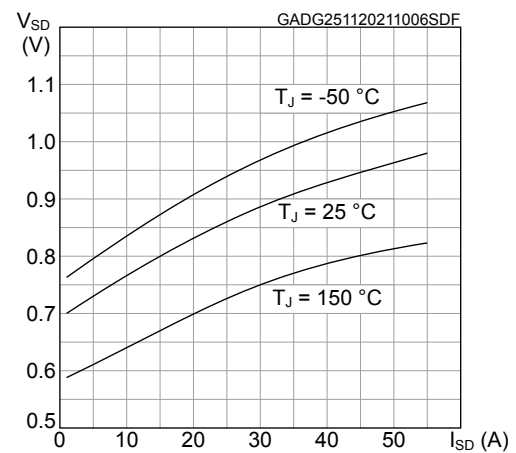
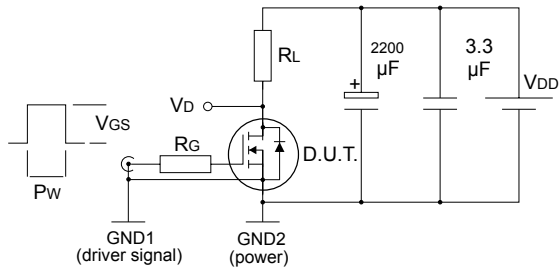


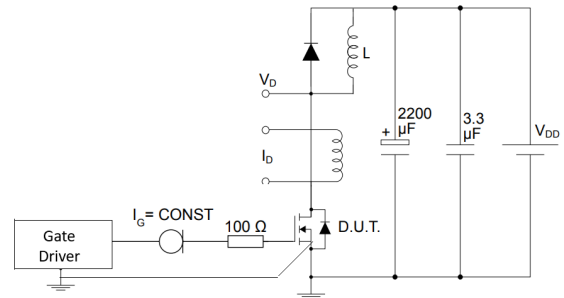
Figure 12. Typical reverse diode forward characteristics



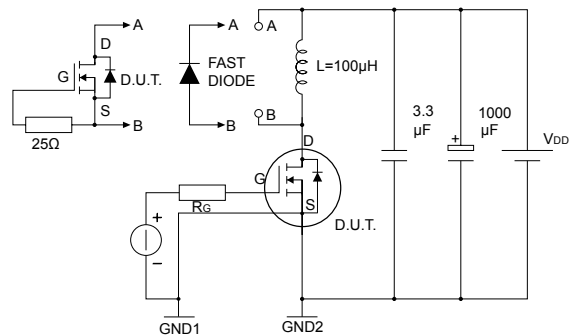
3 Test circuits

Figure 13. Switching times test circuit for resistive load


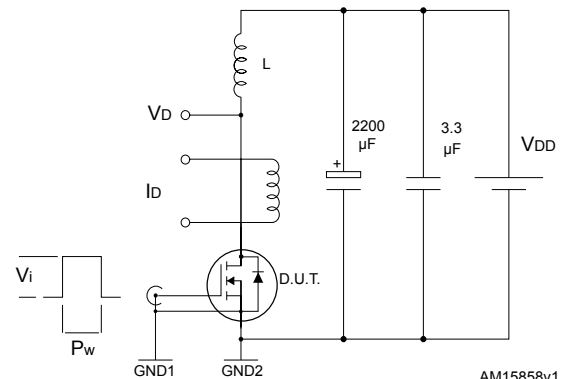
AM15855v1

Figure 14. Test circuit for gate charge behavior


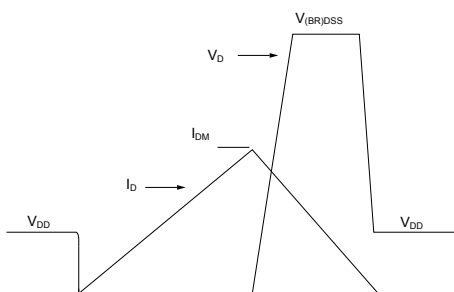
GDPDP191120241113SA

Figure 15. Test circuit for inductive load switching and diode recovery times


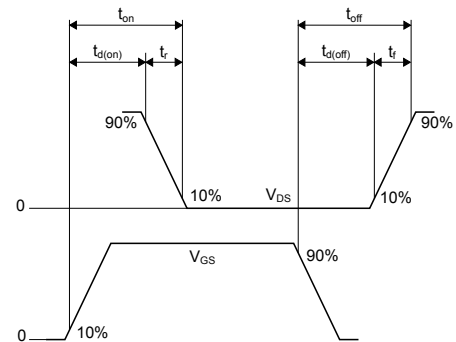
AM15857v1

Figure 16. Unclamped inductive load test circuit


AM15858v1

Figure 17. Unclamped inductive waveform


AM01472v1

Figure 18. Switching time waveform


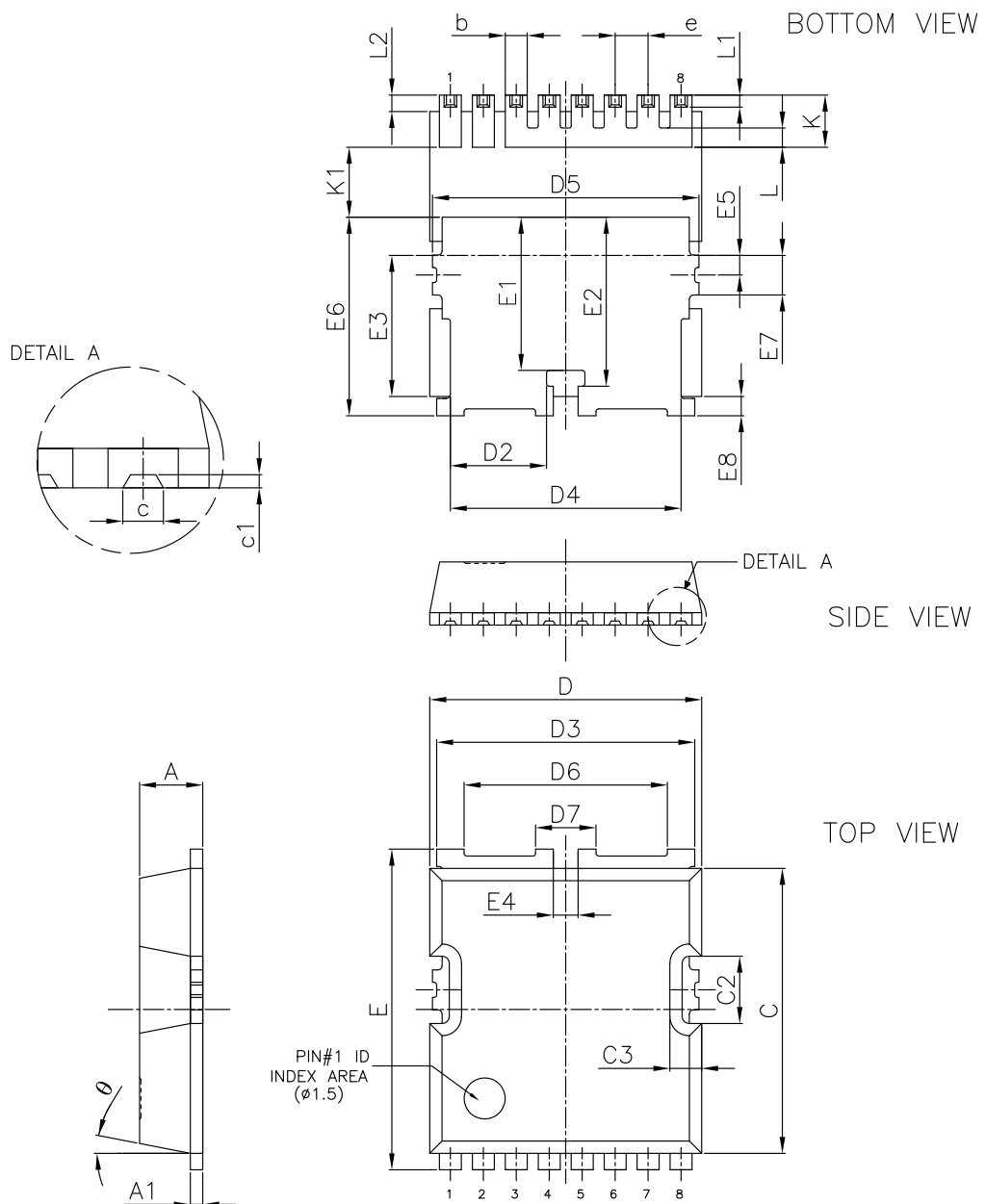
AM01473v1

4 Package information

To meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 TO-LL type A2 package information

Figure 19. TO-LL type A2 package outline

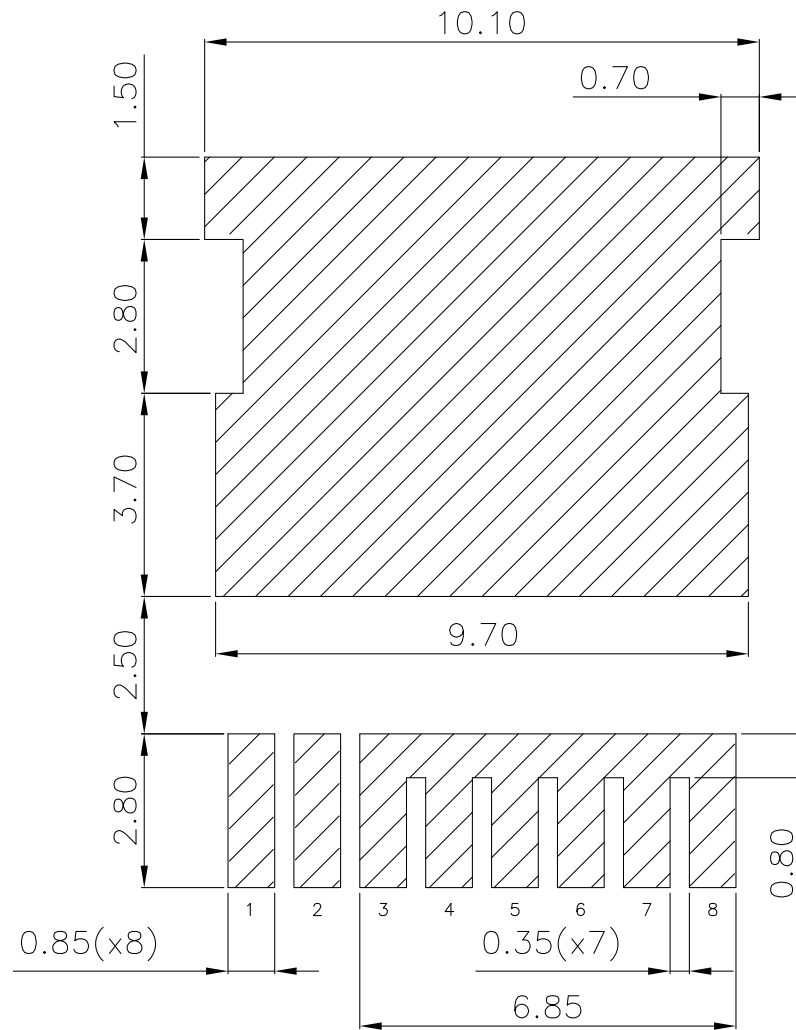


DM00276569_7_type_A2

Table 8. TO-LL type A2 package mechanical data

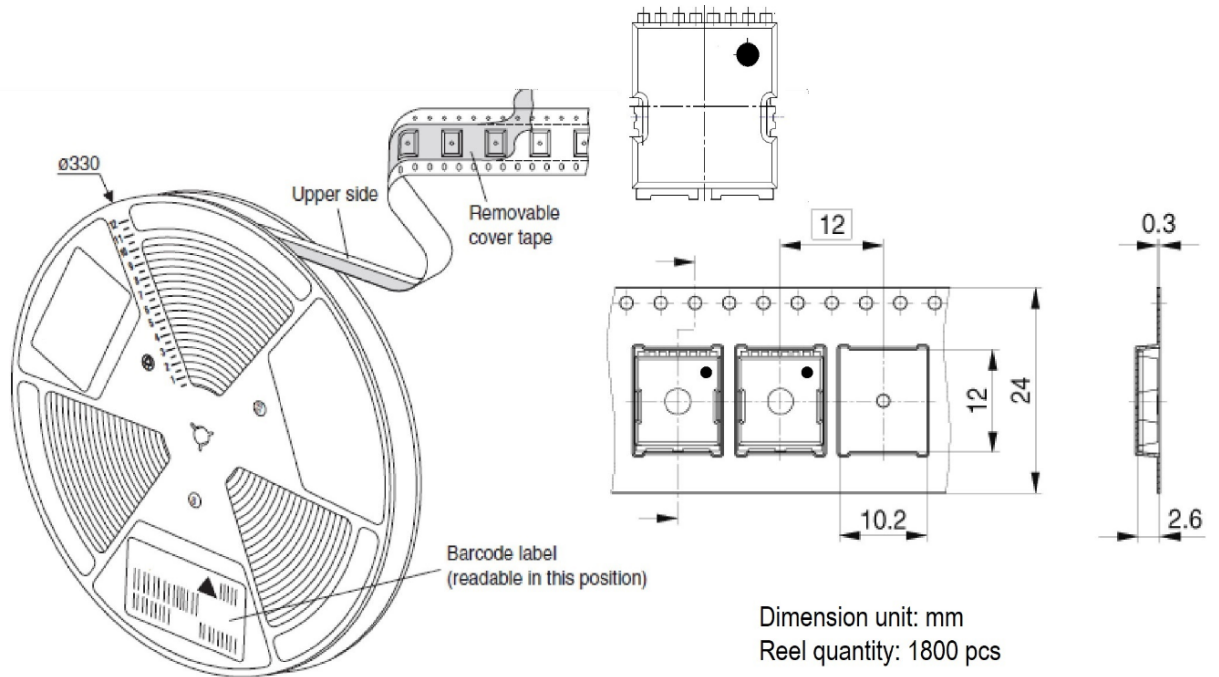
Dim.	mm		
	Min.	Typ.	Max.
A	2.20	2.30	2.40
A1	0.40	0.48	0.60
b	0.70	0.80	0.90
c		0.46	
c1		0.15	
C	10.28	10.38	10.48
C2	2.35	2.45	2.55
C3		1.16	
D	9.80	9.90	10.00
D2	3.30	3.50	3.70
D3	9.30	9.40	9.50
D4	8.20	8.40	8.60
D5	9.50	9.70	9.90
D6		7.40	
D7		2.20	
e		1.20	
E	11.48	11.68	11.88
E1		5.58	
E2		6.15	
E3		5.14	
E4		0.90	
E5		0.72	
E6	7.03	7.23	7.43
E7		1.44	
E8	0.50	0.70	0.90
K	1.70	1.90	2.10
K1	2.40		
L		0.70	
L1		0.44	
L2	0.40	0.60	0.80
θ		11°	

Figure 20. TO-LL type A2 recommended footprint (dimensions are in mm)



DM00276569_7_type_A2

Figure 23. TO-LL orientation in tape pocket



Revision history

Table 9. Document revision history

Date	Revision	Changes
18-Dec-2024	1	First release.

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