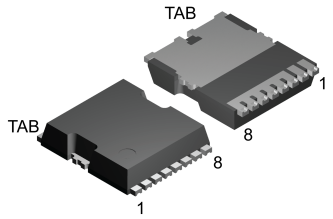
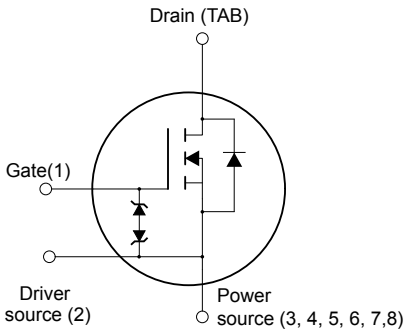
N-channel 600 V, 44 mΩ typ., 34 A MDmesh™ M6 Power MOSFET in a TO-LL HV package



TO-LL HV



N-chG1DS2PS345678DTABZ

Product status link
STO68N60M6AV

Product summary	
Order code	STO68N60M6AV
Marking	68N60M6AV
Package	TO-LL HV
Packing	Tape and reel

Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STO68N60M6AV	600 V	49 mΩ	38 A

- Reduced switching losses
- Lower $R_{DS(on)}$ * area vs previous generation
- Low gate input resistance
- 100% avalanche tested
- Zener-protected
- High-creepage package
- Excellent switching performance thanks to the extra driving source pin

Applications

- Switching applications

Description

The new MDmesh™ M6 technology incorporates the most recent advancements to the well-known and consolidated MDmesh family of SJ MOSFETs. STMicroelectronics builds on the previous generation of MDmesh devices through its new M6 technology, which combines excellent $R_{DS(on)}$ per area improvement with one of the most effective switching behaviors available, as well as a user-friendly experience for maximum end-application efficiency.

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 25	V
I_D	Drain current (continuous) at T_C = 25 °C	38	A
I_D	Drain current (continuous) at T_C = 100 °C	24	A
I_{DM} (1)	Drain current (pulsed)	TBD	A
P_{TOT}	Total dissipation at T_C = 25 °C	174	W
dv/dt(2)	Peak diode recovery voltage slope	15	V/ns
dv/dt(3)	MOSFET dv/dt ruggedness	50	V/ns
T_{stg}	Storage temperature range	- 55 to 150	°C
T_j	Operating junction temperature range		

1. *Pulse width limited by safe operating area.*
2. *I_{SD} ≤ 38 A, di/dt ≤ 400 A/µs; $V_{DS(peak)}$ < $V_{(BR)DSS}$, V_{DD} = 400 V.*
3. *V_{DS} ≤ 480 V*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case	0.72	°C/W
$R_{thj\text{-}amb}$(1)	Thermal resistance junction-amb	43	°C/W
$R_{thj\text{-}amb}$(2)	Thermal resistance junction-amb	46	°C/W

1. *When mounted on 1 inch² FR-4 pcb, standard footprint 2 Oz copper board.*
2. *When mounted on 40x40mm FR-4 pcb, 6 cm² 2 Oz copper board.*

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T_{jmax})	TBD	A
E_{AS}	Single pulse avalanche energy (starting T_j = 25 °C, I_D = I_{AR}; V_{DD} = 50 V)	TBD	mJ

2 Electrical characteristics

T_C = 25 °C unless otherwise specified

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	600			V
I_{DSS}	Zero gate voltage Drain current	V_{GS} = 0 V, V_{DS} = 600 V			1	µA
		V_{GS} = 0 V, V_{DS} = 600 V, T_C = 125 °C(1)			100	µA
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±25 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	3.25	4	4.75	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 19 A		44	49	mΩ

1. *Defined by design, not subject to production test.*

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS}= 100 V, f = 1 MHz, V_{GS} = 0 V	-	3250	-	pF
C_{oss}	Output capacitance		-	245	-	pF
C_{rss}	Reverse transfer capacitance		-	3	-	pF
$C_{oss\ eq.}$ (1)	Equivalent output capacitance	V_{DS} = 0 to 480 V, V_{GS} = 0 V	-	TBD	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz, I_D = 0 A	-	2.5	-	Ω
Q_g	Total gate charge	V_{DD} = 480 V, I_D = 38 A, V_{GS} = 0 to 10 V (see)Figure 4. Test circuit for gate charge behavior	-	80	-	nC
Q_{gs}	Gate-source charge		-	TBD	-	nC
Q_{gd}	Gate-drain charge		-	TBD	-	nC

1. *$C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}*

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 300 V, I_D = 19 A, R_G = 4.7 Ω, V_{GS} = 10 V (see Figure 3. Test circuit for resistive load switching times and Figure 8. Switching time waveform)	-	TBD	-	ns
t_r	Rise time		-	TBD	-	ns
$t_{d(off)}$	Turn-off-delay time		-	TBD	-	ns
t_f	Fall time		-	TBD	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		38	A
I_{SDM} (1)	Source-drain current (pulsed)		-		TBD	A
V_{SD} (2)	Forward on voltage	V_{GS} = 0 V, I_{SD} = 38 A	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 38 A, di/dt = 100 A/µs, V_{DD} = 60 V, T_j = 150 °C (see Figure 5. Test circuit for inductive load switching and diode recovery times)	-	TBD		ns
Q_{rr}	Reverse recovery charge		-	TBD		µC
I_{RRM}	Reverse recovery current		-	TBD		A

1. *Pulse width is limited by safe operating area*
2. *Pulsed: pulse duration = 300 µs, duty cycle 1.5%*

3 Test circuits

Figure 3. Test circuit for resistive load switching times

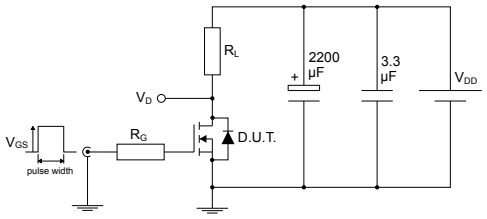


Figure 4. Test circuit for gate charge behavior

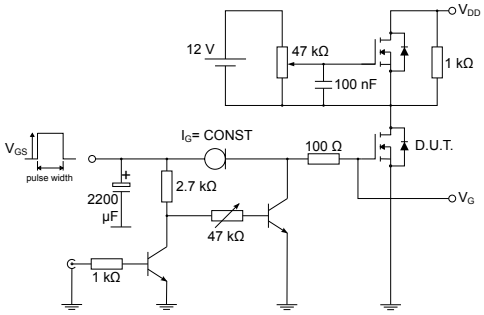


Figure 5. Test circuit for inductive load switching and diode recovery times

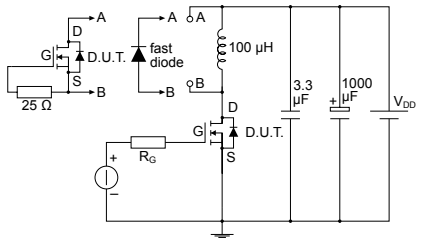


Figure 6. Unclamped inductive load test circuit

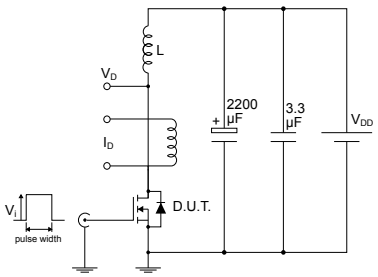


Figure 7. Unclamped inductive waveform

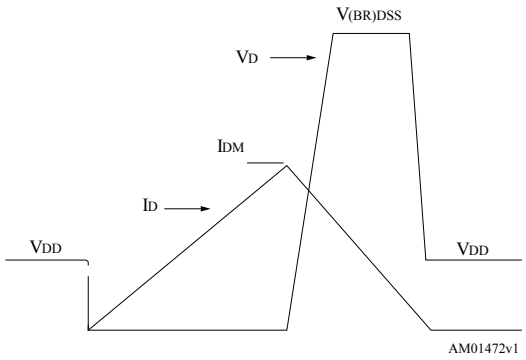
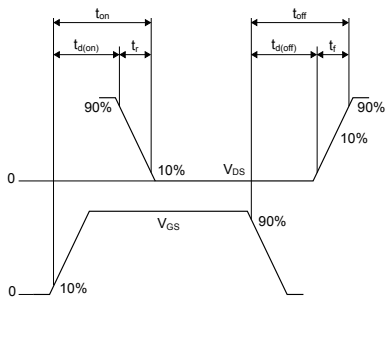


Figure 8. Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 TO-LL HV package information

Figure 9. TO-LL HV package outline

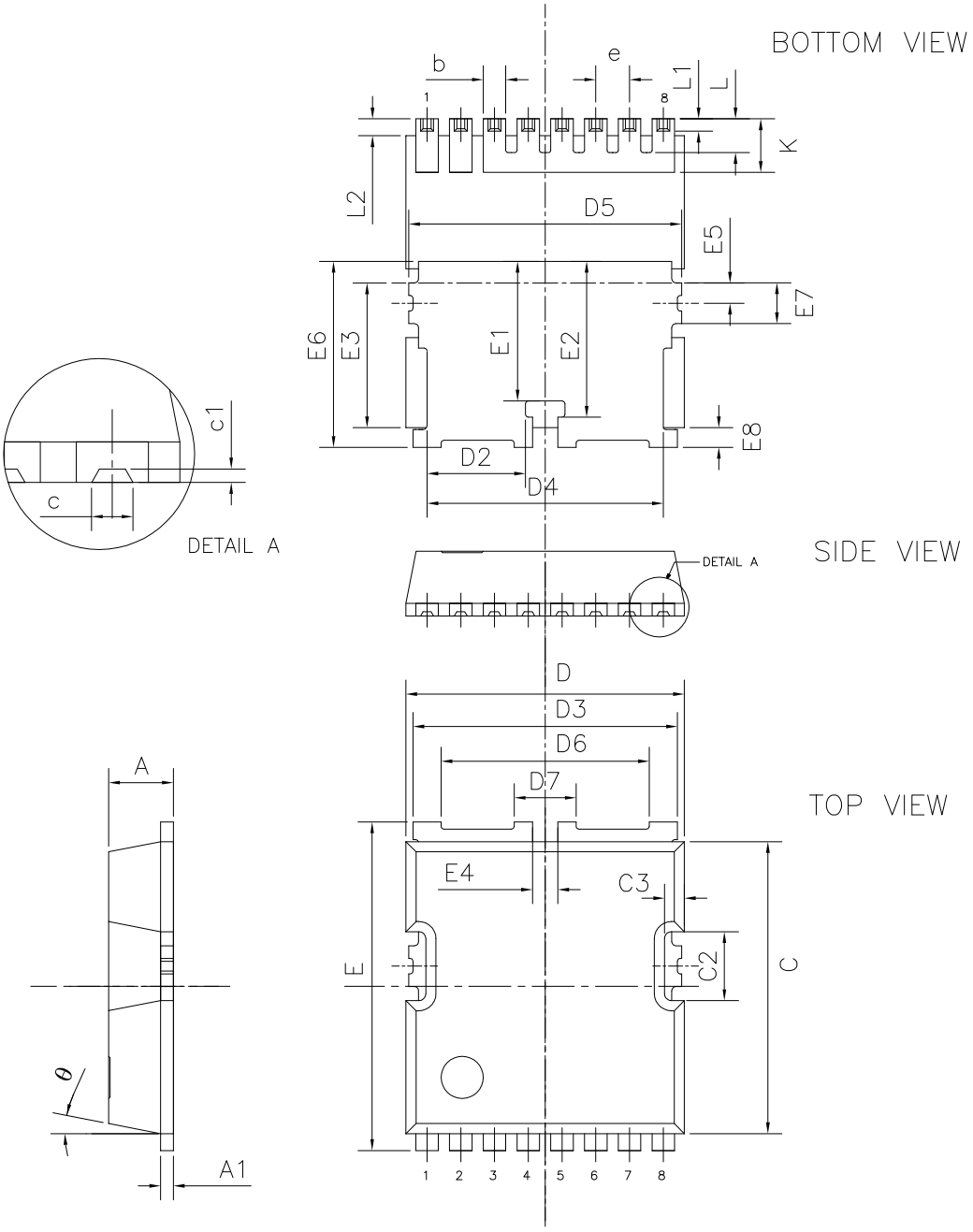


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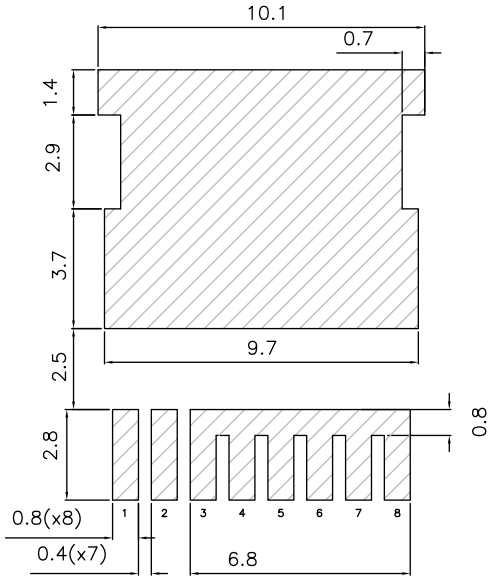
Table 8. **TO-LL HV package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	2.20	2.30	2.40
A1	0.40	0.48	0.60
b		0.80	0.93
c		0.46	
c1		0.15	
C	10.28	10.38	10.48
C2	2.35	2.45	2.55
C3		0.71	
D	9.80	9.90	10.00
D2	3.30	3.50	3.70
D3	9.30	9.40	9.50
D4	8.20	8.40	8.60
D5	9.50	9.70	9.90
D6		7.40	
D7		2.20	
e		1.20	
E	11.48	11.68	11.88
E1		4.96	
E2		5.54	
E3		5.14	
E4		0.90	
E5		0.72	
E6	6.41	6.61	6.81
E7	0.50	0.70	0.90
K	1.70	1.90	2.10
L	1.05	1.20	1.35
L1	0.25	0.35	0.45
L2	0.40	0.60	0.80
θ		11°	

Figure 10. TO-LL HV recommended footprint (dimensions are in mm)



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Revision history

Table 9. **Document revision history**

Date	Revision	Changes
28-May-2018	1	First release.

Contents

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