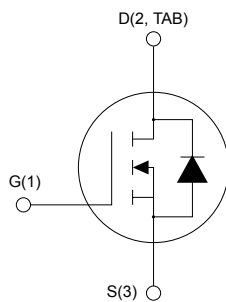
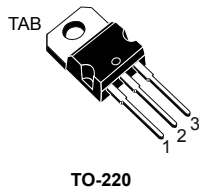


## N-channel 250 V, 15 mΩ typ., 56 A MDmesh M9 Power MOSFET in a TO-220 package



AM01475v1\_noZen



### Features

Order code	$V_{DS}$	$R_{DS(on)}$ max.	$I_D$
STP25N018M9	250 V	18 mΩ	56 A

- Very low FOM ( $R_{DS(on)} \cdot Q_g$ )
- Higher dv/dt capability
- Excellent switching performance
- Easy to drive
- 100% avalanche tested

### Application

- AC-DC converters
- DC-DC converters
- Microinverter

### Description

This N-channel Power MOSFET is based on the most innovative super-junction MDmesh M9 technology, suitable for medium/high voltage MOSFETs featuring very low  $R_{DS(on)}$  per area. The silicon based M9 technology benefits from a multi-drain manufacturing process which allows an enhanced device structure. The resulting product has one of the lower on-resistance and reduced gate charge values, among all silicon based fast switching super-junction Power MOSFETs, making it particularly suitable for applications that require superior power density and outstanding efficiency.

#### Product status link

[STP25N018M9](#)

#### Product summary

Order code	STP25N018M9
Marking	25N018M9
Package	TO-220
Packing	Tube

# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{GS}$	Gate-source voltage	$\pm 30$	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	56	A
	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	54	
$I_{DM}^{(2)}$	Drain current (pulsed)	375	A
$P_{TOT}$	Total power dissipation at $T_C = 25\text{ }^\circ\text{C}$	320	W
$dv/dt^{(3)}$	Peak diode recovery voltage slope	50	V/ns
$di/dt^{(3)}$	Peak diode recovery current slope	900	A/ $\mu\text{s}$
$dv/dt^{(4)}$	MOSFET $dv/dt$ ruggedness	120	V/ns
$T_{stg}$	Storage temperature range	-55 to 150	$^\circ\text{C}$
$T_J$	Operating junction temperature range		$^\circ\text{C}$

- Limited by package.
- Pulse width is limited by safe operating area.
- $I_{SD} \leq 28\text{ A}$ ,  $V_{DS} (\text{peak}) < V_{(BR)DSS}$ ,  $V_{DD} = 100\text{ V}$ .
- $V_{DS} (\text{peak}) < V_{(BR)DSS}$ ,  $V_{DD} = 100\text{ V}$ .

**Table 2. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thJC}$	Thermal resistance, junction-to-case	0.39	$^\circ\text{C/W}$
$R_{thJA}$	Thermal resistance, junction-to-ambient	62.5	$^\circ\text{C/W}$

**Table 3. Avalanche characteristics**

Symbol	Parameter	Value	Unit
$I_{AR}$	Avalanche current, repetitive or non-repetitive (pulse width limited by $T_J$ max.)	6	A
$E_{AS}$	Single pulse avalanche energy (starting $T_J = 25\text{ }^\circ\text{C}$ , $I_D = I_{AR}$ , $V_{DD} = 100\text{ V}$ )	839	mJ

## 2 Electrical characteristics

$T_C = 25\text{ °C}$  unless otherwise specified.

**Table 4. On-/off-states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$ , $I_D = 1\text{ mA}$	250			V
$I_{DSS}$	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$ , $V_{DS} = 250\text{ V}$			1	$\mu\text{A}$
		$V_{GS} = 0\text{ V}$ , $V_{DS} = 250\text{ V}$ , $T_C = 125\text{ °C}^{(1)}$			200	
$I_{GSS}$	Gate-body leakage current	$V_{DS} = 0\text{ V}$ , $V_{GS} = \pm 25\text{ V}$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	3.2	3.7	4.2	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$ , $I_D = 28\text{ A}$		15	18	m $\Omega$

1. Specified by design, not tested in production.

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 100\text{ V}$ , $f = 250\text{ kHz}$ , $V_{GS} = 0\text{ V}$	-	4600	-	pF
$C_{oss}$	Output capacitance		-	250	-	pF
$C_{oss\text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{DS} = 0\text{ to }200\text{ V}$ , $V_{GS} = 0\text{ V}$	-	2130	-	pF
$R_g$	Intrinsic gate resistance	$f = 250\text{ kHz}$ , open drain	-	1	-	$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 100\text{ V}$ , $I_D = 28\text{ A}$ , $V_{GS} = 0\text{ to }10\text{ V}$ (see Figure 14. Test circuit for gate charge behavior)	-	85	-	nC
$Q_{gs}$	Gate-source charge		-	23	-	nC
$Q_{gd}$	Gate-drain charge		-	32	-	nC

1.  $C_{oss\text{ eq.}}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to stated value.

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 100\text{ V}$ , $I_D = 28\text{ A}$ , $R_G = 4.7\text{ }\Omega$ , $V_{GS} = 10\text{ V}$ (see Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform)	-	23	-	ns
$t_r$	Rise time		-	3.6	-	ns
$t_{d(off)}$	Turn-off delay time		-	61	-	ns
$t_f$	Fall time		-	31	-	ns

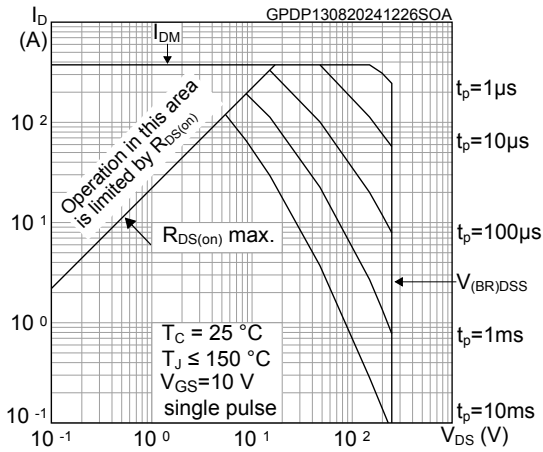
**Table 7. Source-drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}^{(1)}$	Source-drain current		-		56	A
$I_{SDM}^{(2)}$	Source-drain current (pulsed)		-		375	A
$V_{SD}^{(3)}$	Forward on voltage	$I_{SD} = 55 \text{ A}$ , $V_{GS} = 0 \text{ V}$	-		1.6	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 55 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$ ,	-	151		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 100 \text{ V}$	-	0.9		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current	(see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	12		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 55 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$ ,	-	213		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 100 \text{ V}$ , $T_J = 150 \text{ }^\circ\text{C}$	-	1.9		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current	(see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	17.5		A

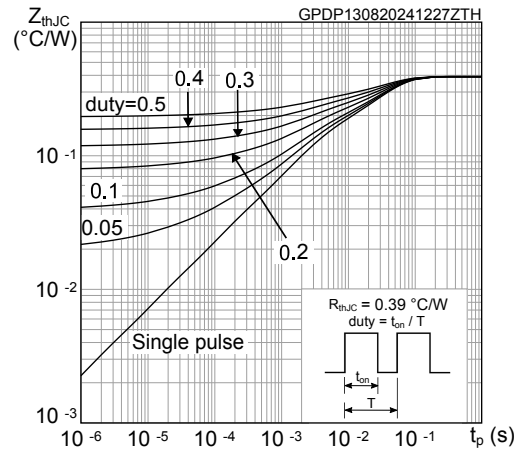
1. Limited by package.
2. Pulse width is limited by safe operating area.
3. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%.

## 2.1 Electrical characteristics (curves)

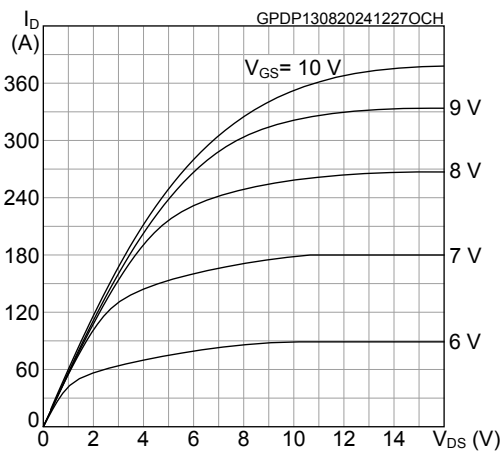
**Figure 1. Safe operating area**



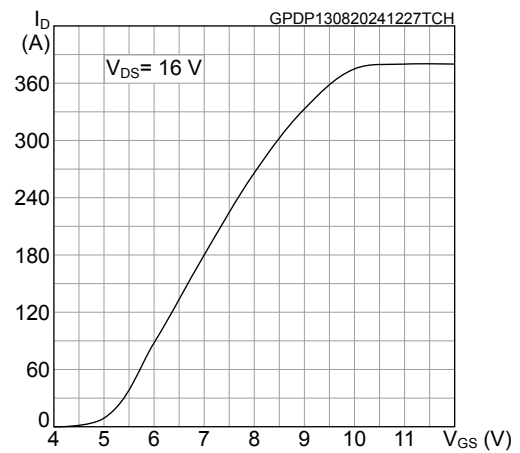
**Figure 2. Maximum transient thermal impedance**



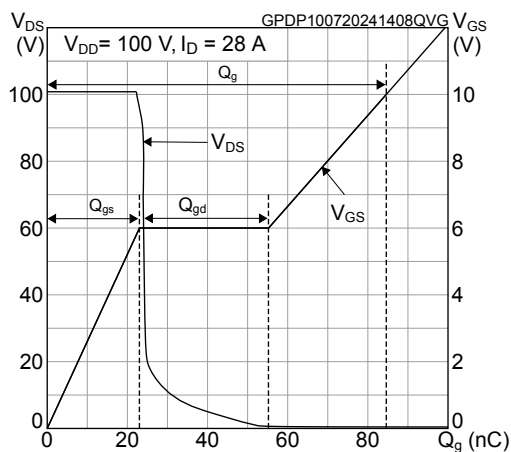
**Figure 3. Typical output characteristics**



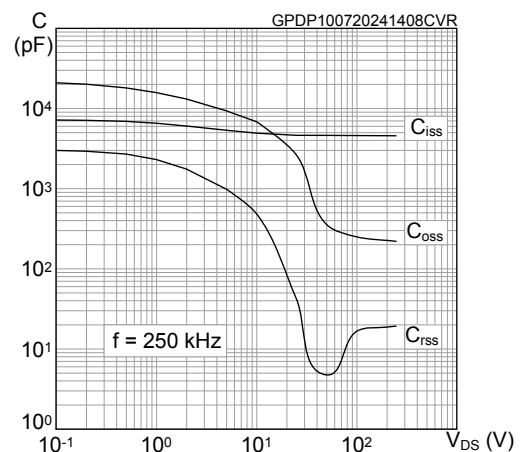
**Figure 4. Typical transfer characteristics**



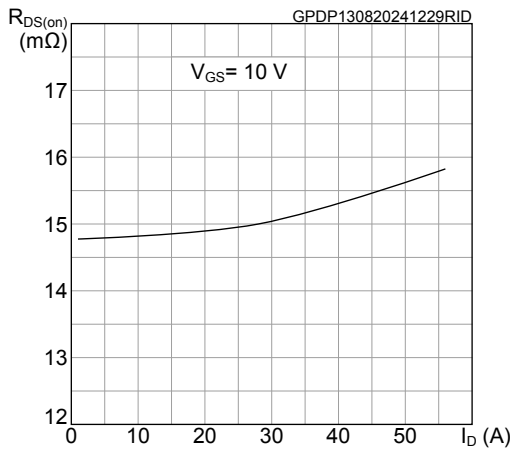
**Figure 5. Typical gate charge characteristics**



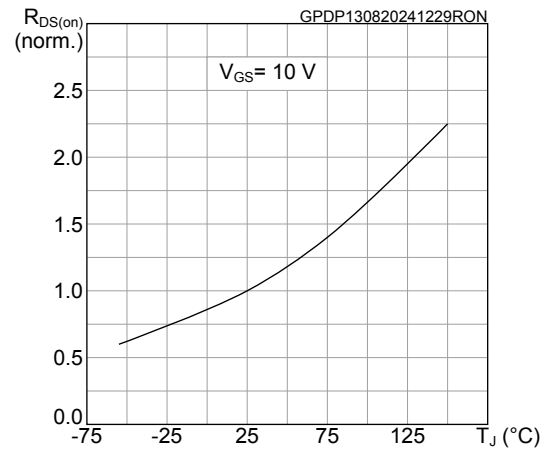
**Figure 6. Typical capacitance characteristics**



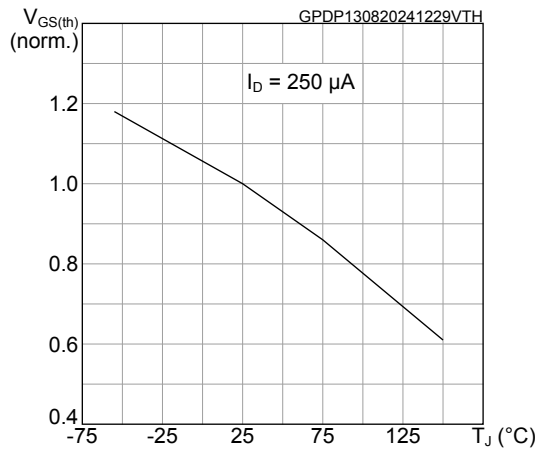
**Figure 7. Typical drain-source on-resistance**



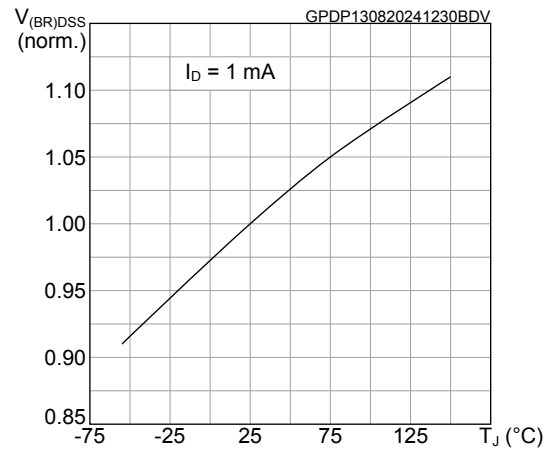
**Figure 8. Normalized on-resistance vs temperature**



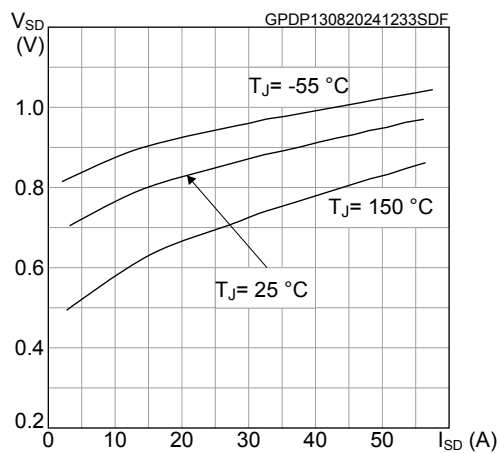
**Figure 9. Normalized gate threshold vs temperature**



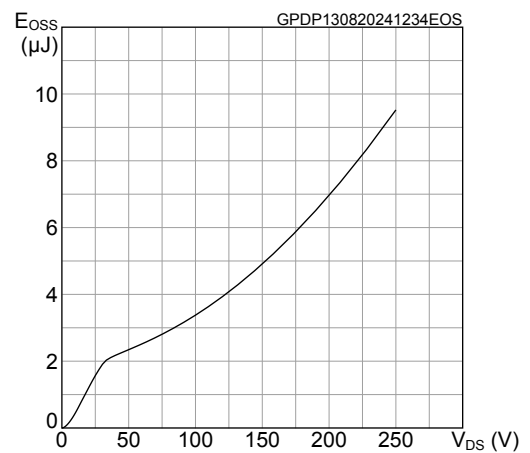
**Figure 10. Normalized breakdown voltage vs temperature**



**Figure 11. Typical reverse diode forward characteristics**

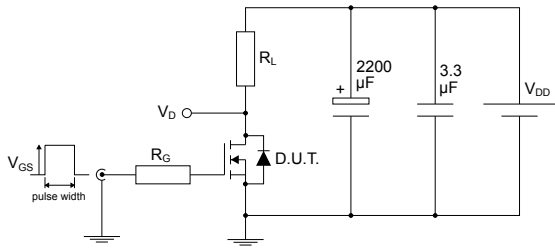


**Figure 12. Typical output capacitance stored energy**



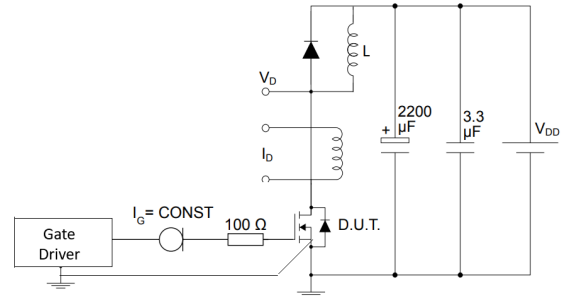
### 3 Test circuits

Figure 13. Test circuit for resistive load switching times



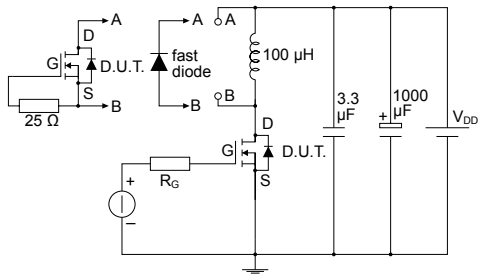
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Figure 14. Test circuit for gate charge behavior



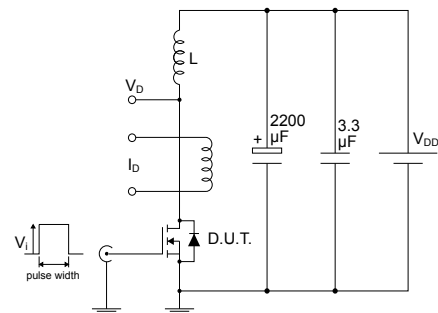
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Figure 15. Test circuit for inductive load switching and diode recovery times



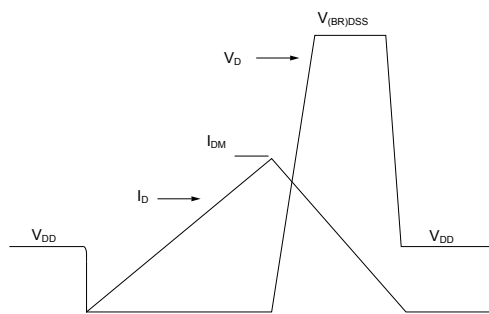
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Figure 16. Unclamped inductive load test circuit



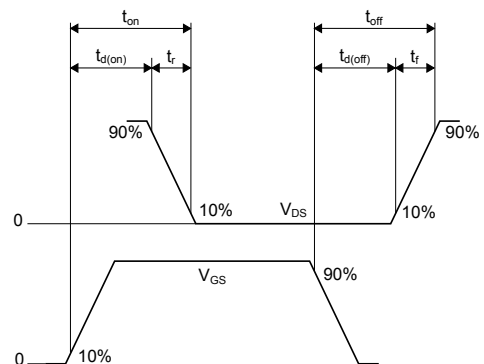
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Figure 17. Unclamped inductive waveform



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Figure 18. Switching time waveform



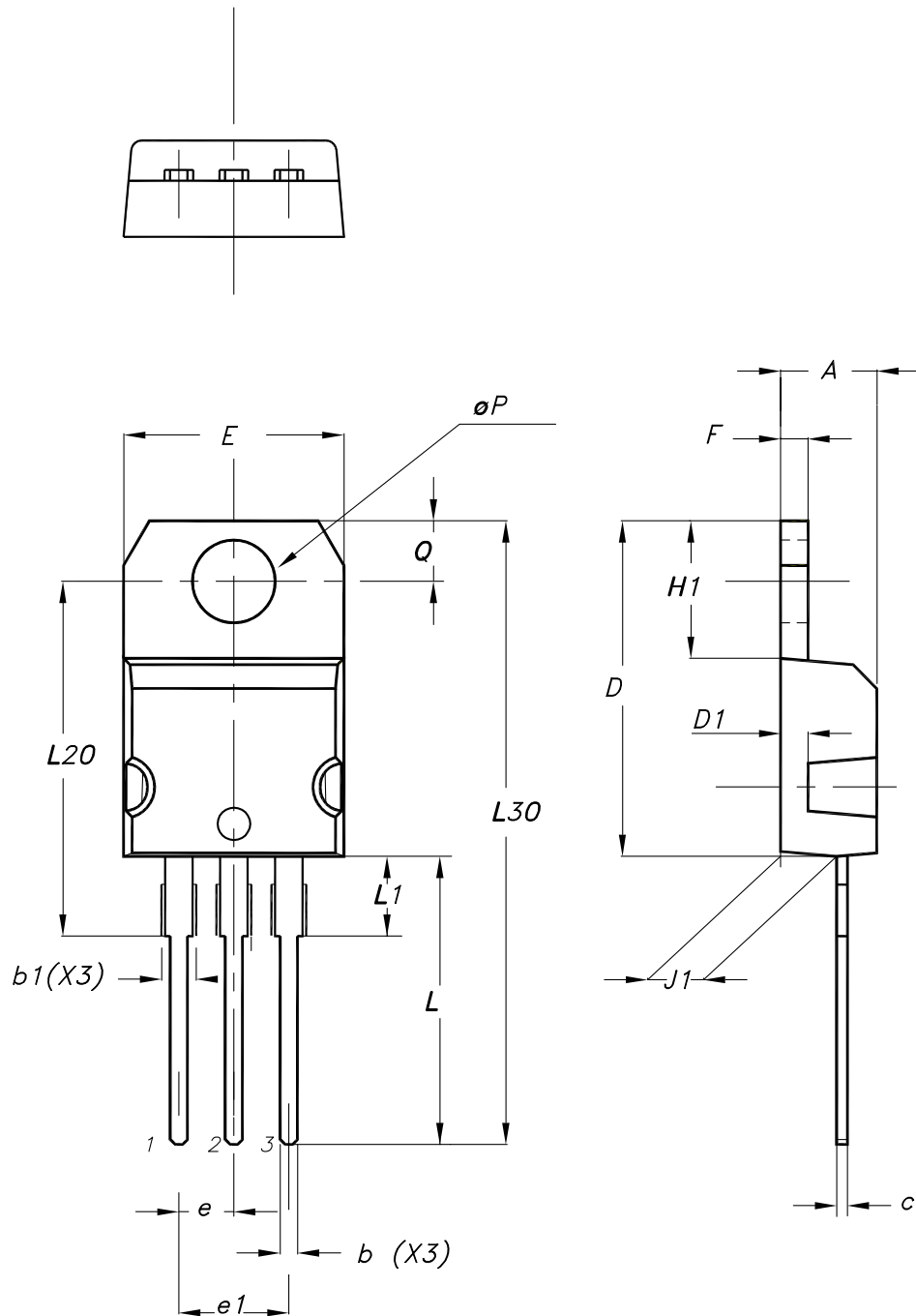
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## 4 Package information

To meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

### 4.1 TO-220 type A package information

Figure 19. TO-220 type A package outline



0015988\_typeA\_Rev\_24



**Table 8. TO-220 type A package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.55
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10.00		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13.00		14.00
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95
Slug flatness		0.03	0.10

## Revision history

**Table 9. Document revision history**

Date	Revision	Changes
20-Aug-2024	1	First release.
15-Jan-2025	2	Updated <a href="#">Features and Application</a> on cover page. Updated <a href="#">Table 5. Dynamic</a> . Updated <a href="#">Figure 5. Typical gate charge characteristics</a> and <a href="#">Figure 6. Typical capacitance characteristics</a> . Updated <a href="#">Section 3: Test circuits</a> .

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## Contents

<b>1</b>	<b>Electrical ratings</b> .....	<b>2</b>
<b>2</b>	<b>Electrical characteristics</b> .....	<b>3</b>
<b>2.1</b>	<b>Electrical characteristics (curves)</b> .....	<b>5</b>
<b>3</b>	<b>Test circuits</b> .....	<b>7</b>
<b>4</b>	<b>Package information</b> .....	<b>8</b>
<b>4.1</b>	<b>TO-220 type A package information</b> .....	<b>8</b>
	<b>Revision history</b> .....	<b>10</b>

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