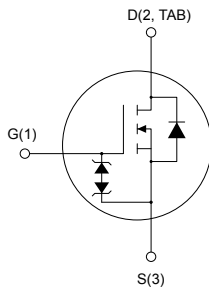
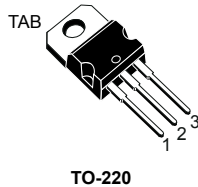


N-channel 400 V, 0.85 Ω typ., 5.4 A SuperMESH Power MOSFET in a TO-220 package



AM01476v1_tab



Product status link

[STP7NK40Z](#)

Product summary

Order code	STP7NK40Z
Marking	P7NK40Z
Package	TO-220
Packing	Tube

Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STP7NK40Z	400 V	1 Ω	5.4 A

- 100% avalanche tested
- Gate charge minimized
- Very low intrinsic capacitance
- Zener-protected

Applications

- Switching applications

Description

This high-voltage device is a Zener-protected N-channel Power MOSFET developed using the SuperMESH technology by STMicroelectronics, an optimization of the well-established PowerMESH. In addition to a significant reduction in on-resistance, this device is designed to ensure a high level of dv/dt capability for the most demanding applications.

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	400	V
V_{DGR}	Drain-gate voltage ($R_{GS} = 20\text{ k}\Omega$)	400	V
V_{GS}	Gate-source voltage	± 30	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	5.4	A
	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	3.4	
$I_{DM}^{(1)}$	Drain current (pulsed)	21.6	A
P_{TOT}	Total power dissipation at $T_C = 25\text{ }^\circ\text{C}$	70	W
ESD	Gate-source, human body model ($R = 1.5\text{ k}\Omega$, $C = 100\text{ pF}$)	3	kV
$dv/dt^{(2)}$	Peak diode recovery voltage slope	4.5	V/ns
T_{stg}	Storage temperature range	-55 to 150	$^\circ\text{C}$
T_J	Operating junction temperature range		$^\circ\text{C}$

1. Pulse width limited by safe operating area.
2. $I_{SD} \leq 5.4\text{ A}$, $di/dt \leq 200\text{ A}/\mu\text{s}$, $V_{DD} < V_{(BR)DSS}$.

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	1.78	$^\circ\text{C}/\text{W}$
R_{thJA}	Thermal resistance, junction-to-ambient	62.5	$^\circ\text{C}/\text{W}$

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width is limited by T_J max.)	5.4	A
E_{AS}	Single pulse avalanche energy (starting $T_J = 25\text{ }^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	130	mJ

2 Electrical characteristics

$T_C = 25\text{ °C}$ unless otherwise specified.

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$, $V_{GS} = 0\text{ V}$	400			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = 400\text{ V}$			1	μA
		$V_{GS} = 0\text{ V}$, $V_{DS} = 400\text{ V}$, $T_C = 125\text{ °C}^{(1)}$			50	
I_{GSS}	Gate body leakage current	$V_{GS} = \pm 20\text{ V}$, $V_{DS} = 0\text{ V}$			± 10	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 50\text{ }\mu\text{A}$	3.00	3.75	4.50	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 2.7\text{ A}$		0.85	1	Ω

1. Specified by design, not tested in production.

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 25\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$	-	535		pF
C_{oss}	Output capacitance		-	82		pF
C_{rss}	Reverse transfer capacitance		-	18		pF
$C_{oss\text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{GS} = 0\text{ V}$, $V_{DS} = 0\text{ to }320\text{ V}$	-	53		pF
Q_g	Total gate charge	$V_{DD} = 320\text{ V}$, $I_D = 5.4\text{ A}$, $V_{GS} = 0\text{ to }10\text{ V}$ (see Figure 14. Test circuit for gate charge behavior)	-	19	26	nC
Q_{gs}	Gate-source charge		-	4		nC
Q_{gd}	Gate-drain charge		-	10		nC

1. $C_{oss\text{ eq.}}$ is defined as the constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS} .

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 200\text{ V}$, $I_D = 2.7\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$	-	15	-	ns
t_r	Rise time		-	15	-	ns
$t_{d(off)}$	Turn-off delay time	(see Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform)	-	30	-	ns
t_f	Fall time		-	12	-	ns
$t_{r(voff)}$	Off-voltage rise time	$V_{DD} = 320\text{ V}$, $I_D = 5.4\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$	-	12	-	ns
t_f	Fall time		-	10	-	ns
t_c	Crossover time	(see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	20	-	ns

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		5.4	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		21.6	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 5.4 \text{ A}, V_{GS} = 0 \text{ V}$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 5.4 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s},$	-	220		ns
Q_{rr}	Reverse recovery charge	$V_{DD} = 50 \text{ V}, T_J = 150 \text{ }^\circ\text{C}$	-	990		nC
I_{RRM}	Reverse recovery current	(see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	9		A

1. Pulsed: pulse duration = 300 μs , duty cycle 1.5%.
2. Pulse width is limited by safe operating area.

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

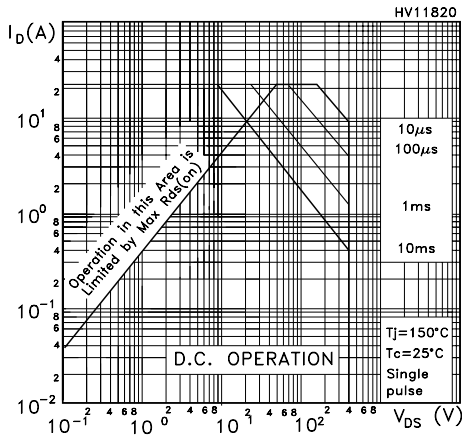


Figure 2. Thermal impedance

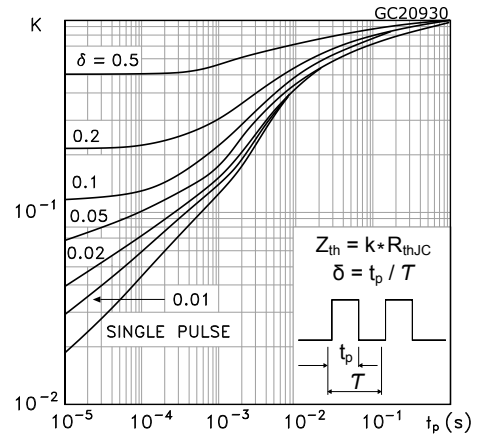


Figure 3. Output characteristics

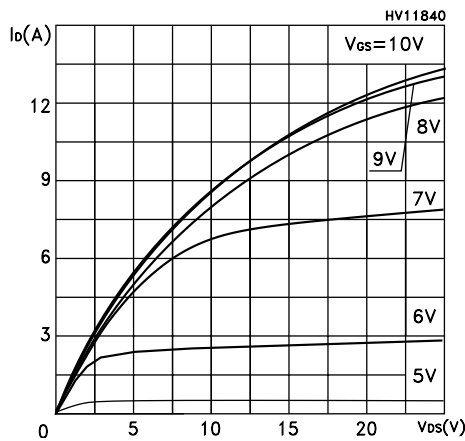


Figure 4. Transfer characteristics

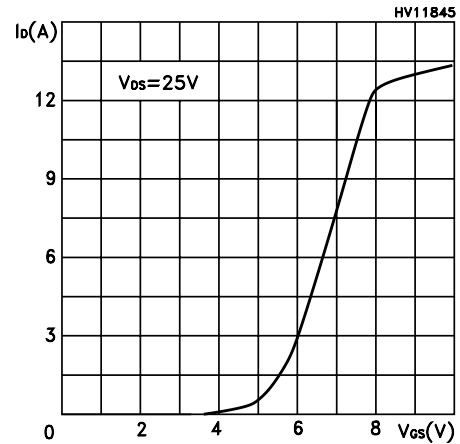


Figure 5. Static drain-source on-resistance

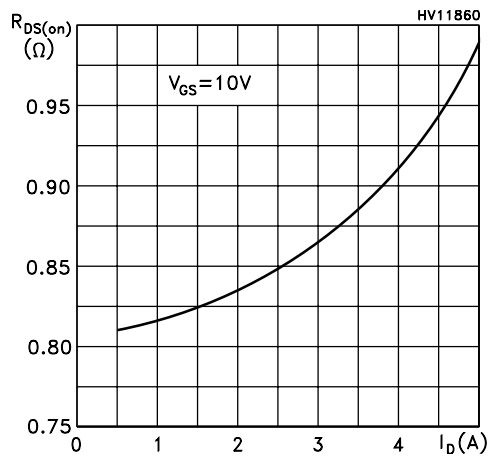


Figure 6. Gate charge vs gate-source voltage

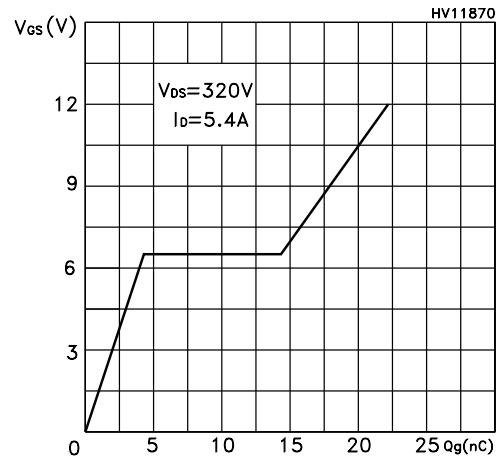


Figure 7. Capacitance variations

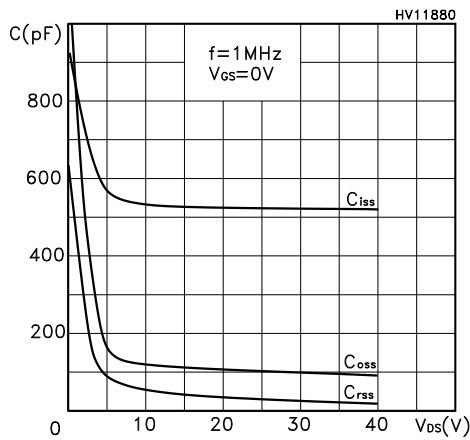


Figure 8. Normalized gate threshold voltage vs temperature

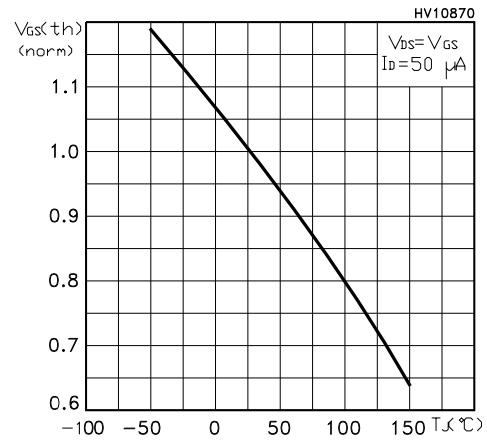


Figure 9. Normalized on-resistance vs temperature

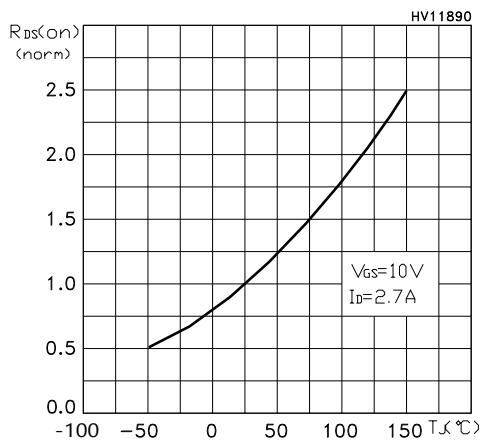


Figure 10. Source-drain diode forward characteristics

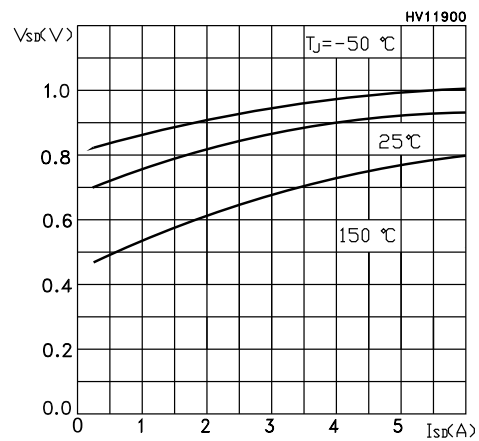


Figure 11. Normalized $V_{(BR)DSS}$ vs temperature

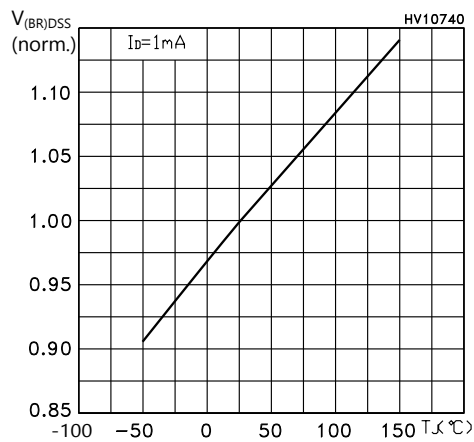
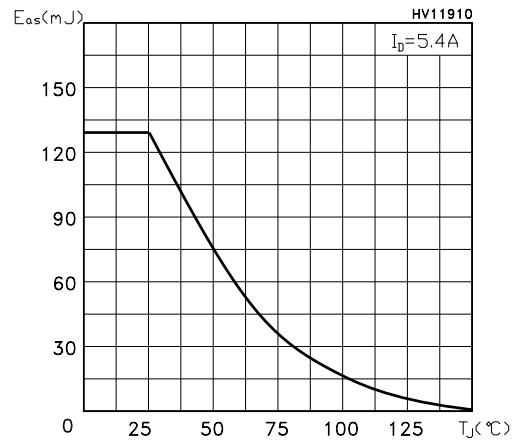


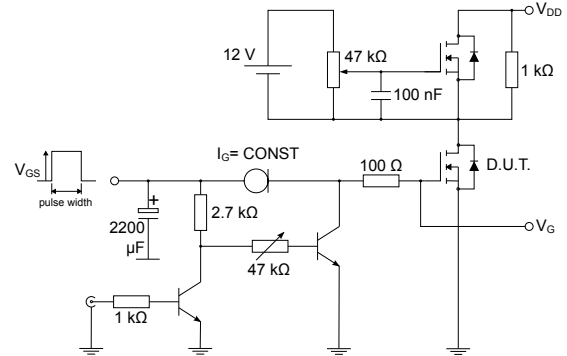
Figure 12. Maximum avalanche energy vs temperature



3 Test circuits

Figure 13. Test circuit for resistive load switching times

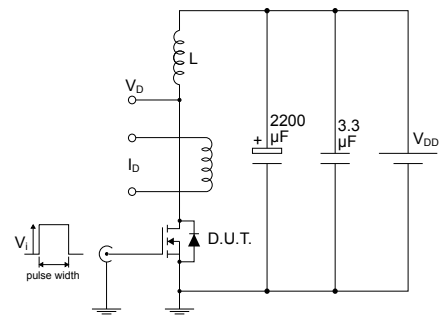

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Figure 14. Test circuit for gate charge behavior


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Figure 15. Test circuit for inductive load switching and diode recovery times


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Figure 16. Unclamped inductive load test circuit


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Figure 17. Unclamped inductive waveform


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Figure 18. Switching time waveform

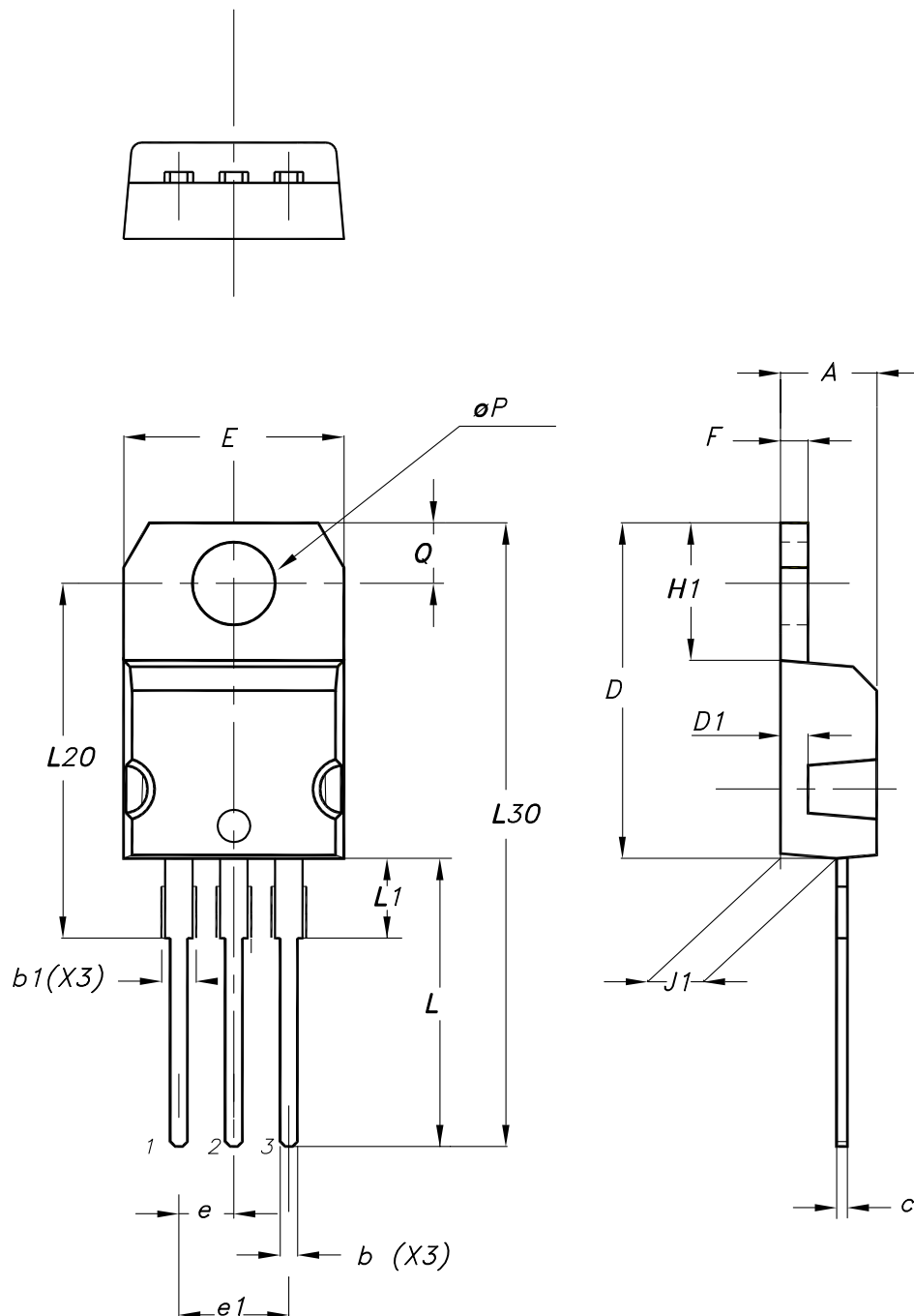

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4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 TO-220 type A package information

Figure 19. TO-220 type A package outline



0015988_typeA_Rev_23

Table 8. TO-220 type A package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.55
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10.00		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13.00		14.00
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95
Slug flatness		0.03	0.10

Revision history

Table 9. Document revision history

Date	Revision	Changes
25-May-2023	1	First release. The part number STP7NK40Z was previously inserted in the DS2855.

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