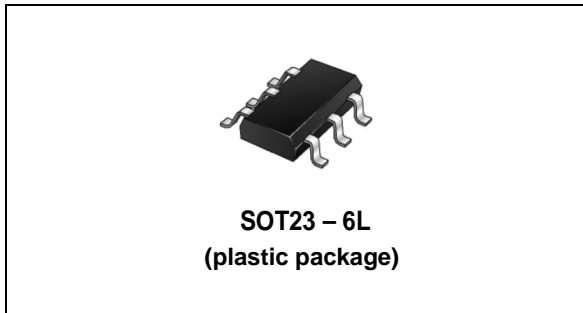


Secondary side wake-up controller

Datasheet - preliminary data



Features

- Precise voltage references: 2 V \pm 1% and 2.4 V \pm 2%, within temperature range
- Wide operating V_{DD} range (from 4.5 to 20 V)
- Low consumption during burst mode: 150 μ A
- OVP detection function during burst mode
- Internal 100 V N-channel MOSFET
- SOT23-6L micropackage

Applications

- Adapter/charger: mobile phone, tablet, camcorder, shaver, emergency light, etc. based on the primary side controller STCH01

Description

The STWK01 device is intended to operate at a converter secondary side as the wake-up controller during burst mode operation, in applications using the STCH01, a primary side advanced multi-mode power management IC (flyback-like converters).

For the correct operation of the circuit, the secondary side of the converter has to be configured connecting the rectifier diode with an anode to GND and a cathode to the proper secondary winding pin, while the output capacitor is connected to the other pin of the secondary

winding. The internal N-channel MOSFET (the source connected to GND and the drain to the OUT pin) has to be placed in parallel to the flyback converter output diode.

When at a light load or no-load the main device STCH01 enters burst mode operation and stops switching, the wake-up controller senses at the secondary side that there is no switching activity and remains waiting that the output voltage discharges down to the threshold set by an external resistive divider connected to the sensing pin V_{sns} : when the internal threshold is reached, the wake-up controller switches on the internal MOSFET for a short time interval: this allows to generate a wake-up pulse across the transformer secondary winding that, by a transformer coupling, is transferred at the primary side across the auxiliary winding connected to the primary side controller STCH01. The transferred wake-up pulse is detected by the ZCD pin of the main IC that resumes the operation.

The device generates a wake-up pulse also in case, during burst mode operation, it detects an overvoltage condition on the output.

Figure 1. Pin connections (top view)

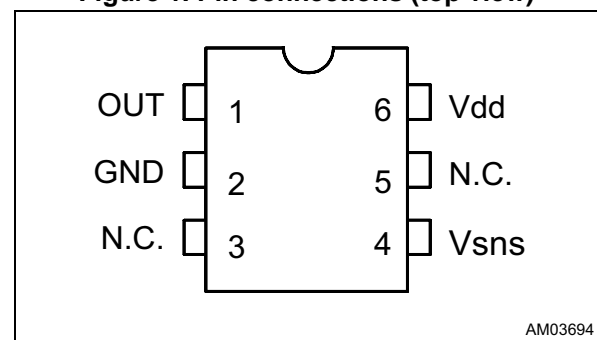


Table 1. Device summary

Order code	Package	Packing
STWK01TR	SOT23-6L	Tape and reel

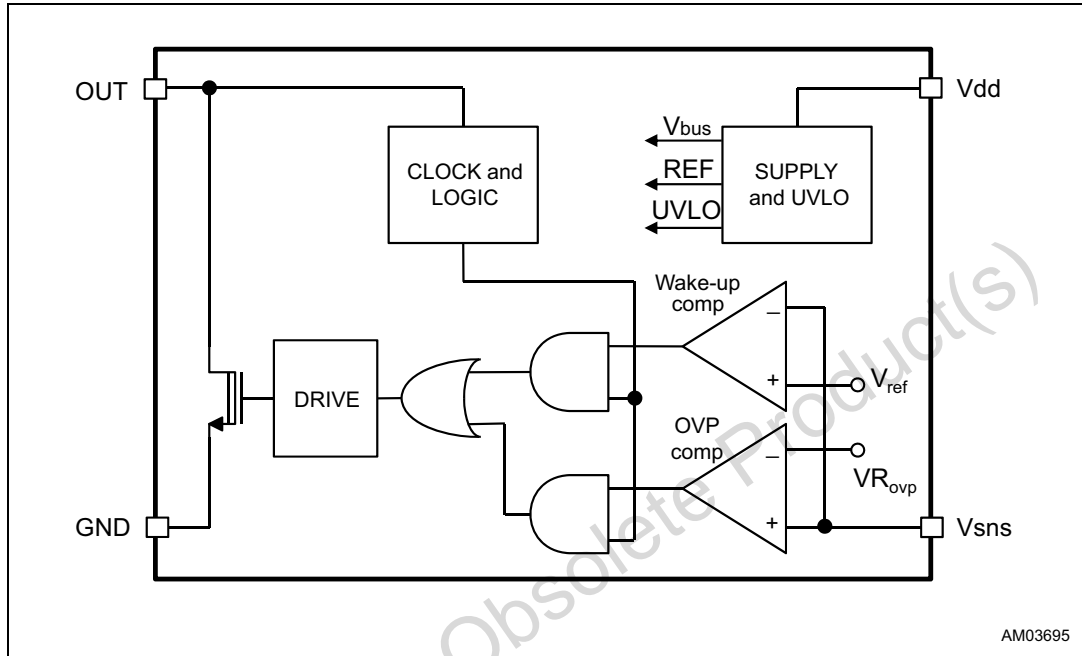
Contents

1	Block diagram	3
2	Maximum ratings	4
3	Electrical characteristics	5
4	Application information	6
5	Operation	7
	5.1 Wake-up comparator	7
	5.2 OVP comparator	8
6	Package information	9
7	Revision history	11

Obsolete Product(s) - Obsolete Product(s)

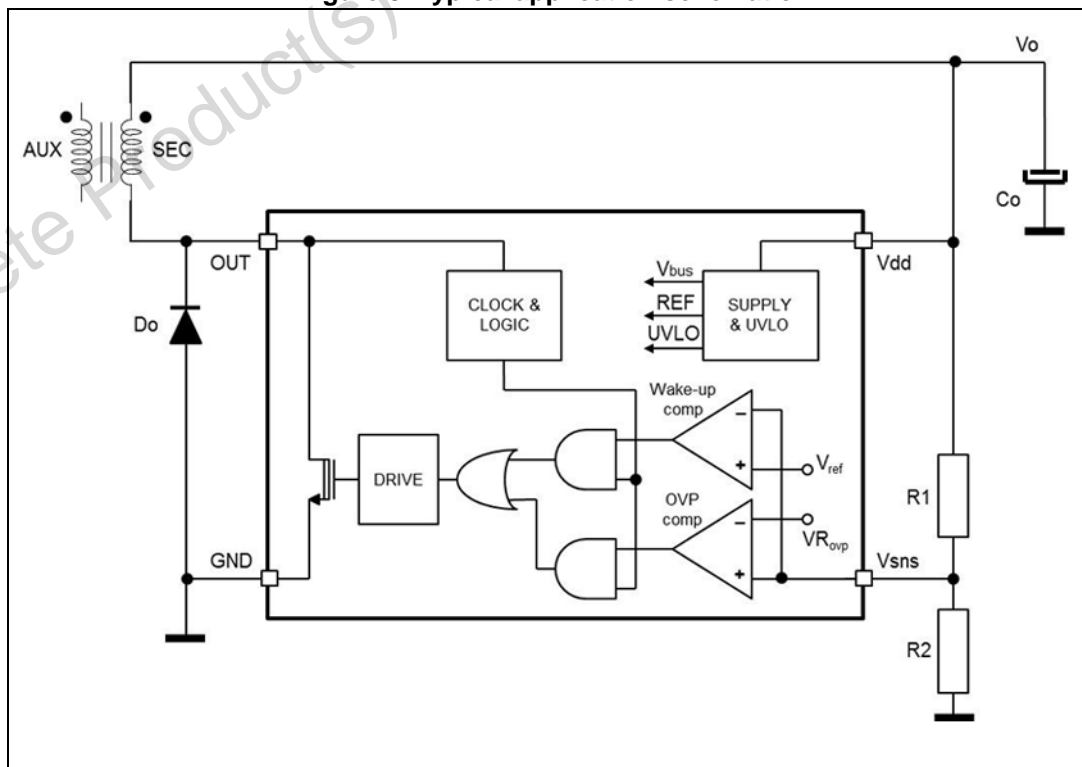
1 Block diagram

Figure 2. Block diagram



AM03695

Figure 3. Typical application schematic



2 Maximum ratings

Table 2. Absolute maximum ratings

Symbol	Pin	Parameter	Value	Unit
V _{DD}	6	Device supply voltage	-0.3 to 22	V
V _{OUT}	1	OUT pin to GND voltage	-3 to 100	V
I _{OUT}	1	Max. sink pulsed current (pulse width internally limited to 4 μs)	2.5	A
V _{sns}	4	Sense pin voltage	-0.3 to 3.6	V

Stressing the device above the rating listed in *Table 2: Absolute maximum ratings* may cause permanent damage to the device. Exposure to absolute maximum rated conditions may affect device reliability.

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R _{th j-amb}	Thermal resistance, junction to ambient	250	°C/W
P _{TOT}	Max. power dissipation at T _{amb} = 50 °C	0.4	W
T _{Jop}	Junction temperature operating range	-40 to 150	°C
T _{stg}	Storage temperature	-55 to 150	

Table 4. Pin functions

No.	Name	Function
1	OUT	The drain of the internal N-channel MOSFET: has to be connected to the cathode of the rectifier diode at secondary side of the flyback converter. Note that, for the correct operation of the circuit, the secondary side of the converter has to be configured connecting the rectifier diode with an anode to GND and a cathode to the proper secondary winding terminal, while the output capacitor is connected to the other terminal of the secondary winding.
2	GND	Return of the bias current of the device and 0 V reference for all voltages.
3	N.C.	This pin has to be connected to ground (GND).
3	GND	Return of the bias current of the device and 0 V reference for all voltages.
4	V _{sns}	Sensing input: the mid-point of a resistive divider from the converter output to GND should be connected to this pin for output voltage sensing. The sensed voltage on the pin is compared to the internal references for the wake-up and OVP function.
5	N.C.	This pin has to be connected to ground (GND).
6	V _{DD}	Supply voltage of the device. A small bypass capacitor (0.1 μF typ.) to GND, located as close to IC's pins as possible, might be useful to get a clean supply voltage.

3 Electrical characteristics

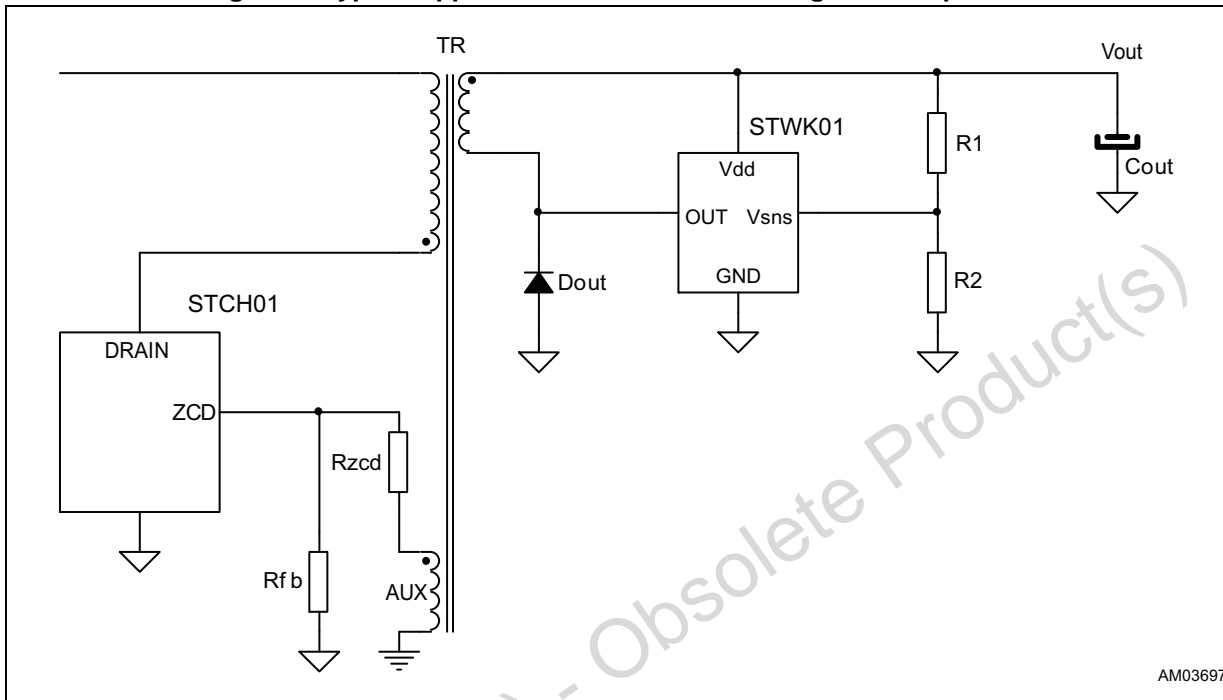
Table 5. Electrical characteristics ($T_J = -25\text{ °C}$ to 125 °C , $V_{DD} = 5\text{ V}$; unless otherwise specified)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Internal MOSFET (between OUT and GND pins)						
V_{DS_Max}	Max. operating voltage	$T_J = 25\text{ °C}$			100	V
I_{OFF}	Off state drain leakage current	$V_{DS} = 100\text{ V}$; $T_J = 125\text{ °C}$, $V_{sns} > V_{ref}$			15	μA
$R_{DS(on)}$	Static drain-source ON-resistance	$I_D = 0.5\text{ A}$; $T_J = 25\text{ °C}$		3		Ω
Supply section						
V_{DD}	Voltage operating range		4.5		20	V
V_{dd_on}	V_{dd} turn on threshold		4.45	4.6	4.75	V
V_{dd_off}	V_{dd} turn off threshold		4.2	4.35	4.5	V
V_{dd_hyst}	Turn on - turn off threshold hysteresis		190			mV
I_{DD}	Quiescent current	$V_{sns} = 2.06\text{ V}$; not switching	70		150	μA
Wake-up sensing						
V_{ref}	Wake-up comparator voltage reference	⁽¹⁾ V_{DD} within supply range, $T_J = 25\text{ °C}$	1.99	2	2.01	V
		⁽¹⁾ V_{DD} within supply range	1.98	2	2.02	
$V_{R_{ovp}}$	OVP comparator voltage reference	⁽¹⁾ V_{DD} within supply range	2.35	2.4	2.45	V
T_{pulse}	Gate drive pulse width	On comparators triggering		4		μs

1. All voltages in tracking.

4 Application information

Figure 4. Typical application schematic including STCH01 portion



5 Operation

During the burst mode this device operates at the converter secondary side as the wake-up controller, in flyback-like applications using the STCH01, a primary side advanced multi-mode power management IC.

For the correct operation of the circuit, the secondary side of the converter has to be configured connecting the output rectifier diode with an anode connected to GND and a cathode connected to the proper secondary winding terminal of the flyback transformer, while the output filter capacitor is connected to the other terminal of the secondary winding.

In very light load or no-load conditions, when the COMP pin of the STCH01 reaches the burst mode threshold V_{COMPBM} , the primary controller stops switching, entering a very low consumption state and waiting for a wake-up signal (on the ZCD pin) from the secondary side: as a result of an operation stop, the output voltage will start decreasing due to the residual load.

The operation of the wake-up device (after start-up phase) is to detect the switching activity stop and trigger the internal wake-up comparator when the output voltage is sensed below the threshold fixed by the resistive divider connected to the sense pin V_{SNS} and compared to the internal reference V_{ref} .

Referring to the block diagram in [Figure 2 on page 3](#), the clock and logic block detects the switching activity stop and only after this it enables the wake-up and OVP comparators.

On the comparator triggering, the internal N-channel MOSFET is turned on for a short time (T_{pulse}), allowing a voltage pulse to be transferred from the secondary winding to the auxiliary winding, through the transformer coupling. The resulting pulse train on the ZCD pin is detected by the primary side controller that resumes the operation. The IC implements also a snooze function: after releasing the first pulse, in case no switching activity is detected within a snooze time (22 μ sec. typ.), it releases a second wake-up pulse in order to increase the robustness of the communication between primary and secondary controllers.

The complementary operation of the primary and secondary ICs during very light load or no-load conditions allows extremely low power consumption, making the architecture suitable for those charger applications where 5-star requirements in the no-load have to be exceeded.

5.1 Wake-up comparator

The wake-up threshold is set by the R1 - R2 divider and has to be selected lower than the nominal output voltage (set at the primary side, through the resistive divider connected to the ZCD pin of the STCH01), but of course above the minimum allowed value in the specification for the output.

Once chosen this threshold V_{o_wake} and the resistor R2 of the divider, the other resistor R1 can be calculated as follows:

Equation 1

$$R1 = \left(\frac{V_{o_wake}}{V_{ref}} - 1 \right) R2$$

5.2 OVP comparator

During burst mode operation (when a switching operation stop is detected), the same resistive divider R1 - R2 is also used to sense an overvoltage condition: the sensed voltage V_{sns} is sent to the OVP comparator and compared to a second threshold VR_{ovp} that is set 20% higher than voltage reference V_{ref} . As a result, the OVP comparator triggers when the output voltage surpasses the value:

Equation 2

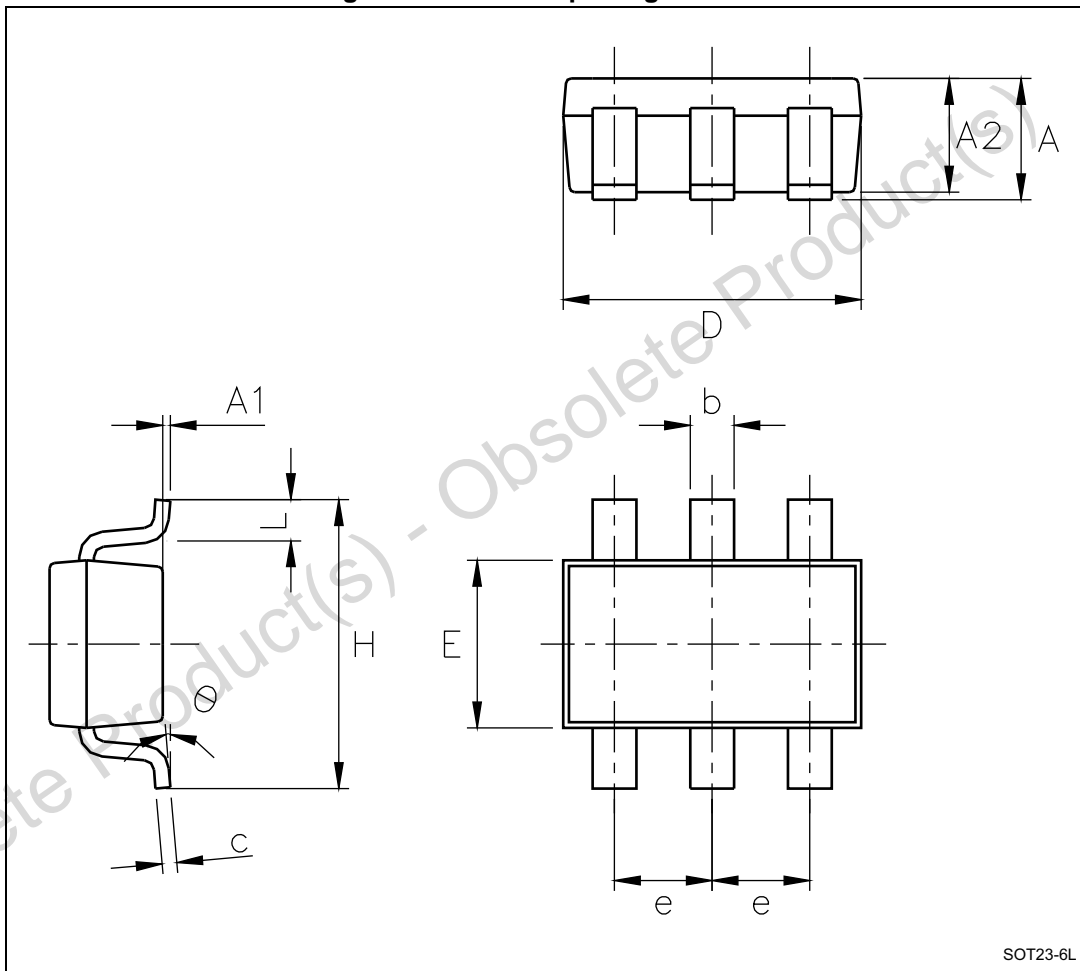
$$V_{\text{o_ovp}} = VR_{\text{ovp}} \left(\frac{R1}{R2} + 1 \right) = 1.2 \cdot V_{\text{ref}} \left(\frac{R1}{R2} + 1 \right)$$

and a wake-up pulse is transferred from the secondary to auxiliary winding, where it is detected by the ZCD pin of the STCH01. Also in this case a second pulse is released, in case no switching activity is detected within a snooze time (22 μsec . typ.).

6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Figure 5. SOT23-6L package outline



SOT23-6L

Table 6. SOT23-6L package mechanical data

Symbol	Dimensions ⁽¹⁾					
	mm.			inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A		0.9	1.45		0.035	0.057
A1		0	0.1		0	0.0039
A2		0.9	1.3		0.035	0.0512
b		0.35	0.5		0.014	0.02
c		0.09	0.2		0.004	0.008
D		2.8	3.05		0.11	0.120
E		1.5	1.75		0.059	0.0689
e	0.95			0.037		
H		2.6	3		0.102	0.118
L		0.1	0.6		0.004	0.024
Θ (degrees)		0°	10°		0°	10°

1. Dimensions per JEDEC MO178AB.

7 Revision history

Table 7. Document revision history

Date	Revision	Changes
06-Aug-2014	1	Initial release.

Obsolete Product(s) - Obsolete Product(s)

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2014 STMicroelectronics – All rights reserved