TSC1801

Datasheet

Bidirectional low-side current sensing amplifier

SOT23-6

Maturity status link
TSC1801

Features

- Wide supply voltage range: 2.0 V to 5.5 V
- Fixed gain: 20 V/V
- Total output error < 0.5%
- Offset voltage: ±200 μV max.
- Gain error: 0.1% max.
- Bandwidth: 2.1 MHz
- Extended temperature range: -40 °C to +125 °C
- Automotive grade version available
- Benefits:
  - Total error guaranteed
  - Reduced bill of material

Applications

- High bandwidth low-side current sensing
- Low-side motor control
- Power management in Solar Powered Systems
- Power management in HEV and EV

Description

The TSC1801 is a low-side current measurement amplifier. The TSC1801 is designed to sense drops across shunt resistors at low common-mode voltages. The gain value is set to 20 V/V, selectable by part number.

1 Schematic diagram

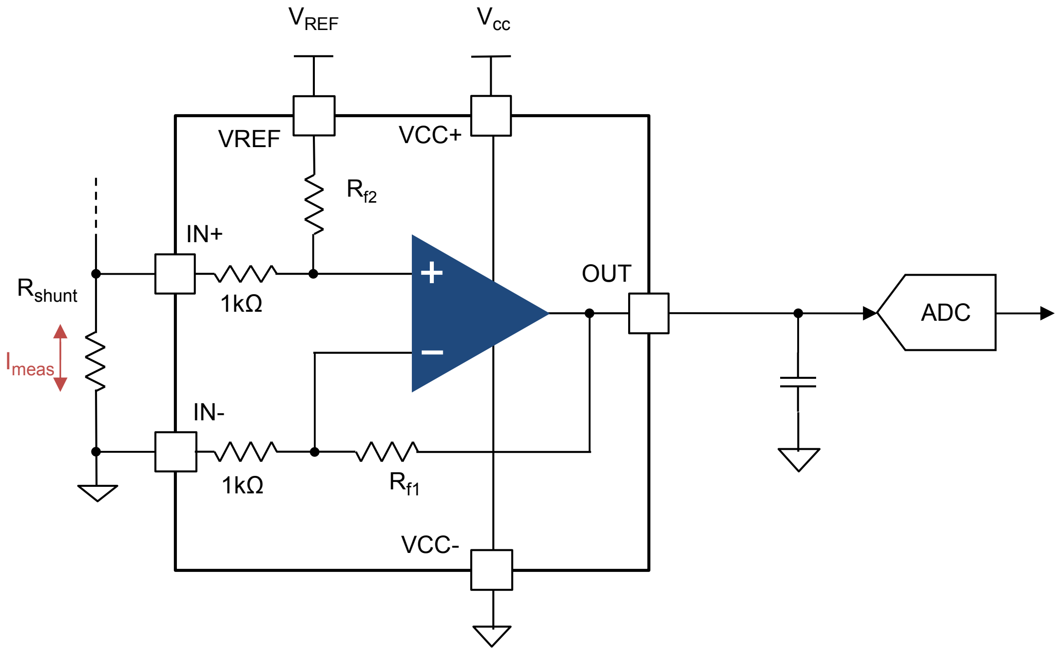


Figure 1. Internal schematic diagram

2 Pin description

Figure 2. Pin connections (top view)

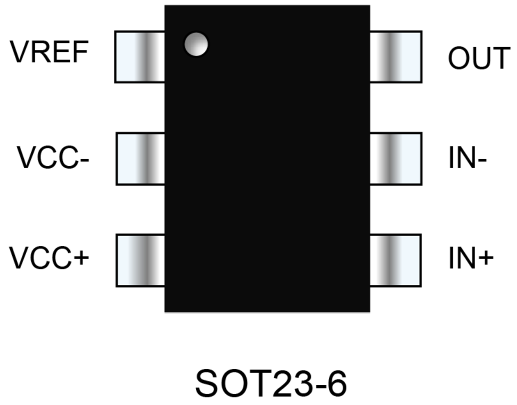


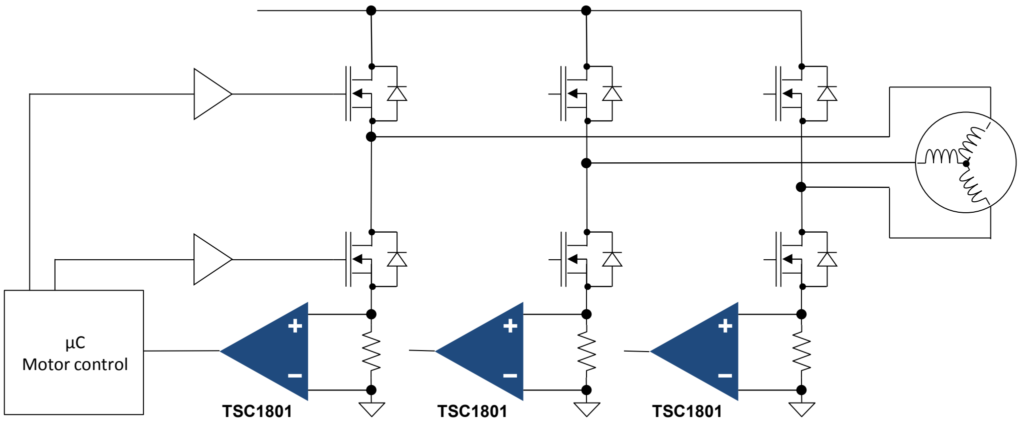
Table 1. Pin description

Pin n°	Pin name	Description
1	VREF	Voltage reference input for zero-current mid-point setting
2	VCC-	Negative supply voltage
3	VCC+	Positive supply voltage
4	IN+	Non-inverting input channel
5	IN-	Inverting input channel
6	OUT	Output channel

3 Typical application schematic

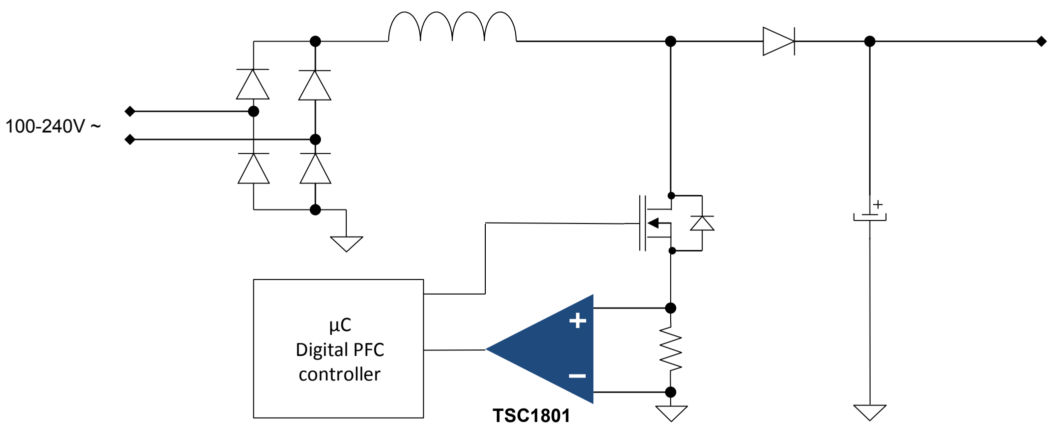
3.1 Motor control

Figure 3. 3-phase motor-control with low-side current measurement by TSC1801



3.2 PFC converter

Figure 4. Power Factor Corrector with low-side current measurement by TSC1801



4 Maximum ratings and operating conditions

Table 2. Absolute maximum ratings

Symbol	Parameter [1]	Value	Unit
VCC	Supply voltage	6	V
Vid	Input voltage differential (V_{IN+} - V_{IN-}) [2]	$\pm V_{CC}$	V
Vin	Input voltage: IN+, IN-, VREF pins [2]	(VCC-) - 0.4 to (VCC+) + 0.3	V
Iin	Input current	±10	mA
T_{stg}	Storage temperature	-65 to +150	°C
T_j	Maximum junction temperature	150	
Rth-ja [3]	Thermal resistance junction-to-ambient SOT23-6	240	°C / W
ESD	HBM: human body model (industrial grade) [4]	4	kV
	HBM: human body model (automotive grade) [5]	4	kV
	CDM: charged device model [6]	1.5	kV

1. *All voltage values are with respect to the VCC- pin, unless otherwise specified.*
2. *The maximum input voltage value may be extended to the condition that the input current is limited to ±10 mA.*
3. *Rth-ja is a typical value, obtained with PCB according to JEDEC 2s2p without vias.*
4. *Human body model: HBM test according to the standard ESDA-JS-001-2017.*
5. *Human body model: HBM test according to the standard AEC-Q100-002.*
6. *Charged device model: the CDM test is done according to the standard AEC-Q100-011.*

Table 3. Operating conditions

Symbol	Parameter	Value
V_{CC}	Supply voltage	2.0 V to 5.5 V
V_{ref}	VREF pin voltage	V_{CC-} to V_{CC+}
V_{icm}	Common-mode input voltage range	V_{CC-} – 0.1 V to V_{CC+} - 1.5 V
V_{sense}	V_{IN+} - V_{IN-} operating range with total error < 0.3%	
	Gain 20 V/V	± 122 mV
T_{oper}	Operating free air temperature range	-40 °C to +125 °C

5 Electrical characteristics

Table 4. DC electrical characteristics at V_{CC} = 3.3 V and V_{CC} = 5 V, V_{ref} = Vcc/2, V_{IN-} = 0 V, V_{sense} = V_{IN+} - V_{IN-} = 0 V, T = 25 °C, C_L = 47 pF and R_L = 10 kΩ connected to V_{CC}/2 (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Gain	TSC1801B			20		V/V
ΔV_{OUT}	Total output error Gain = 20, V_{CC} = 5 V, Vsense = +/-100 mV [1]	T = 25 °C			± 0.5	%
		-40 °C ≤ T ≤ 125 °C			± 1	
Eg	Gain error	100 mV < V_{out} < V_{cc} - 150 mV, T = 25 °C			0.1	%
		100 mV < V_{out} < V_{cc} - 150 mV, -40 °C ≤ T ≤ 125 °C			0.15	
V_{io}	Input offset voltage, referred to input	T = 25 °C		± 50	± 200	µV
		-40 °C ≤ T ≤ 125 °C			± 700	
$\Delta V_{io}/\Delta T$	Input offset voltage temperature drift	-40 °C ≤ T ≤ 125 °C			± 5	µV/°C
R_{diff}	Differential input resistor			2		kΩ
ΔEg/ΔT	Gain error drift				10	ppm/°C
NLE	Non-linearity error	100 mV < V_{out} < V_{cc} - 150 mV		±0.01		%
CMR	Common-mode rejection ratio 20.log ($\Delta V_{io}/\Delta V_{icm}$)	V_{CC-} ≤ V_{icm} ≤ V_{CC+}- 1.5 V, T = 25 °C	83	100		dB
		V_{CC-} ≤ V_{icm} ≤ V_{CC+}- 1.5 V, -40 °C ≤ T ≤ 125 °C	83	100		
REFR	Reference voltage rejection ratio 20.log ($\Delta V_{io}/\Delta V_{ref}$)	10%.V_{CC} ≤ V_{ref} ≤ 90%.V_{CC}, T = 25 °C	85	100		dB
		10%.V_{CC} ≤ V_{ref} ≤ 90%.V_{CC}, -40 °C ≤ T ≤ 125 °C	85	100		
SVR	Supply-voltage rejection ratio 20.log($\Delta V_{io}/\Delta V_{CC}$)	2.0 V ≤ V_{CC} ≤ 5.5 V, T = 25 °C		109		dB
		2.0 V ≤ V_{CC} ≤ 5.5 V, -40 °C ≤ T ≤ 125 °C	90	108		
V_{OH}	High-level output voltage drop (V_{OH} = V_{CC+} - V_{OUT})	V_{sense} = 1 V, T = 25 °C			20	mV
		V_{sense} = 1 V, -40 °C ≤ T ≤ 125 °C			25	
V_{OL}	Low-level output voltage drop (V_{OL} = V_{OUT})	V_{sense} = - 1 V, T = 25 °C			10	mV
		V_{sense} = - 1 V, -40 °C ≤ T ≤ 125 °C			20	
I_{OUT}	I_{SINK}, V_{sense} = - 1 V	Output shorted to V_{CC+}, T = 25 °C	55	70		mA
		Output shorted to V_{CC+}, -40 °C ≤ T ≤ 125 °C	40			
	I_{SOURCE}, V_{sense} = 1 V	Output shorted to V_{CC-}, T = 25 °C	50	63		
		Output shorted to V_{CC-}, -40 °C ≤ T ≤ 125 °C	40			
C_{Lmax}	Maximum capacitive load Gain = 20	No sustained oscillations		1		nF
$\Delta V_{out}/\Delta I_{out}$	Load regulation	-10 mA ≤ I_{out} ≤ 10 mA		0.3	2	mV/mA
Power supply						
I_{CC}	Supply current V_{IN+} = V_{IN-}= V_{CC}/2	T = 25 °C		3.3	3.6	mA
		-40 °C ≤ T ≤ 125 °C			3.6	

1. *Total output error defined by the formula:* $\Delta Vout = \frac{Voutmeas - Vsense \cdot Gain - Vref}{Vsense \cdot Gain}$

Table 5. AC electrical characteristics at V_{CC} = 3.3 V and V_{CC} = 5 V, V_{ref} = $V_{CC}/2$, V_{IN-} = 0 V, V_{sense} = V_{IN+} - V_{IN-} = 0 V, T = 25 °C, C_L = 47 pF and R_L = 10 kΩ connected to $V_{CC}/2$ (unless otherwise specified)

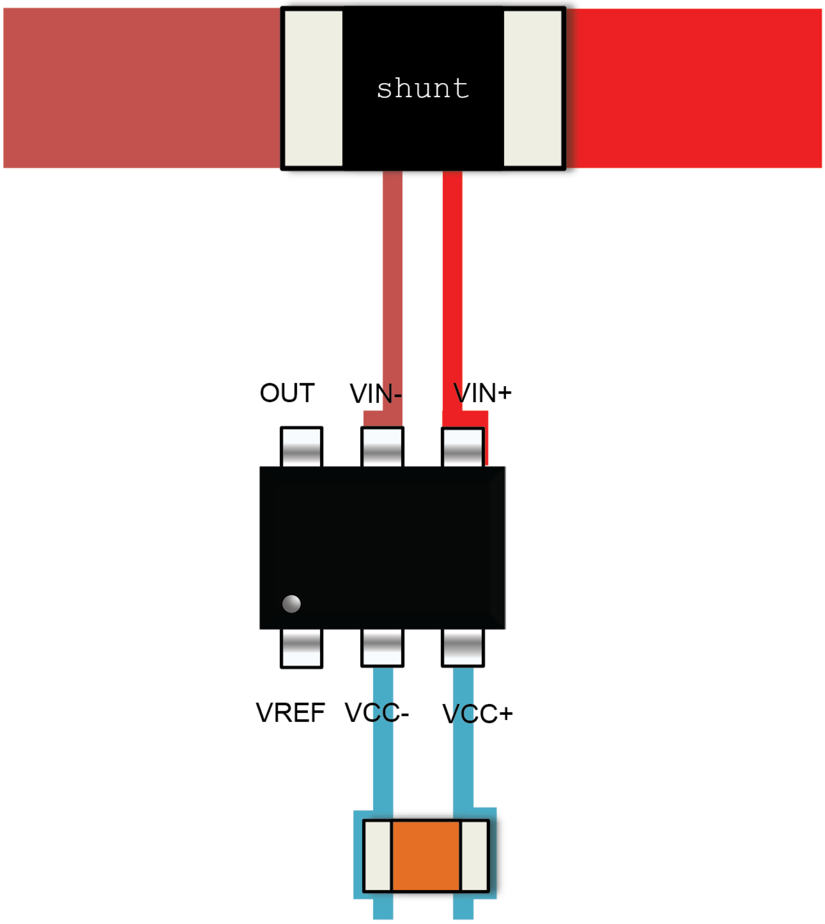
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
		AC performance				
BW	Bandwidth at -3 dB	Gain 20 V/V		2.1		MHz
SR	Slew rate, V_{out} 10% to 90%	V_{out} from 300 mV to V_{cc} - 300 mV		14		V/µs
en	Input voltage noise density	f = 10 Hz		170		nV/√Hz
		f = 100 Hz		50		
		f = 10 kHz		9		
en p-p	Input noise voltage Gain = 20	0.1 Hz ≤ f ≤ 10 Hz		8		μV_{pp}
t_S	Settling time	V_{sense} = 0 to 40 mV, V_{out} ± 1%		300		ns
t_{init}	Initialization time	V_{sense} = 40 mV, V_{out} ± 1%		25		µs
EMIRR	EMI rejection ratio EMIRR = 20 log ($V_{RF}/\Delta V_{io}$)	V_{RF} = 200 $mV_{peak-peak}$, f = 400 MHz		60		dB
		V_{RF} = 200 $mV_{peak-peak}$, f = 900 MHz		85		
		V_{RF} = 200 $mV_{peak-peak}$, f = 1800 MHz		90		
		V_{RF} = 200 $mV_{peak-peak}$, f = 2400 MHz		90		

6 Application information

6.1 PCB layout recommendations

Particular attention must be paid to the layout of the PCB tracks connected to the amplifier, load, and power supply. The power and ground traces are critical as they must provide adequate energy and grounding for all circuits. The best practice is to use short and wide PCB traces to minimize voltage drops and parasitic inductance. In addition, to minimize parasitic impedance over the entire surface, a multi-via technique that connects the bottom and top layer ground planes together in many locations is often used. The copper traces that connect the output pins to the load and supply pins should be as wide as possible to minimize trace resistance.

Figure 5. PCB traces



6.2 Decoupling capacitor

In order to ensure op amp full functionality, it is mandatory to place a decoupling capacitor of at least 22 nF as close as possible to the op amp supply pin. A good decoupling helps to reduce electromagnetic interference impact.

6.3 Macromodel

Accurate macromodels of the TSC1801 device are available on the STMicroelectronics' website at: www.st.com. These models are a trade-off between accuracy and complexity (that is, time simulation) of the TSC1801 operational amplifier. They emulate the nominal performance of a typical device within the specified operating conditions mentioned in the datasheet. They also help to validate a design approach and to select the right operational amplifier, but they do not replace on-board measurements.

7 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

7.1 SOT23-6 package information

Figure 6. SOT23-6 package outline

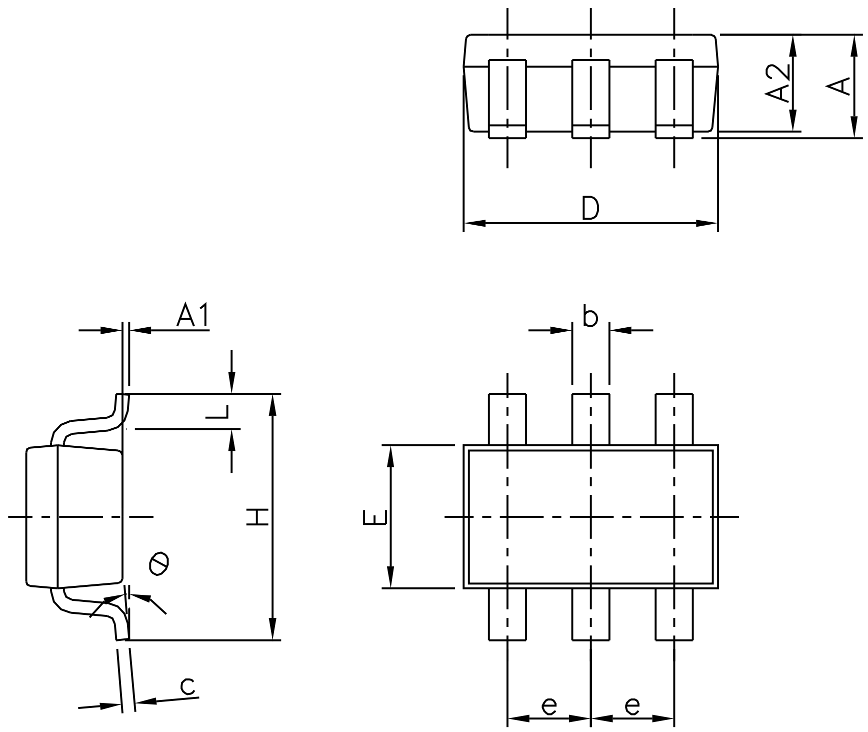


Table 6. SOT23-6 mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.90		1.45	0.035		0.057
A1			0.10			0.004
A2	0.90		1.30	0.035		0.051
b	0.35		0.50	0.013		0.019
c	0.09		0.20	0.003		0.008
D	2.80		3.05	0.110		0.120
E	1.50		1.75	0.060		0.069
e		0.95			0.037	
H	2.60		3.00	0.102		0.118
L	0.10		0.60	0.004		0.024
θ	0 °		10 °	0 °		10 °

8 Ordering information

Table 7. Order codes

Order code	Temperature range	Package	Marking
TSC1801BILT	-40 °C to 125 °C	SOT23-6	K314
TSC1801BIYLT	-40 °C to 125 °C automotive grade [1]	SOT23-6	K317

1. *Qualified and characterized according to AEC-Q100 and Q003 or equivalent, advanced screening according to AEC Q001 and Q002 or equivalent. For qualification status details, click on the "Maturity Status Link" on the datasheet first page. On the product page in www.st.com, check "Quality and Reliability" tab.*

Revision history

Table 8. **Document revision history**

Date	Revision	Changes
11-Dec-2024	1	Initial release.

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