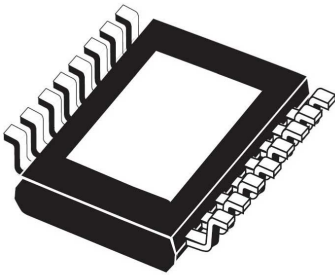


Quad channel high-side driver with Current Sense analog feedback for automotive applications



PowerSSO-16

Features

Description	Parameter	Value
Max transient supply voltage	V_{CC}	36 V
Operating voltage range	V_{CC}	4 to 28 V
Typ. on-state resistance (per Ch)	R_{ON}	86 m Ω
Current limitation (typ)	I_{LIMH}	13.6 A
Standby current (max)	I_{STBY}	0.5 μ A



- AEC-Q100 qualified
- Extreme low voltage operation for deep cold cranking applications (compliant with LV124, revision 2013)
- General
 - Quad channel smart high-side driver with current sense analog feedback
 - Very low standby current
 - Compatible with 3 V and 5 V CMOS outputs
- CurrentSense diagnostic functions
 - Multiplexed analog feedback of: load current with high precision proportional current mirror
 - Overload and short to ground (power limitation) indication
 - Thermal shutdown indication
 - OFF-state open-load detection (with external pull-up)
 - Output short to V_{CC} detection
 - Sense enable/disable
- Protections
 - Undervoltage shutdown
 - Overvoltage clamp
 - Load current limitation
 - Self limiting of fast thermal transients
 - Configurable latch-off on overtemperature or power limitation with dedicated fault reset pin
 - Loss of ground and loss of V_{CC}
 - Reverse battery with external components
 - Electrostatic discharge protection

Product status link	
VNQ9080AJ	
Product summary	
Order code	VNQ9080AJTR
Package	PowerSSO-16
Packing	Tape and reel

Applications

- Automotive resistive, inductive and capacitive loads
- Protected supply for ADAS systems: radars and sensors
- Automotive signal lamp: R10W and LEDs

Description

The device is a quad channel high-side driver manufactured using ST proprietary VIPower M0-9 technology and housed in PowerSSO-16 package. The device is designed to drive 12 V automotive grounded loads through a 3 V and 5 V CMOS-compatible interface, providing protection and diagnostics.

The device integrates advanced protective functions such as load current limitation, overload active management by power limitation and overtemperature shutdown with configurable latch-off.

A $\overline{\text{FaultRST}}$ pin unlatches the output in case of fault or disables the latch-off functionality.

A dedicated multifunction multiplexed analog output pin delivers diagnostic functions including high precision proportional load current sense, in addition to the detection of overload and short circuit to ground, short to V_{CC} and OFF-state open-load.

A sense enable pin allows OFF-state diagnosis to be disabled during the module low-power mode as well as external sense resistor sharing among similar devices.

1 Block diagram and pin description

Figure 1. Block diagram

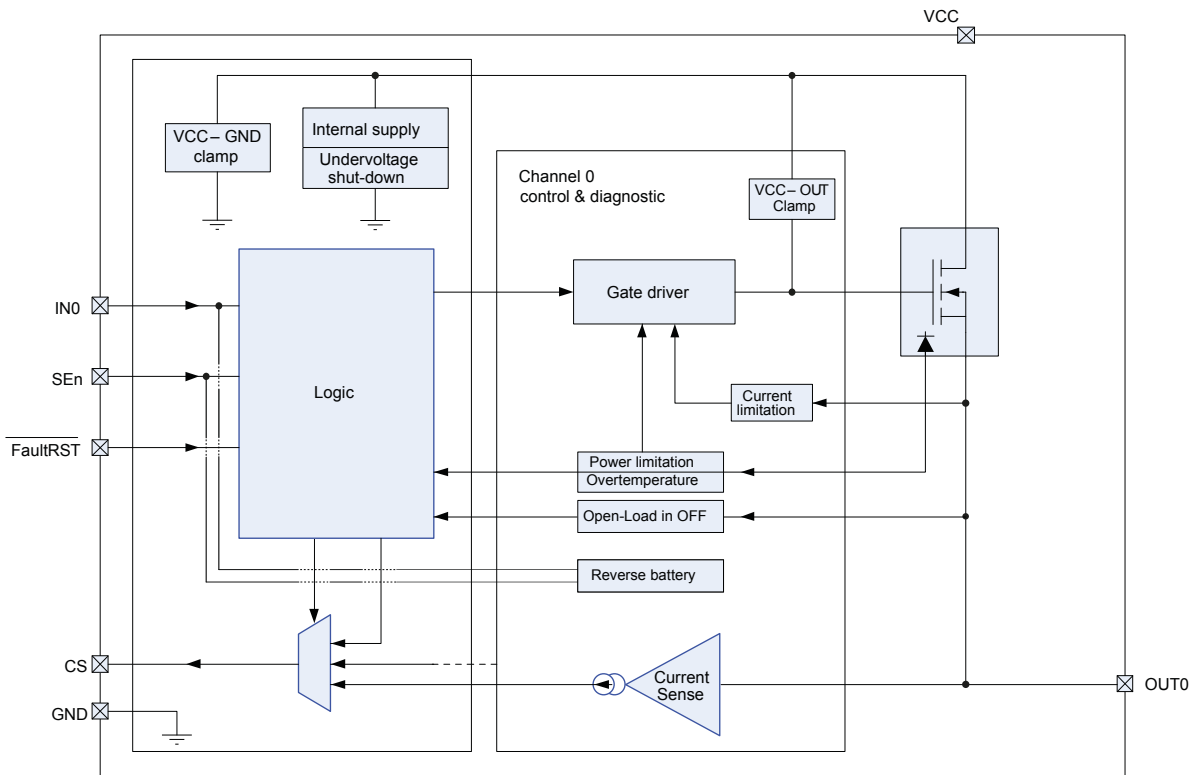
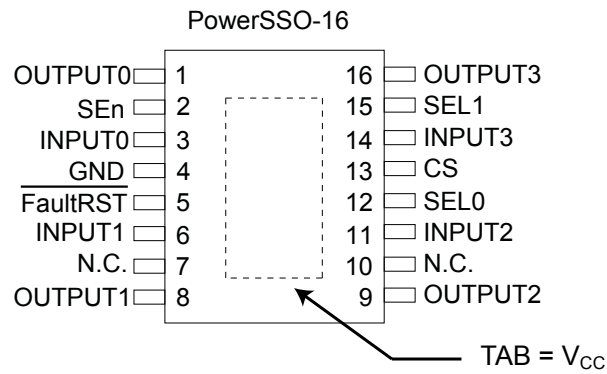


Table 1. Pin functions

Name	Function
V _{CC}	Battery connection.
OUTPUT _{0,1,2,3}	Power output
GND	Ground connection; must be reverse battery protected by an external diode / resistor network.
INPUT _{0,1,2,3}	Voltage controlled input pin with hysteresis, compatible with 3 V and 5 V CMOS outputs; controls output switch state.
CS	analog current sense output pin; it delivers a current proportional to the selected load current.
SEn	Active high compatible with 3 V and 5 V CMOS outputs pin; enables the CS diagnostic pin.
SEL _{0,1}	Active high compatible with 3 V and 5 V CMOS outputs pin; it addresses the CS multiplexer.
FaultRST	Active low compatible with 3 V and 5 V CMOS outputs pin; it unlatches the output in case of fault - if kept low, sets the output to auto-restart mode.

Figure 2. Configuration diagram (top view)



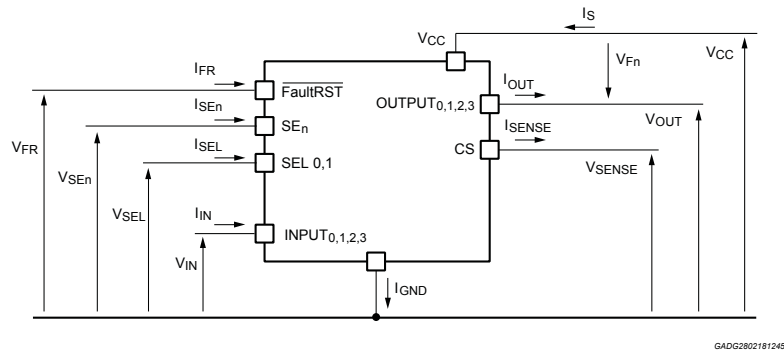
GADG010318144RI

Table 2. Suggested connections for unused and not connected pins

Connection/pin	CS	NC	Output	Input	SEn, SELx, FaultRST
Floating	Not allowed	X	X ⁽¹⁾	X	X
To ground	Through 1 kΩ resistor	X	Not allowed	Through 15 kΩ resistor	Through 15 kΩ resistor

1. X: do not care.

2 Electrical specification

Figure 3. Current and voltage conventions


Note: $V_{FN} = V_{OUTn} - V_{CC}$ during reverse battery condition.

2.1 Absolute maximum ratings

Stressing the device above the rating listed in Table 3. Absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to the conditions in the table below for extended periods may affect the device reliability.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage	36	V
$-V_{CC}$	Reverse DC supply voltage	0.3	
V_{CCJS}	Maximum jump start voltage for single pulse short circuit protection	28	V
$-I_{GND}$	DC reverse ground pin current	200	mA
I_{OUT}	OUTPUT _{0,1,2,3} DC output current	Internally limited	A
$-I_{OUT}$	Reverse DC output current	2.2	
I_{IN}	INPUT _{0,1,2,3} DC input current	-1 to 10	mA
I_{SEn}	SEn DC input current	-1 to 3	
$I_{SEL0,1}$	SEL _{0,1} DC input current	-1 to 10	
I_{FR}	$\overline{\text{FaultRST}}$ DC input current		
I_{SENSE}	CS pin DC output current ($V_{GND} = V_{CC}$ and $V_{SENSE} < 0$ V)	10	mA
	CS pin DC output current in reverse ($V_{CC} < 0$ V)	-20	
E_{MAX}	Maximum switching energy (single pulse); $T_{jstart} = 150$ °C)	4	mJ
V_{ESD}	Electrostatic discharge (JEDEC 22A-114F)		
	INPUT _{0,1,2,3}	2000	V
	CS	2000	
	SEn, SEL _{0,1} , $\overline{\text{FaultRST}}$	2000	
OUTPUT _{0,1,2,3}	4000		

Symbol	Parameter	Value	Unit
V _{ESD}	V _{CC}	4000	V
V _{ESD}	Charge device model (CDM-AEC-Q100-011)	750	V
T _J	Junction operating temperature	-40 to 150	°C
T _{stg}	Storage temperature	-55 to 150	

2.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Typ. value	Unit
R _{thj-board}	Thermal resistance junction-board (JEDEC JESD 51-5 / 51-8) ⁽¹⁾⁽²⁾	9.5	°C/W
R _{thj-amb}	Thermal resistance junction-ambient (JEDEC JESD 51-5) ⁽¹⁾⁽³⁾	54.5	
R _{thj-amb}	Thermal resistance junction-ambient (JEDEC JESD 51-7) ⁽¹⁾⁽²⁾	22.5	

1. *One channel ON.*
2. *Device mounted on four-layer 2s2p PCB.*
3. *Device mounted on two-layer 2s0p PCB with 2 cm² heatsink copper trace.*

2.3 Main electrical characteristics

7 V < V_{CC} < 28 V; -40 °C < T_j < 150 °C, unless otherwise specified.

All typical values refer to V_{CC} = 13 V; T_j = 25 °C, unless otherwise specified.

Table 5. Power section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{CC}	Operating supply voltage		4	13	28	V
V _{USD}	Undervoltage shutdown			2.1	2.7	V
V _{USDReset}	Undervoltage shutdown reset				4.5	V
V _{USDhyst}	Undervoltage shutdown hysteresis			0.15		V
R _{ON}	On-state resistance ⁽¹⁾	I _{OUT} = 0.7 A; T _j = 25 °C		86		mΩ
		I _{OUT} = 0.7 A; T _j = 150 °C			190	
		I _{OUT} = 0.7 A; V _{CC} = 4 V; T _j = 25 °C			149	
		I _{OUT} = 0.07 A; V _{CC} = 2.7 V; V _{CC} decreasing			516	
V _{clamp}	Clamp voltage	I _S = 20 mA; 25 °C < T _j < 150 °C	36	38	45	V
		I _S = 20 mA; T _j = -40 °C	36			V
I _{STBY}	Supply current in standby at V _{CC} = 13 V ⁽²⁾	V _{CC} = 13 V; V _{IN0,1,2,3} = V _{OUT0,1,2,3} = V _{FR} = V _{SEn} = 0 V; V _{SEL0,1} = 0 V; T _j = 25 °C			0.5	μA
		V _{CC} = 13 V; V _{IN0,1,2,3} = V _{OUT0,1,2,3} = V _{FR} = V _{SEn} = 0 V; V _{SEL0,1} = 0; T _j = 85 °C ⁽³⁾			0.5	
		V _{CC} = 13 V; V _{IN0,1,2,3} = V _{OUT0,1,2,3} = V _{FR} = V _{SEn} = 0 V; V _{SEL0,1} = 0 V; T _j = 125 °C			3	
t _{D_STBY}	Standby mode blanking time	V _{CC} = 13 V; V _{IN} = V _{OUT} = V _{FR} = V _{SEL0,1} = 0 V; V _{SEn} = 5 V to 0 V	60	260	550	μs
I _{S(ON)}	Supply current	V _{CC} = 13 V; V _{SEn} = V _{FR} = V _{SEL0,1} = 0 V; V _{IN0,1,2,3} = 5 V; I _{OUT0,1,2,3} = 0 A		5.5	7.5	mA
I _{GND(ON)}	Control stage current consumption in ON state. All channels active.	V _{CC} = 13 V; V _{SEn} = 5 V; V _{FR} = V _{SEL0,1} = 0 V; V _{IN0,1,2,3} = 5 V; I _{OUT0,1,2,3} = 0.7 A;			9	mA
I _{L(off)}	Off-state output current at V _{CC} = 13 V ⁽²⁾	V _{IN0,1,2,3} = V _{OUT0,1,2,3} = 0 V; V _{CC} = 13 V; T _j = 25 °C	0	0.01	0.5	μA
		V _{IN0,1,2,3} = V _{OUT0,1,2,3} = 0 V; V _{CC} = 13 V; T _j = 125 °C	0		3	
V _F	Output - V _{CC} diode voltage at T _j = 150 °C	I _{OUT} = -0.7 A; T _j = 150 °C			0.7	V

1. For each channel.
2. Power MOSFET leakage included.
3. Parameter specified by design; not subject to production test.

Table 6. Switching

V _{CC} = 13 V; -40 °C < T _j < 150 °C, unless otherwise specified						
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t _{d(on)} ⁽¹⁾	Turn-on delay time at T _j = 25 °C	R _L = 18.6 Ω	10	26	120	μs
t _{d(off)} ⁽¹⁾	Turn-off delay time at T _j = 25 °C		10	30	100	
(dV _{OUT} /dt) _{on} ⁽¹⁾	Turn-on voltage slope at T _j = 25 °C		0.2	0.42	0.7	V/μs
(dV _{OUT} /dt) _{off} ⁽¹⁾	Turn-off voltage slope at T _j = 25 °C		0.2	0.45	0.7	
W _{ON}	Switching energy losses at turn-on (t _{won})			0.06	0.095 ⁽²⁾	mJ
W _{OFF}	Switching energy losses at turn-off (t _{woff})			0.06	0.095 ⁽²⁾	mJ
t _{SKEW}	Differential pulse skew (t _{PHL} - t _{PLH})			-45	5	55

1. See Figure 4. *Switching time and pulse skew.*
2. *Specified by design and evaluated by characterization, not tested in production.*

Table 7. Logic inputs

7 V < V _{CC} < 28 V; -40 °C < T _j < 150 °C						
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
INPUT _{0,1,2,3} characteristics						
V _{IL}	Input low level voltage				0.9	V
I _{IL}	Low level input current	V _{IN} = 0.9 V	1			μA
V _{IH}	Input high level voltage		2.1			V
I _{IH}	High level input current	V _{IN} = 2.1 V			10	μA
V _{I(hyst)}	Input hysteresis voltage		0.2			V
V _{ICL}	Input clamp voltage	I _{IN} = 1 mA	6		8.5	V
		I _{IN} = -1 mA		-0.7		
FaultRST characteristics						
V _{FRL}	Input low level voltage				0.9	V
I _{FRL}	Low level input current	V _{IN} = 0.9 V	1			μA
V _{FRH}	Input high level voltage		2.1			V
I _{FRH}	High level input current	V _{IN} = 2.1 V			10	μA
V _{FR(hyst)}	Input hysteresis voltage		0.2			V
V _{FRCL}	Input clamp voltage	I _{IN} = 1 mA	6		8.5	V
		I _{IN} = -1 mA		-0.7		
SEL _{0,1} characteristics (7 V < V _{CC} < 18 V)						
V _{SELL}	Input low level voltage				0.9	V
I _{SELL}	Low level input current	V _{IN} = 0.9 V	1			μA
V _{SELH}	Input high level voltage		2.1			V
I _{SELH}	High level input current	V _{IN} = 2.1 V			10	μA
V _{SEL(hyst)}	Input hysteresis voltage		0.2			V
V _{SELCL}	Input clamp voltage	I _{IN} = 1 mA	6		8.5	V
		I _{IN} = -1 mA		-0.7		
SEn characteristics (7 V < V _{CC} < 18 V)						
V _{SEnL}	Input low level voltage				0.9	V
I _{SEnL}	Low level input current	V _{IN} = 0.9 V	1			μA
V _{SEnH}	Input high level voltage		2.1			V
I _{SEnH}	High level input current	V _{IN} = 2.1 V			10	μA
V _{SEn(hyst)}	Input hysteresis voltage		0.2			V
V _{SEnCL}	Input clamp voltage	I _{SEN} = 1 mA	9		12	V
		I _{SEN} = -1 mA		-0.7		

Table 8. Protections

7 V < V _{CC} < 18 V; -40 °C < T _j < 150 °C						
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I _{LIMH} ⁽¹⁾	DC short- circuit current	V _{CC} = 16 V; T _j = -40 °C	-15%	14	15%	A
		V _{CC} = 16 V; T _j = 150 °C	-15%	10	15%	
I _{LIMH2} ⁽²⁾		V _{CC} = 19 V; T _j = -40 °C	-15%	11.2	15%	
		V _{CC} = 19 V; T _j = 150 °C	-15%	8.9	15%	
I _{LIMH} at 22 V		V _{CC} = 22 V; T _j = 25 °C		4.2		
T _{TSD}		Shutdown temperature		150	175	
T _{RS}	Thermal reset of fault diagnostic indication	V _{FR} = 0 V; V _{SEn} = 5 V	135			
T _{HYST}	Thermal hysteresis (T _{TSD} - T _{RS}) ⁽³⁾			7		
ΔT _{J_SD}	Dynamic temperature	V _{CC} = 19 V		55		K
		V _{CC} = 16 V		80		
t _{LATCH_RST}	Fault reset time for output unlatch ⁽³⁾	V _{FR} = 5 V to 0 V; V _{SEn} = 5 V; For example Ch ₀ : V _{IN0} = 5 V; V _{SEL0,1} = 0 V	3	10	20	μs
t _{D_Restart}	Latch-OFF delay time before automatic restart	T _j > 125 °C		50	75	ms
V _{DEMAG}	Turn-off output voltage clamp	I _{OUT} = 0.7 A; L = 6 mH; T _j = -40 °C	V _{CC} - 36			V
		I _{OUT} = 0.7 A; L = 6 mH; T _j = 25 °C to 150 °C	V _{CC} - 36	V _{CC} - 38	V _{CC} - 45	V

1. I_{LIMH} guaranteed between 7 V and 16 V, -40 °C < T_j < 150 °C.
2. I_{LIMH2} guaranteed between 16 V and 19 V, -40 °C < T_j < 150 °C.
3. Specified by design and evaluated by characterization, not tested in production.

Table 9. Current Sense

7 V < V _{CC} < 18 V; -40 °C < T _j < 150 °C						
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{SENSE_CL}	CurrentSense clamp voltage	V _{SEn} = 0 V; I _{SENSE} = 1 mA	-9	-8	-7	V
		V _{SEn} = 0 V; I _{SENSE} = -1 mA		7		
CurrentSense characteristics						
K _{OL}	I _{OUT} /I _{SENSE}		810			
dK _{OL} /K _{OL} ⁽¹⁾⁽²⁾	CurrentSense ratio drift at calibration point	I _{OUT} = 0.01 A; V _{SENSE} = 0.5 V; V _{SEn} = 5 V	-25		25	%
K ₀	I _{OUT} /I _{SENSE}		-35%	1500	+35%	
dK ₀ /K ₀ ⁽¹⁾⁽²⁾	CurrentSense ratio drift	I _{OUT} = 0.025 A; V _{SENSE} = 0.5 V; V _{SEn} = 5 V	-25		25	%
K ₁	I _{OUT} /I _{SENSE}		-15%	1500	15%	
dK ₁ /K ₁ ⁽¹⁾⁽²⁾	CurrentSense ratio drift	I _{OUT} = 0.15 A; V _{SENSE} = 0.5 V; V _{SEn} = 5 V	-15		15	%
K ₂	I _{OUT} /I _{SENSE}		-7%	1500	7%	
dK ₂ /K ₂ ⁽¹⁾⁽²⁾	CurrentSense ratio drift	I _{OUT} = 0.7 A; V _{SENSE} = 3.5 V; V _{SEn} = 5 V	-7		7	%
K ₈₅₀	I _{OUT} /I _{SENSE}		-7%	1500	7%	
dK ₈₅₀ /K ₈₅₀ ⁽¹⁾⁽²⁾	CurrentSense ratio drift	I _{OUT} = 0.85 A; V _{SENSE} = 3.5 V; V _{SEn} = 5 V	-7		7	%
K ₃	I _{OUT} /I _{SENSE}		-5%	1500	5%	
dK ₃ /K ₃ ⁽¹⁾⁽²⁾	CurrentSense ratio drift	I _{OUT} = 2.1 A; V _{SENSE} = 3.5 V; V _{SEn} = 5 V	-5		5	%
I _{SENSE0}	CurrentSense leakage current	CS disabled: V _{SEn} = 0 V	0		0.5	μA
		CS disabled: -1 V < V _{SENSE} < 5 V ⁽¹⁾	-0.5		0.5	
		CS enabled: V _{SEn} = 5 V; all channel ON; I _{OUTX} = 0 A; Ch _X diagnostic selected; For example Ch ₀ : V _{IN0} = 5 V; V _{IN1,2,3} = 5 V; V _{SEL0,1} = 0 V; I _{OUT0} = 0 A; I _{OUT1,2,3} = 0.7 A	0		10	
		CS enabled: V _{SEn} = 5 V; Ch _X OFF; I _{OUTX} = 0 A; Ch _X diagnostic selected; For example Ch ₀ : V _{IN0} = 0 V; V _{IN1,2,3} = 5 V; V _{SEL0,1} = 0 V; I _{OUT0} = 0 A; I _{OUT1,2,3} = 0.7 A	0		1	
V _{OUT_MSD} ⁽¹⁾	Output voltage for CurrentSense shutdown	V _{SEn} = 5 V; R _{SENSE} = 2.7 kΩ; For example Ch ₀ : V _{IN0} = 5 V; V _{SEL0,1} = 0 V; I _{OUT0} = 0.7 A		5		V
V _{SENSE_SAT}	CurrentSense saturation voltage	V _{CC} = 7 V; R _{SENSE} = 10 kΩ; V _{SEn} = 5 V; V _{IN0} = 5 V; V _{SEL0,1} = 0 V; I _{OUT0} = 6 A; T _j = -40 °C	4.8			V
I _{SENSE_SAT} ⁽¹⁾	CS saturation current	V _{CC} = 7 V; V _{SENSE} = 3.5 V; V _{IN0} = 5 V; V _{SEn} = 5 V; V _{SEL0,1} = 0 V; T _j = 150 °C	2			mA

7 V < V _{CC} < 18 V; -40 °C < T _j < 150 °C						
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I _{OUT_SAT} ⁽¹⁾	Output saturation current	V _{CC} = 7 V; V _{SENSE} = 3.5 V; V _{IN0} = 5 V; V _{SEn} = 5 V; V _{SEL0,1} = 0 V; T _j = 150 °C	4			A
OFF-state diagnostic						
V _{OL}	OFF-state open-load voltage detection threshold	V _{SEn} = 5 V; Ch _X OFF; Ch _X diagnostic selected; For example Ch ₀ : V _{IN0} = 0 V; V _{SEL0,1} = 0 V;	2	3	4	V
I _{L(off2)}	OFF-state output sink current	V _{IN} = 0 V; V _{OUT} = V _{OL} ; T _j = -40 °C to 125 °C	-150	-40	-5	μA
t _{DSTKON}	OFF-state diagnostic delay time from falling edge of INPUT (see Figure 6. t _{DSTKON})	V _{SEn} = 5 V; Ch _X ON to OFF transition; Ch _X diagnostic selected; For example Ch ₀ : V _{IN0} = 5 V to 0 V; V _{SEL0,1} = 0 V; I _{OUT0} = 0 A; V _{OUT} = 4 V	100	170	250	μs
t _{D_OL_V}	Settling time for valid OFF-state open load diagnostic indication from rising edge of SEn	V _{IN0,1,2,3} = 0 V; V _{FR} = 0 V; V _{OUT0} = 4 V; V _{SEn} = 0 V to 5 V			60	μs
t _{D_VOL}	OFF-state diagnostic delay time from rising edge of V _{OUT}	V _{SEn} = 5 V; Ch _X OFF; Ch _X diagnostic selected; For example Ch ₀ : V _{IN0} = 0 V; V _{SEL0,1} = 0 V; V _{OUT0} = 0 V to 4 V		5	30	μs
Fault diagnostic feedback (see Table 10. Truth table)						
V _{SENSEH}	CurrentSense output voltage in fault condition	13 V < V _{CC} < 18 V; • For example: Ch ₀ in open load; R _{SENSE} = 0.7 kΩ; V _{IN0} = 0 V; V _{SEn} = 5 V; V _{SEL0,1} = 0 V; I _{OUT0} = 0 A; V _{OUT0} = 4 V	5		7.5	V
		V _{CC} = 7 V; • For example: Ch ₀ in open load; R _{SENSE} = 0.7 kΩ; V _{IN0} = 0 V; V _{SEn} = 5 V; V _{SEL0,1} = 0 V; I _{OUT0} = 0 A; V _{OUT0} = 4 V	4.3			
I _{SENSEH}	CurrentSense output current in fault condition	13 V < V _{CC} < 18 V; V _{SENSE} = 5 V • For example: Ch ₀ in open load; V _{IN0} = 0 V; V _{SEn} = 5 V; V _{SEL0,1} = 0 V; I _{OUT0} = 0 A; V _{OUT0} = 4 V	7	8.6	12	mA

7 V < V _{CC} < 18 V; -40 °C < T _j < 150 °C						
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I _{SENSEH}	CurrentSense output current in fault condition	V _{CC} = 7 V; V _{SENSE} = 5 V; • For example: Ch ₀ in open load; V _{IN0} = 0 V; V _{SEn} = 5 V; V _{SEL0,1} = 0 V; I _{OUT0} = 0 A; V _{OUT0} = 4 V	4.4			mA
CurrentSense timings (current sense mode - see Figure 5. Current Sense timings (current sense mode)) ⁽³⁾						
t _{DSENSE1H}	Current sense settling time from rising edge of SE _n	V _{IN} = 5 V; V _{SEn} = 0 V to 5 V; R _{SENSE} = 1 kΩ; R _L = 18.6 Ω			60	μs
t _{DSENSE1L}	Current sense disable delay time from falling edge of SE _n			5	20	μs
t _{DSENSE2H}	Current sense settling time from rising edge of INPUT	V _{IN} = 0 V to 5 V; V _{SEn} = 5 V; R _{SENSE} = 1 kΩ; R _L = 18.6 Ω		100	200	μs
Δt _{DSENSE2H}	Current sense settling time from rising edge of I _{OUT} (dynamic response to a step change of I _{OUT})	V _{IN} = 5 V; V _{SEn} = 5 V; R _{SENSE} = 1 kΩ; I _{SENSE} = 90 % of I _{SENSEMAX} ; R _L = 18.6 Ω			100	μs
t _{DSENSE2L}	Current sense turn-off delay time from falling edge of INPUT	V _{IN} = 5 V to 0 V; V _{SEn} = 5 V; R _{SENSE} = 1 kΩ; R _L = 18.6 Ω		70	250	μs
t _{DSENSE3H}	Current sense latch-OFF filtering time		1.4	2	2.6	ms
CurrentSense timings (Multiplexer transition times) ⁽³⁾						
t _{D_XtoY}	CurrentSense transition delay from Ch _X to Ch _Y	V _{IN0} = 5 V; V _{IN1} = 5 V; V _{SEn} = 5 V; V _{SEL0} = 0 V to 5 V; I _{OUT0} = 0 A; I _{OUT1} = 0.7 A; R _{SENSE} = 1 kΩ			30	μs
t _{D_CStoVSENSEH}	CurrentSense transition delay from stable current sense on Ch _X to V _{SENSEH} on Ch _Y	V _{IN0} = 5 V; V _{IN1} = 0 V; V _{SEn} = 5 V; V _{SEL0} = 0 V to 5 V; I _{OUT0} = 0.7 A; V _{OUT1} = 4 V; R _{SENSE} = 1 kΩ			20	

1. Parameter specified by design; not subject to production test.
2. All values refer to V_{CC} = 13 V; T_j = 25 °C, unless otherwise specified.
3. Transition delay is measured up to ±10% of final conditions.

Figure 4. Switching time and pulse skew

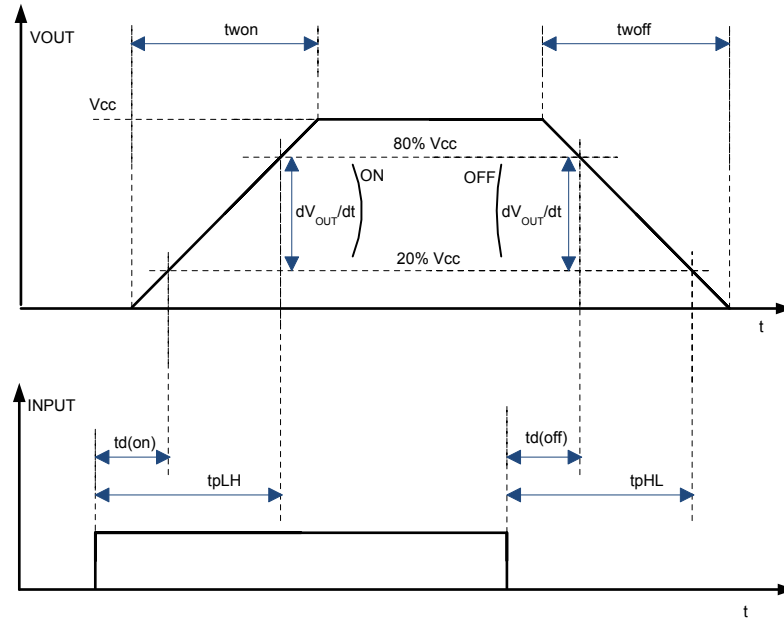
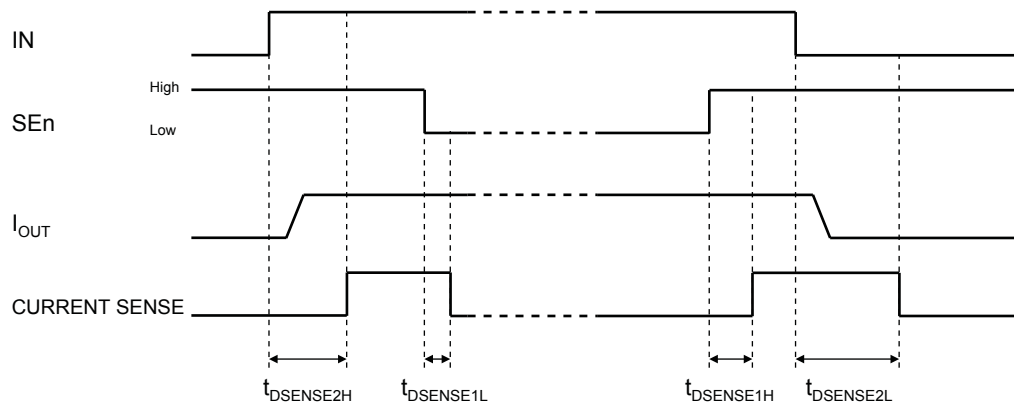
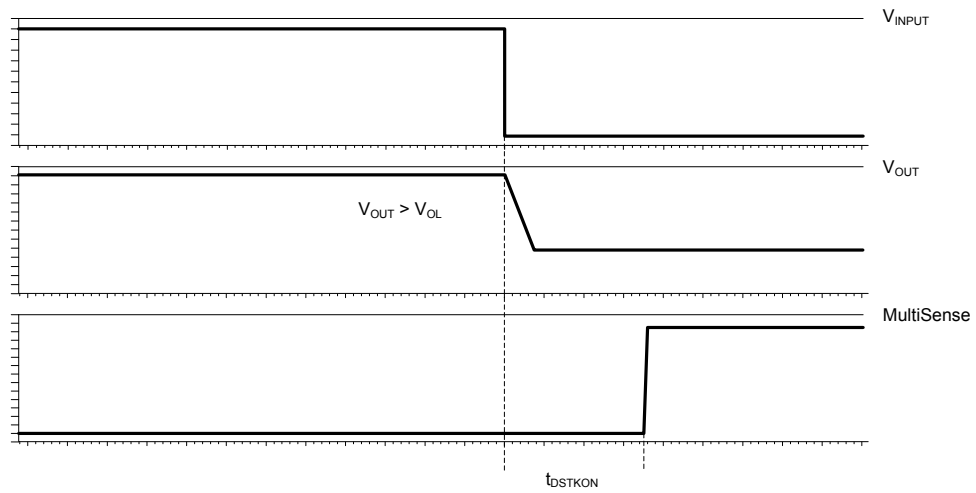


Figure 5. Current Sense timings (current sense mode)



GAPG1003141014CFT

Figure 6. t_{DSTKON}


GAPG2609141140CFT

Table 10. Truth table

Mode	Conditions	IN _x	FR	SEn	SEL _x	OUT _x	CS	Comments
Standby	All logic inputs low	L	L	L	L	L	Hi-Z	Low quiescent current consumption
Normal	Nominal load connected; $T_j < 150\text{ °C}$	L	X	See ⁽¹⁾		L	See ⁽¹⁾	Outputs configured for auto-restart
		H	L			H		Outputs configured for Latch-off
		H	H			H		
Overload	Overload or short to GND causing: $T_j > T_{TSD}$ or $\Delta T_j > \Delta T_{j_SD}$	L	X	See ⁽¹⁾		L	See ⁽¹⁾	Output cycles with temperature hysteresis
		H	L			H		Output latches-off
		H	H			L		
Undervoltage	$V_{CC} < V_{USD}$ (falling)	X	X	X	X	L	Hi-Z	Re-start when $V_{CC} > V_{USD} +$
						L	Hi-Z	$V_{USDhyst}$ (rising)
OFF-state diagnostics	Short to V_{CC}	L	X	See ⁽¹⁾		H	See ⁽¹⁾	
	Open-load	L	X			H		External pull-up
Negative output voltage	Inductive loads turn-off	L	X	See ⁽¹⁾		< 0 V	See ⁽¹⁾	

1. Refer to Table 11. Current sense multiplexer addressing.

Table 11. Current sense multiplexer addressing

SEn	SEL ₁	SEL ₀	MUX channel	CS output			
				Normal mode	Overload	OFF-state diag.	Negative output
L	X	X		Hi-Z			
H	L	L	Channel 0 diagnostic	$I_{SENSE} = 1/K * I_{OUT0}$	$V_{SENSE} = V_{SENSEH}$	$V_{SENSE} = V_{SENSEH}$	Hi-Z
H	L	H	Channel 1 diagnostic	$I_{SENSE} = 1/K * I_{OUT1}$			
H	H	L	Channel 2 diagnostic	$I_{SENSE} = 1/K * I_{OUT2}$			
H	H	H	Channel 3 diagnostic	$I_{SENSE} = 1/K * I_{OUT3}$			

2.4 Waveforms

Figure 7. Latch-off mode - Intermittent short circuit

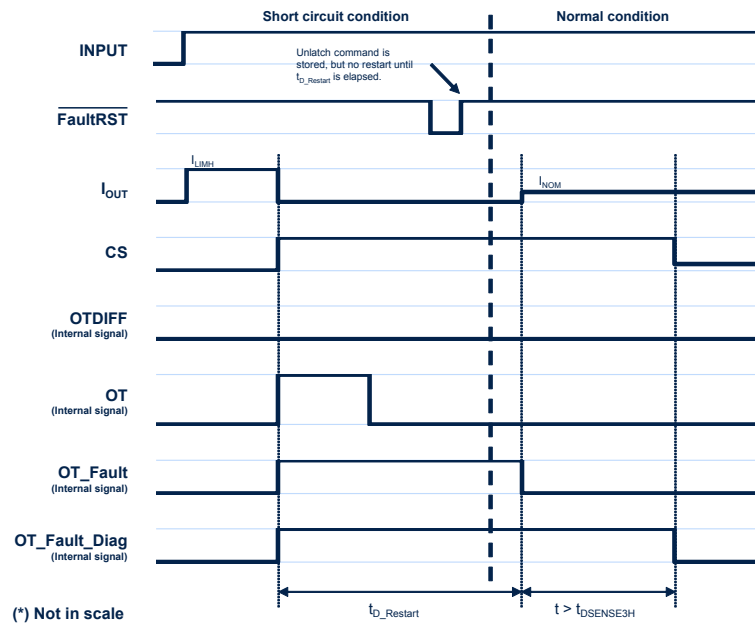


Figure 8. Auto-restart mode - Intermittent short circuit

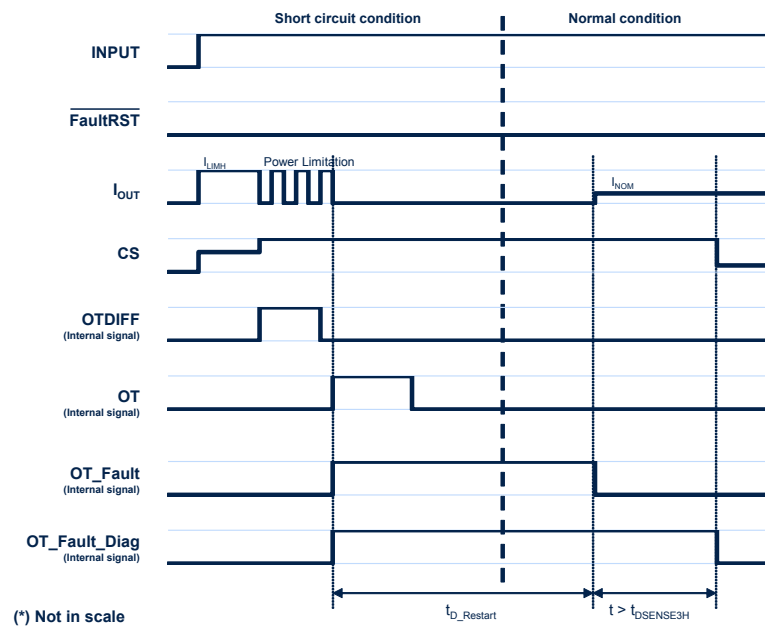


Figure 9. Auto-restart mode - Permanent short circuit

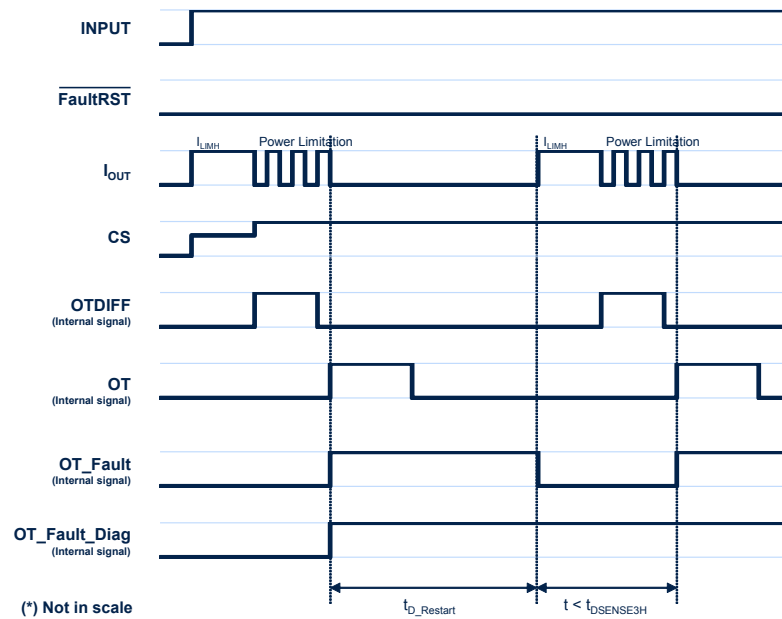


Figure 10. Standby mode activation

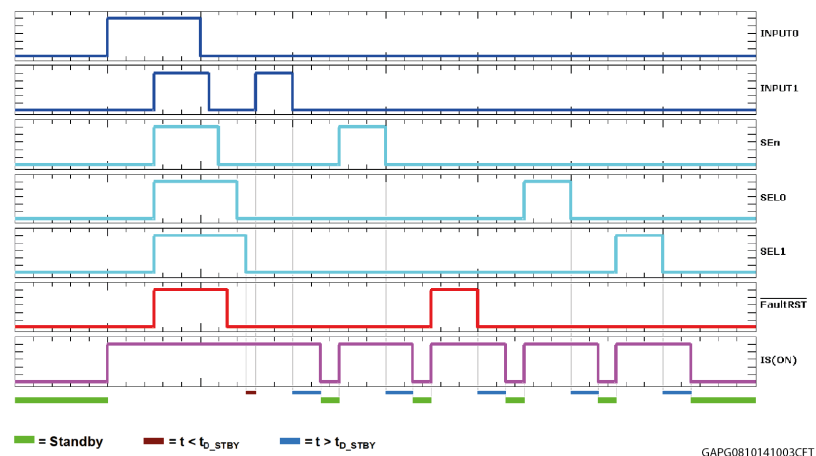
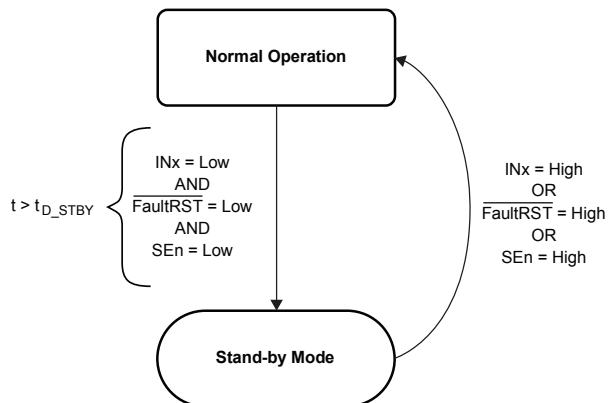


Figure 11. Standby state diagram



GADG2702181047RI

2.5 Electrical characteristics (curves)

Figure 12. OFF-state output current

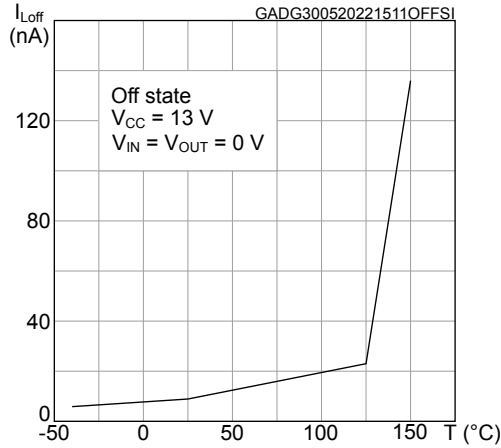


Figure 13. Standby current

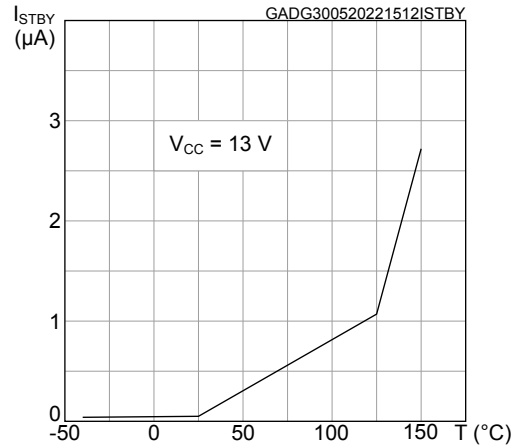


Figure 14. $I_{GND(ON)}$ vs I_{out}

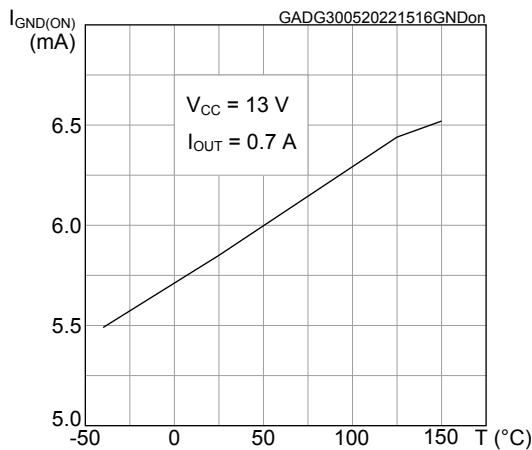


Figure 15. Logic input high level voltage

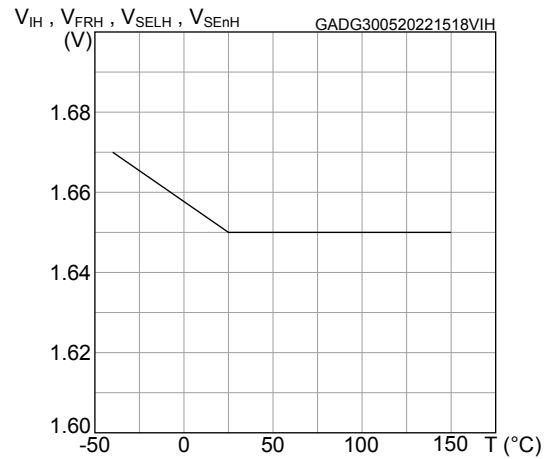


Figure 16. Logic input low level voltage

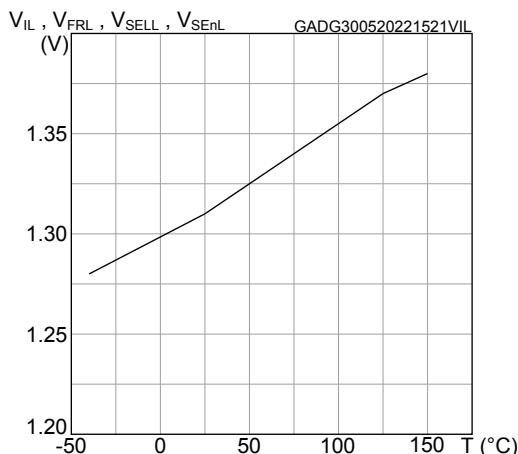


Figure 17. High level logic input current

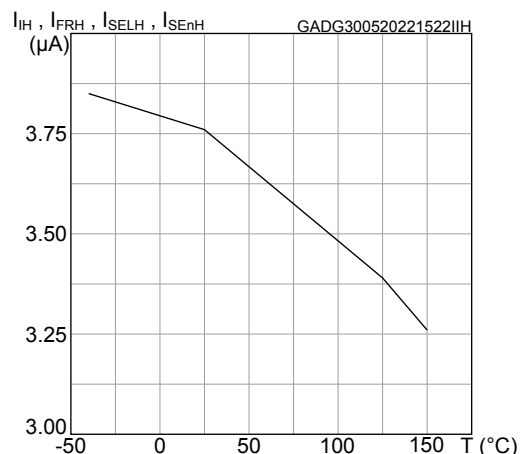


Figure 18. Low level logic input current

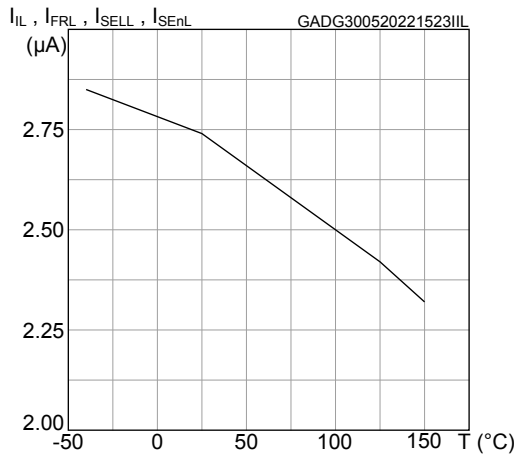


Figure 19. Logic input hysteresis voltage

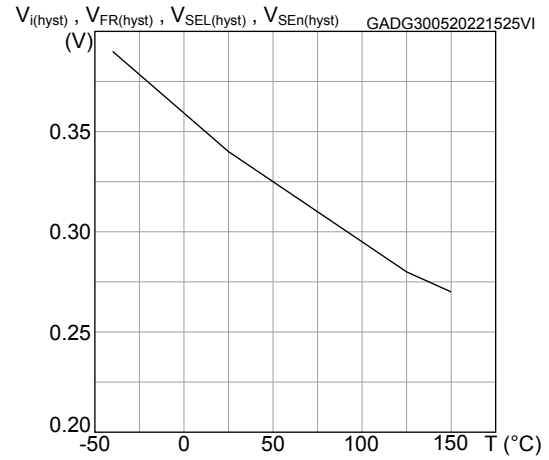


Figure 20. FaultRST input clamp voltage

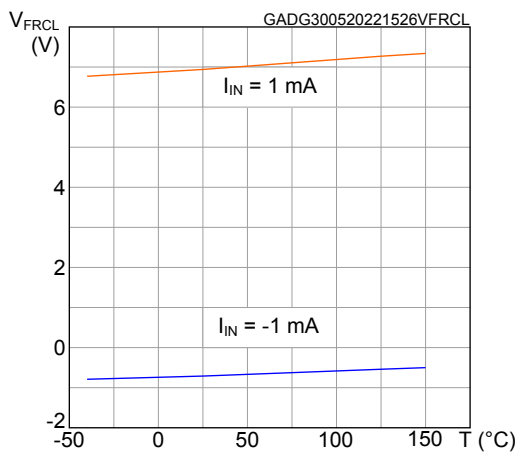


Figure 21. Undervoltage shutdown

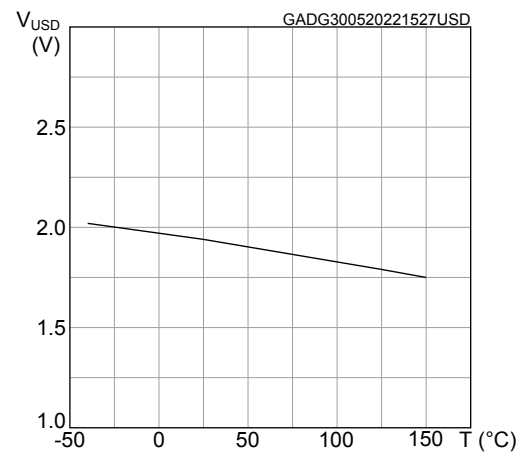


Figure 22. On-state resistance vs T_C

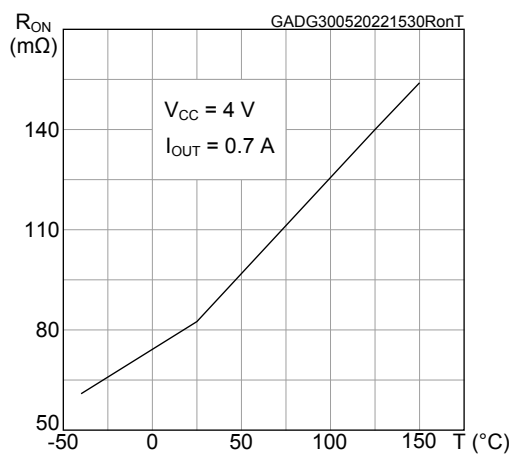


Figure 23. On-state resistance vs V_{CC}

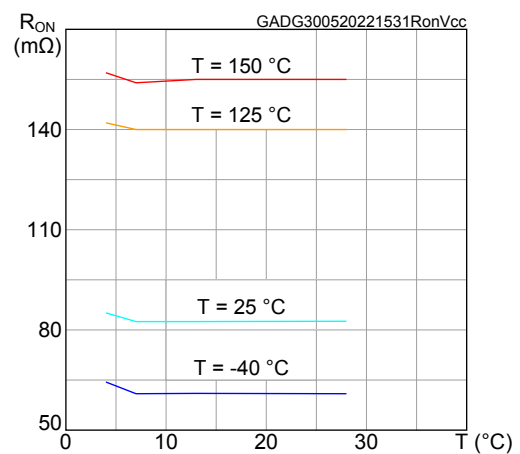


Figure 24. Turn-on voltage slope

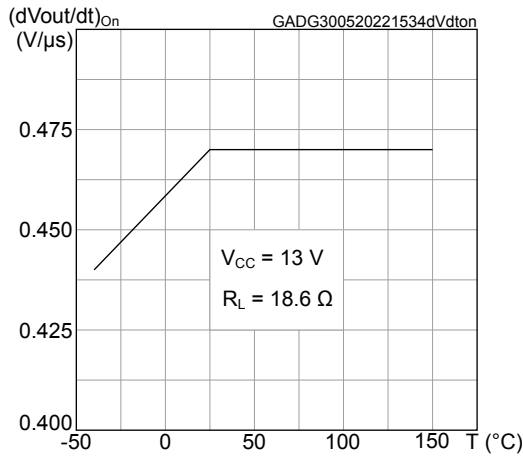


Figure 25. Turn-off voltage slope

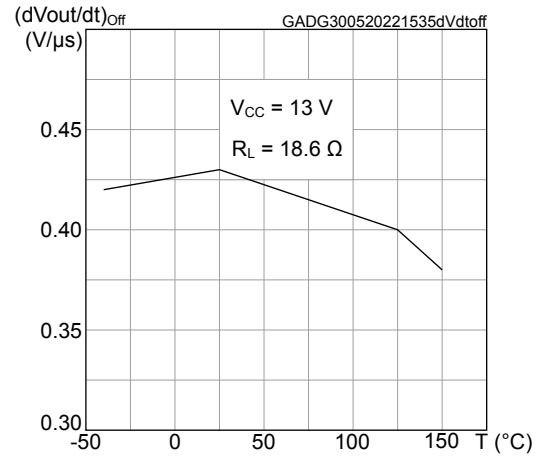


Figure 26. W_{ON} vs T_C

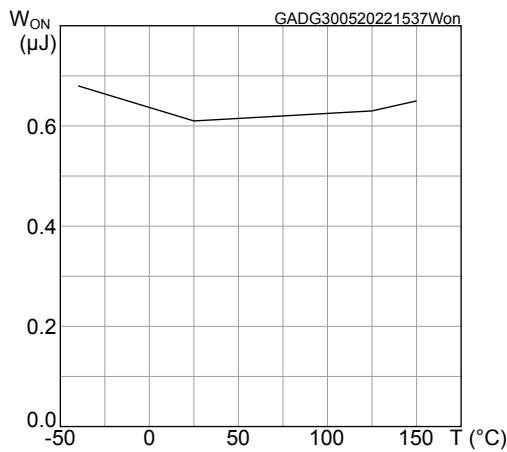


Figure 27. W_{OFF} vs T_C

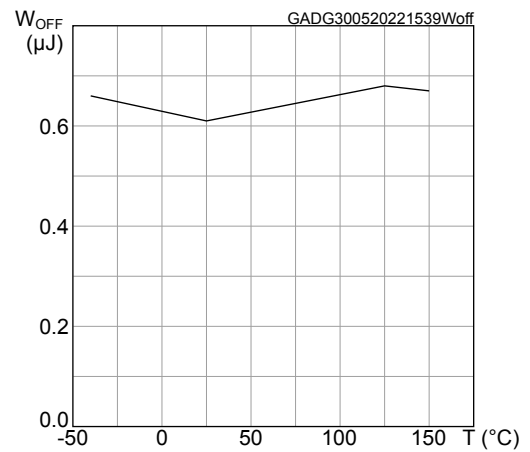


Figure 28. I_{LIMH} vs T_C

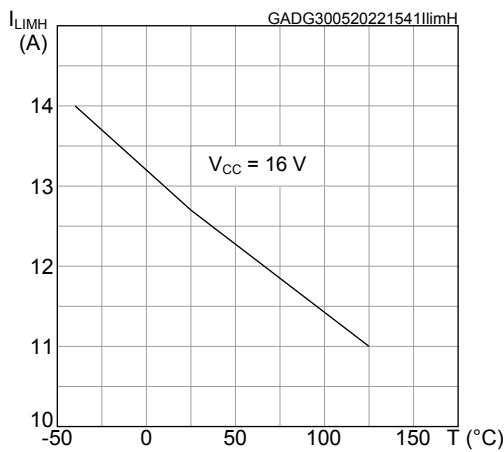


Figure 29. OFF-state open-load voltage detection threshold

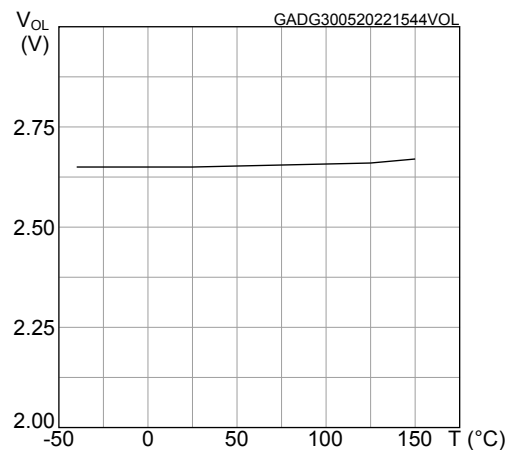


Figure 30. V_{SENSE_CL} vs T_C

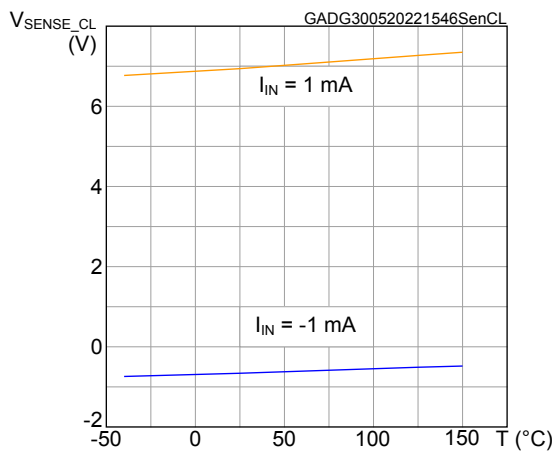
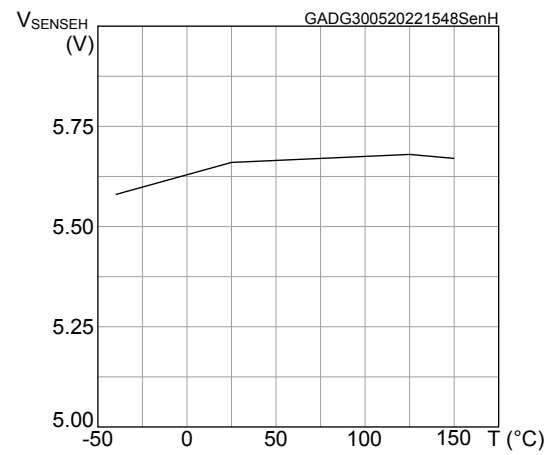


Figure 31. V_{SENSEH} vs T_C



3 Protections

3.1 Power limitation

The basic working principle of this protection consists of an indirect measurement of the junction temperature swing ΔT_J through the direct measurement of the spatial temperature gradient on the device surface in order to automatically shut off the output MOSFET as soon as ΔT_J exceeds the safety level of ΔT_{J_SD} . According to the voltage level on the $\overline{\text{FaultRST}}$ pin, the output MOSFET switches on and cycles with a thermal hysteresis according to the maximum instantaneous power which can be handled ($\overline{\text{FaultRST}} = \text{Low}$) or remains off ($\overline{\text{FaultRST}} = \text{High}$). The protection prevents fast thermal transient effects and, consequently, reduces thermo-mechanical fatigue.

3.2 Thermal shutdown

In case the junction temperature of the device exceeds the maximum allowed threshold (typically 175°C), it automatically switches off and the diagnostic indication is triggered. According to the voltage level on the $\overline{\text{FaultRST}}$ pin, the device switches on again as soon as its junction temperature drops to T_R ($\overline{\text{FaultRST}} = \text{Low}$) or remains off ($\overline{\text{FaultRST}} = \text{High}$).

3.3 Current limitation

The device is equipped with an output current limiter in order to protect the silicon as well as the other components of the system (e.g. bonding wires, wiring harness, connectors, loads, etc.) from excessive current flow. Consequently, in case of short circuit, overload or during load power-up, the output current is clamped to a safety level, I_{LIMH} , by operating the output power MOSFET in the active region.

3.4 Negative voltage clamp

In case the device drives inductive load, the output voltage reaches a negative value during turn off. A negative voltage clamp structure limits the maximum negative voltage to a certain value, V_{DEMAG} , allowing the inductor energy to be dissipated without damaging the device.

4.1.1 Diode (DGND) in the ground line

A resistor (typ. $R_{GND} = 4.7 \text{ k}\Omega$) should be inserted in parallel to D_{GND} if the device drives an inductive load.

This small signal diode can be safely shared amongst several different HSDs. Also in this case, the presence of the ground network produces a shift ($\approx 600 \text{ mV}$) in the input threshold and in the status output values if the microprocessor ground is not common to the device ground. This shift does not vary if more than one HSD shares the same diode/resistor network.

4.2 Immunity against transient electrical disturbances

The immunity of the device against transient electrical emissions, conducted along the supply lines and injected into the V_{CC} pin, is tested in accordance with ISO7637-2:2011 (E) and ISO 16750-2:2010.

The related function performance status classification is shown in [Table 12. ISO 7637-2 - electrical transient conduction along supply line.](#)

Test pulses are applied directly to DUT (device under test) both in ON and OFF-state and in accordance to ISO 7637-2:2011(E), chapter 4.

The DUT is intended as the current device only, with external components as shown in [Figure 34. M0-9 application schematic.](#)

Status II is defined in ISO 7637-1 Function Performance Status Classification (FPSC) as follows: "The function does not perform as designed during the test but returns automatically to normal operation after the test".

Table 12. ISO 7637-2 - electrical transient conduction along supply line

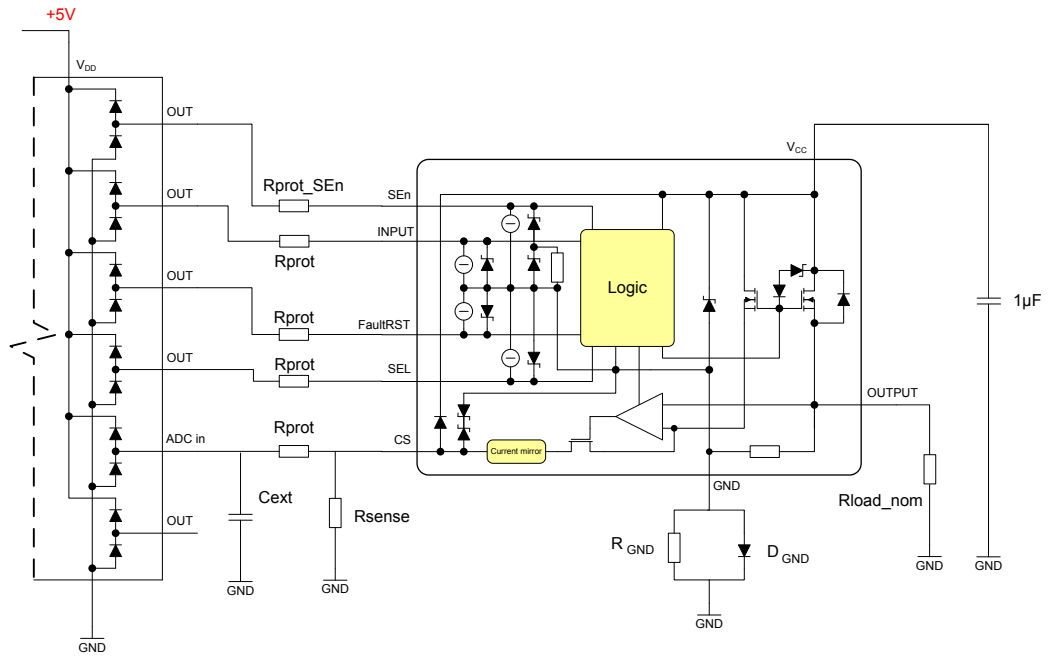
Test Pulse 2011(E)	Test pulse severity level with Status II functional performance status		Minimum number of pulses or test time	Burst cycle / pulse repetition time		Pulse duration and pulse generator internal impedance
	Level	$U_S^{(1)}$		min	max	
1	III	-112 V	500 pulses	0.5 s		2 ms, 10 Ω
2a	III	+55 V	500 pulses	0.2 s	5 s	50 μs , 2 Ω
3a	IV	-220 V	1h	90 ms	100 ms	0.1 μs , 50 Ω
3b	IV	+150 V	1h	90 ms	100 ms	0.1 μs , 50 Ω
4 ⁽²⁾	IV	-7 V	1 pulse			100 ms, 0.01 Ω
Load dump according to ISO 16750-2:2010						
Test B ⁽³⁾		35 V	5 pulse	1 min		400 ms, 2 Ω

1. U_S is the peak amplitude as defined for each test pulse in ISO 7637-2:2011(E), chapter 5.6.

2. Test pulse from ISO 7637-2:2004(E).

3. With 35 V external suppressor referred to ground ($-40^\circ\text{C} < T_j < 150^\circ\text{C}$).

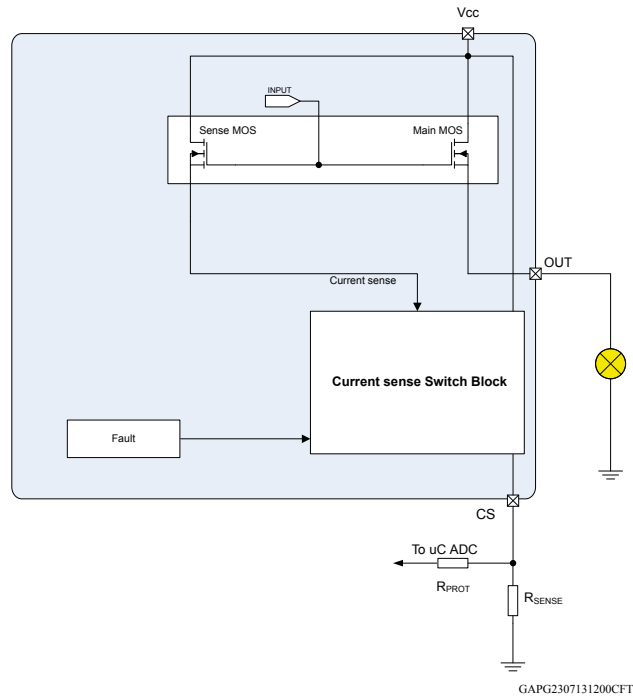
Figure 34. M0-9 application schematic



Note: In case of multiple channels, each OUTPUT must be connected to the resistive nominal load.

4.4.1 Principle of Current Sense signal generation

Figure 36. Current Sense block diagram



Current sense

The output is capable of providing:

- Current mirror proportional to the load current in normal operation, delivering current proportional to the load according to a known ratio named **K**
- Diagnostics flag in fault conditions delivering fixed voltage V_{SENSEH}

The current delivered by the current sense circuit, I_{SENSE} , can be easily converted into a voltage V_{SENSE} by using an external sense resistor, R_{SENSE} , allowing continuous load monitoring and abnormal condition detection.

Normal operation (channel ON, no fault, SEn active)

While the device is operating in normal conditions (no fault intervention), V_{SENSE} calculation can be done using simple equations

Current provided by CS output: $I_{SENSE} = I_{OUT}/K$

Voltage on R_{SENSE} : $V_{SENSE} = R_{SENSE} \cdot I_{SENSE} = R_{SENSE} \cdot I_{OUT}/K$

Where:

- V_{SENSE} is the voltage measurable on R_{SENSE} resistor
- I_{SENSE} is the current provided from CS pin in current output mode
- I_{OUT} is the current flowing through output
- K factor represents the ratio between PowerMOS cells and SenseMOS cells; its spread includes geometric factor spread, current sense amplifier offset and process parameters spread of the overall circuitry, specifying the ratio between I_{OUT} and I_{SENSE} .

Failure flag indication

In case of power limitation/overtemperature, the fault is indicated by the CS pin which is switched to a "current limited" voltage source, V_{SENSEH} .

In any case, the current sourced by the CS in this condition is limited to I_{SENSEH} .

Figure 37. Analog HSD – open-load detection in off-state

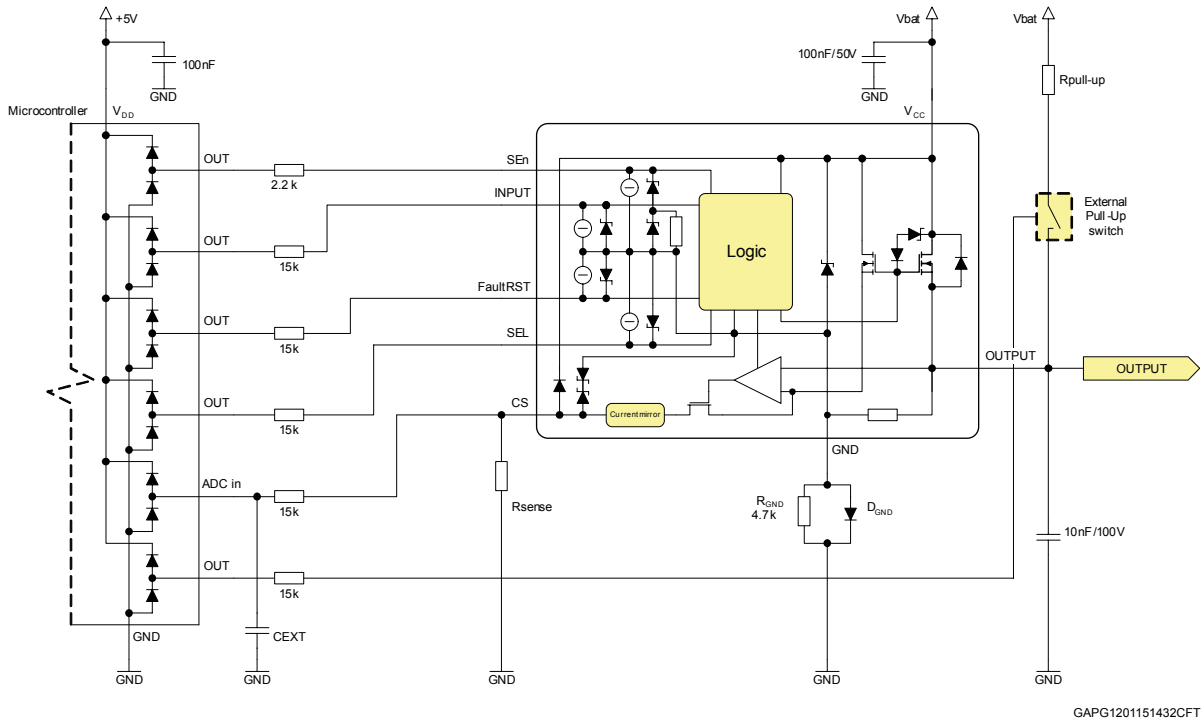


Figure 38. Open-load / short to V_{CC} condition

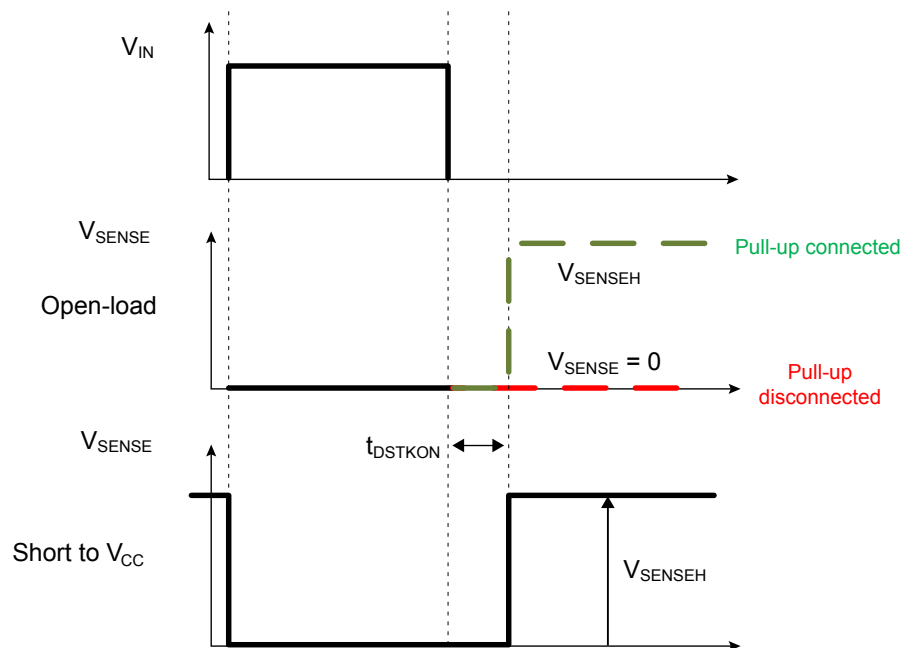


Table 13. Current Sense pin levels in off-state

Condition	Output	CS	SEn
Open-load	$V_{OUT} > V_{OL}$	Hi-Z	L
		V_{SENSEH}	H
	$V_{OUT} < V_{OL}$	Hi-Z	L
		0	H
Short to V_{CC}	$V_{OUT} > V_{OL}$	Hi-Z	L
		V_{SENSEH}	H
Nominal	$V_{OUT} < V_{OL}$	Hi-Z	L
		0	H

4.4.2 Short to V_{CC} and OFF-state open-load detection

Short to V_{CC}

A short circuit between V_{CC} and output is indicated by the relevant current sense pin set to V_{SENSEH} during the device off-state. Small or no current is delivered by the current sense during the on-state depending on the nature of the short-circuit.

OFF-state open-load with external circuitry

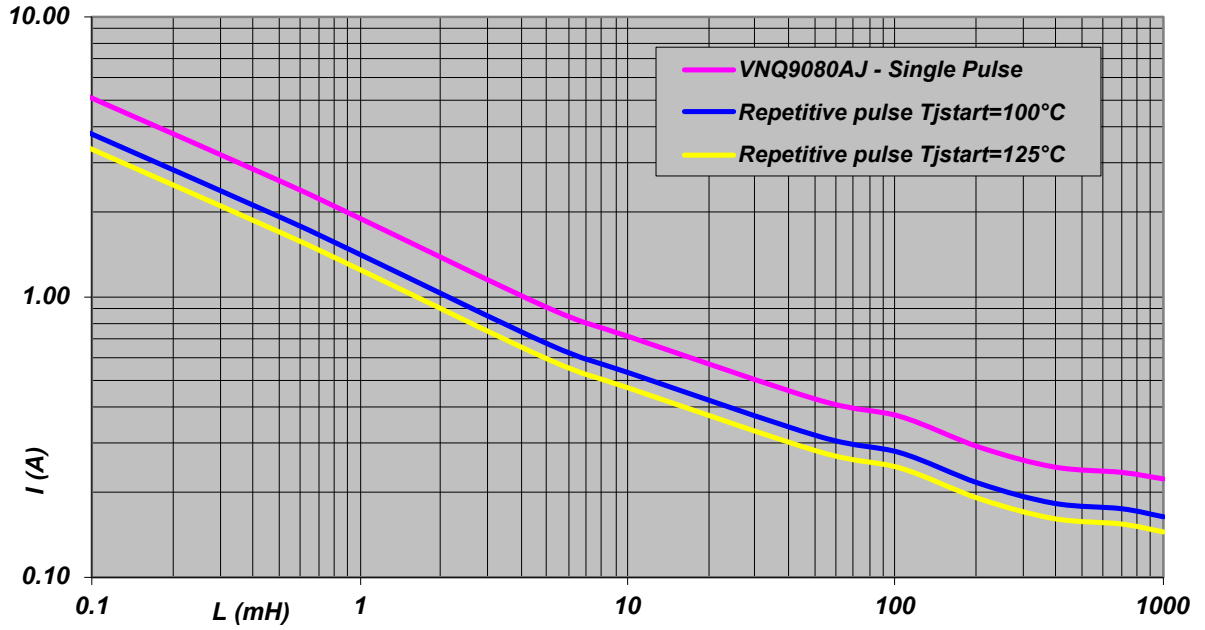
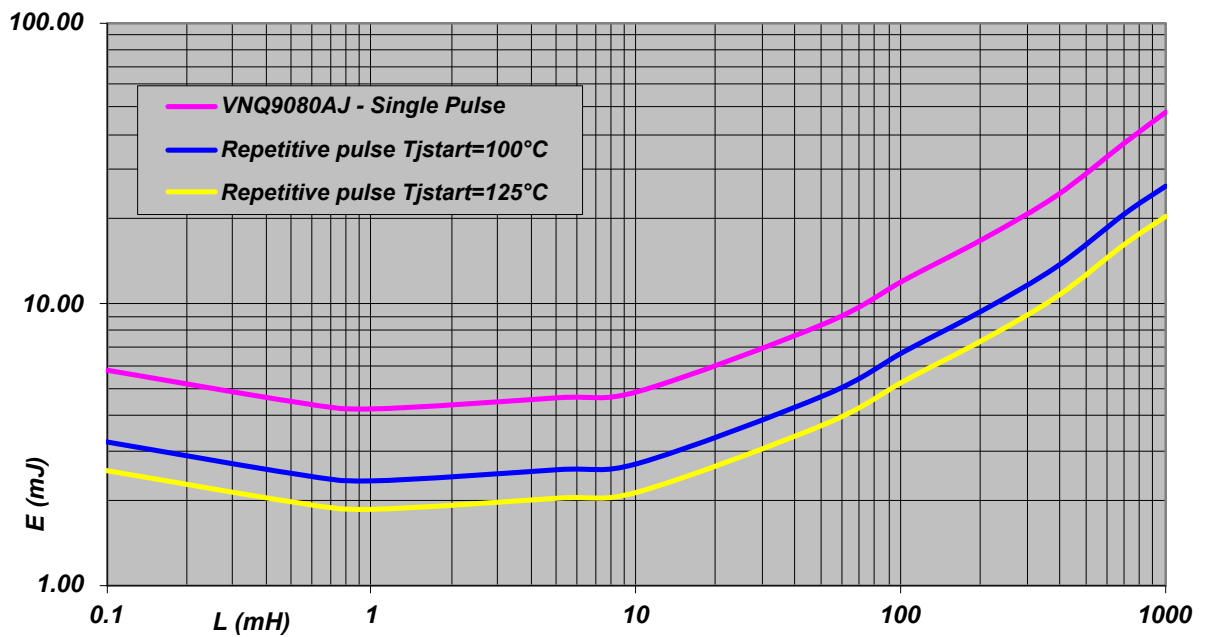
Detection of an open-load in off mode requires an external pull-up resistor R_{PU} connecting the output to a positive supply voltage V_{PU} .

It is preferable that V_{PU} is switched off during the module standby mode in order to avoid the overall standby current consumption to increase in normal conditions, that is when load is connected.

R_{PU} must be selected in order to ensure $V_{OUT} > V_{OLmax}$ in accordance with the following equation:

$$R_{PU} < \frac{V_{PU} - 4}{I_{L(off2)min @ 4V}}$$

5 Maximum demagnetization energy ($V_{cc} = 16\text{ V}$)

Figure 39. Maximum turn off current versus inductance

Figure 40. Maximum turn off energy versus inductance


Note: Values are generated with $R_L = 0\ \Omega$.

In case of repetitive pulses, T_{jstart} (at the beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves A and B.

6 Package and PCB thermal data

6.1 PowerSSO-16 thermal data

Figure 41. PowerSSO-16 on two-layer PCB (2s0p to JEDEC JESD 51-5)

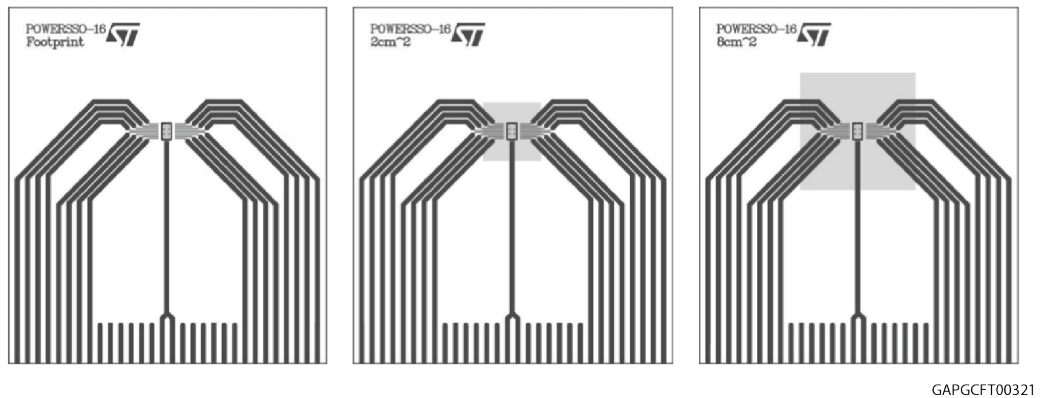


Figure 42. PowerSSO-16 on four-layer PCB (2s2p to JEDEC JESD 51-7)

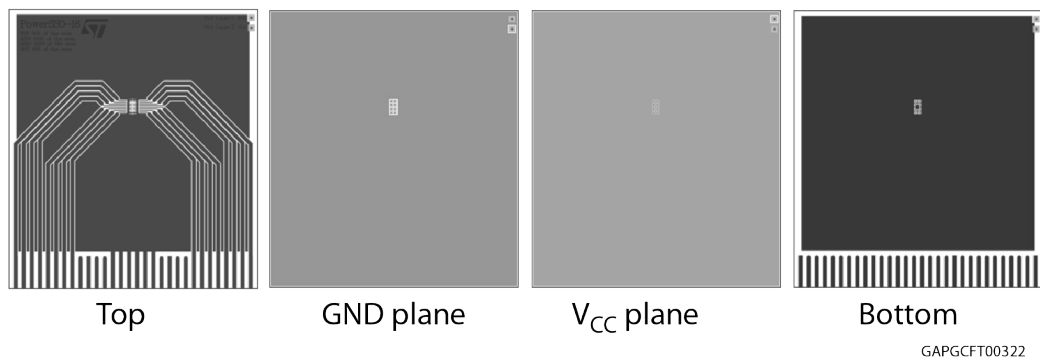


Table 14. PCB properties

Dimension	Value
Board finish thickness	1.6 mm \pm 10%
Board dimension	77 mm x 86 mm
Board Material	FR4
Copper thickness (top and bottom layers)	0.070 mm
Copper thickness (inner layers)	0.035 mm
Thermal vias separation	1.2 mm
Thermal via diameter	0.3 mm \pm 0.08 mm
Copper thickness on vias	0.025 mm
Footprint dimension (top layer)	2.2 mm x 3.9 mm
Heatsink copper area dimension (bottom layer)	Footprint, 2 cm ² or 8 cm ²

Figure 43. $R_{thj-amb}$ vs PCB copper area in open box free air condition (one channel on)

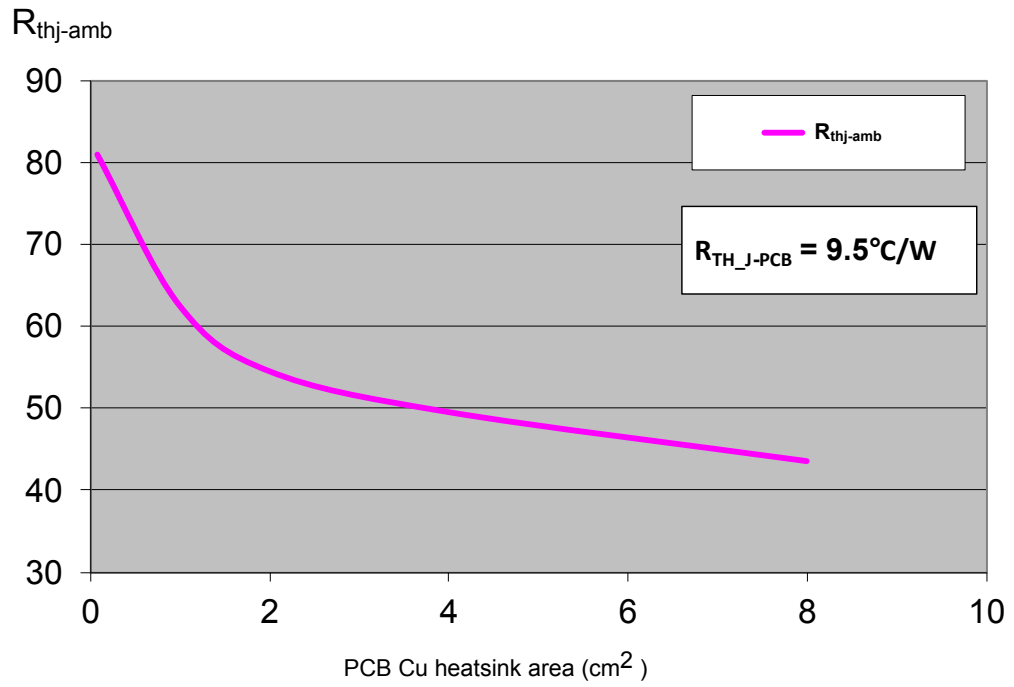
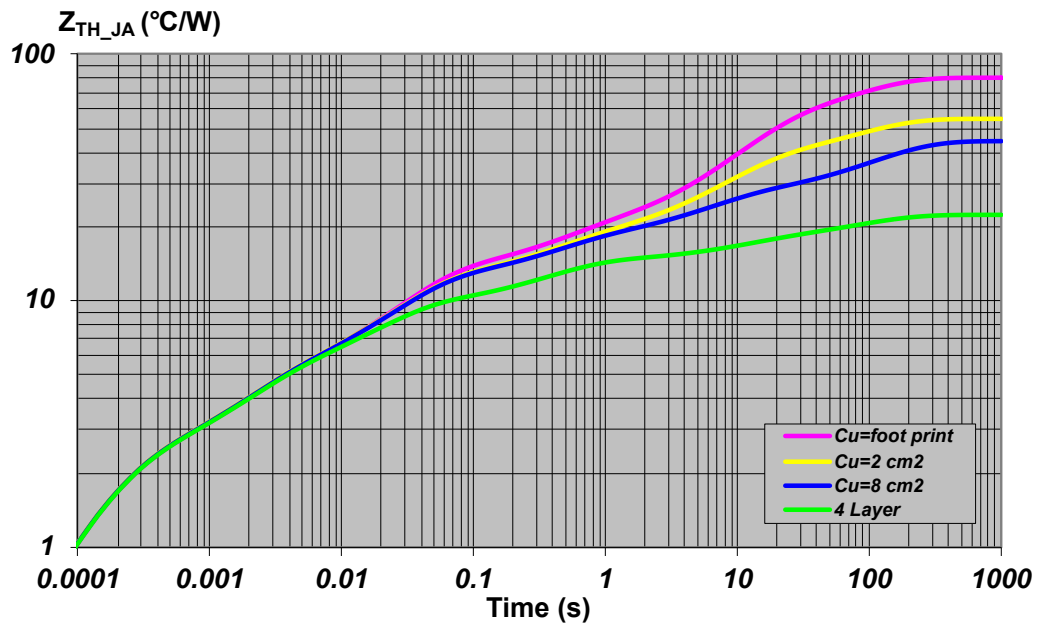


Figure 44. PowerSSO-16 thermal impedance junction ambient single pulse (one channel on)

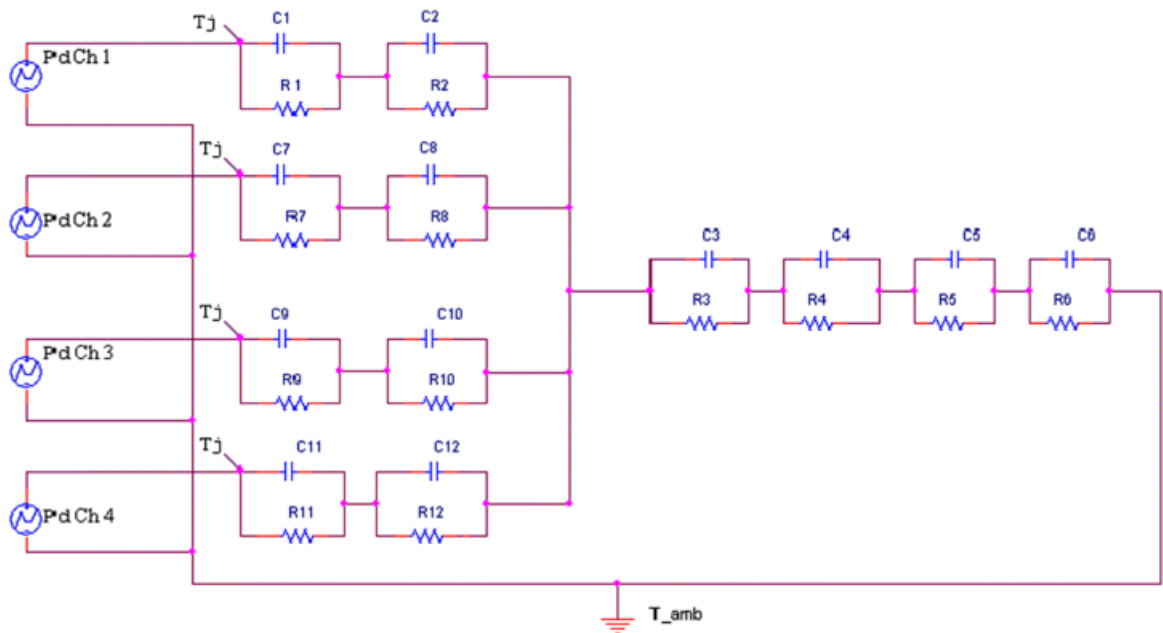


Equation: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp} (1 - \delta)$$

where $\delta = t_p/T$

Figure 45. Thermal fitting model of a double-channel HSD in PowerSSO-16



Note: The fitting model is a simplified thermal tool and is valid for transient evolutions where the embedded protections (power limitation or thermal cycling during thermal shutdown) are not triggered.

Table 15. Thermal parameters

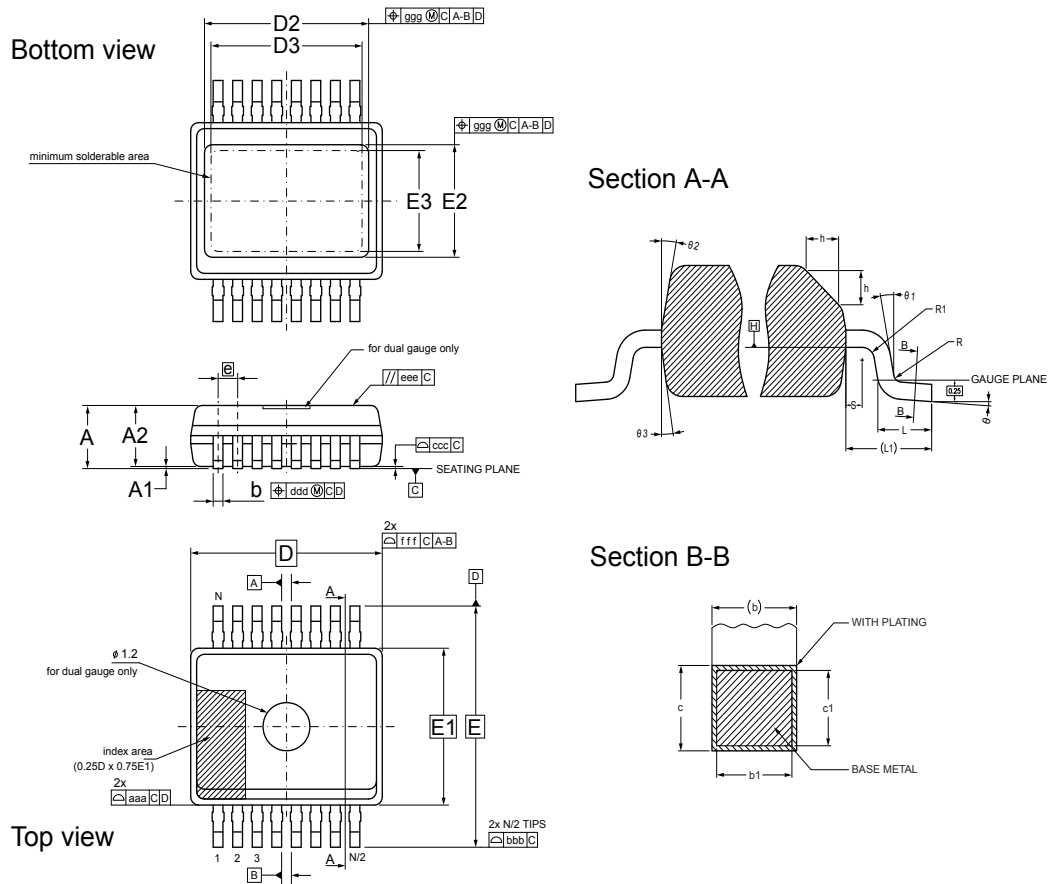
Area/island (cm ²)	FP	2	8	4L
R1 = R7 = R9 = R11 (°C/W)	2	-	-	-
R2 = R8 = R10 = R12 (°C/W)	2.5	-	-	-
R3 (°C/W)	6	5.5	5.5	5
R4 (°C/W)	8.5	7.5	7.5	6
R5 (°C/W)	33	19	9	3
R6 (°C/W)	29	18	18	6
C1 = C7 = C9 = C11 (W·s/°C)	0.00008	-	-	-
C2 = C8 = C10 = C12 (W·s/°C)	0.0008	-	-	-
C3 (W·s/°C)	0.08	-	-	-
C4 (W·s/°C)	0.004	0.004	0.004	0.004
C5 (W·s/°C)	0.4	0.5	0.7	3.5
C6 (W·s/°C)	3	5	7	18

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

7.1 PowerSSO-16 package information

Figure 46. PowerSSO-16 package dimensions



8017965_Rev_9



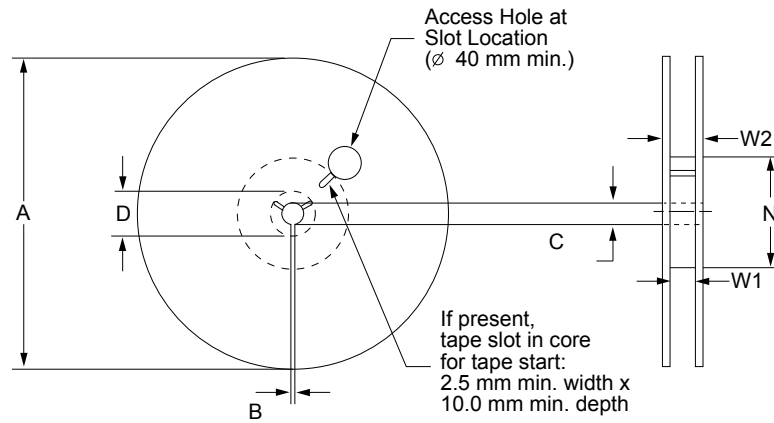
GAPG1605141159CFT

Table 16. PowerSSO-16 mechanical data

Symbol	Millimeters		
	Min.	Typ.	Max.
Θ	0°		8°
Θ1	0°		
Θ2	5°		15°
Θ3	5°		15°
A			1.70
A1	0.00		0.10
A2	1.10		1.60
b	0.20		0.30
b1	0.20	0.25	0.28
c	0.19		0.25
c1	0.19	0.20	0.23
D	4.90 BSC		
D2	3.31		3.91
D3	2.61		
e	0.50 BSC		
E	6.00 BSC		
E1	3.90 BSC		
E2	2.20		2.80
E3	1.49		
h	0.25		0.50
L	0.40	0.60	0.85
L1	1.00 REF		
N	16		
R	0.07		
R1	0.07		
S	0.20		
Tolerance of form and position			
aaa	0.10		
bbb	0.10		
ccc	0.08		
ddd	0.08		
eee	0.10		
fff	0.10		
ggg	0.15		

7.2 PowerSSO-16 packing information

Figure 47. PowerSSO-16 reel 13"



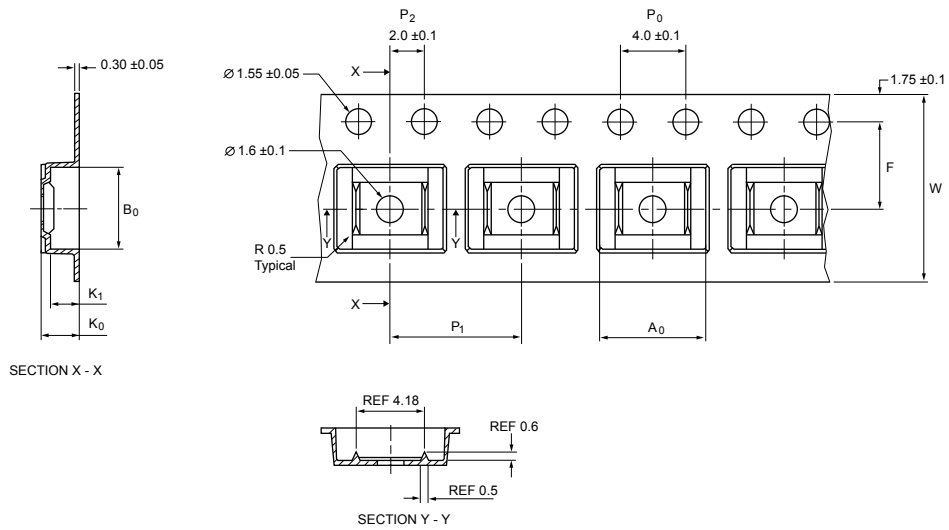
TAPG2004151655CFT

Table 17. Reel dimensions

Description	Value ⁽¹⁾
Base quantity	2500
Bulk quantity	2500
A (max)	330
B (min)	1.5
C (+0.5, -0.2)	13
D (min)	20.2
N	100
W1 (+2 /-0)	12.4
W2 (max)	18.4

1. All dimensions are in mm.

Figure 48. PowerSSO-16 carrier tape



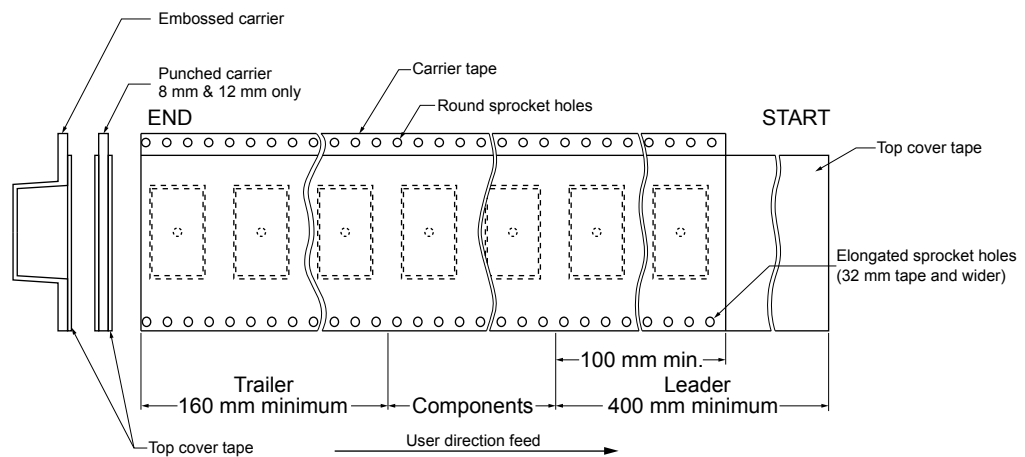
GAPG2204151242CFT

Table 18. PowerSSO-16 carrier tape dimensions

Description	Value ⁽¹⁾
A_0	6.50 ± 0.1
B_0	5.25 ± 0.1
K_0	2.10 ± 0.1
K_1	1.80 ± 0.1
F	5.50 ± 0.1
P_1	8.00 ± 0.1
W	12.00 ± 0.3

1. All dimensions are in mm.

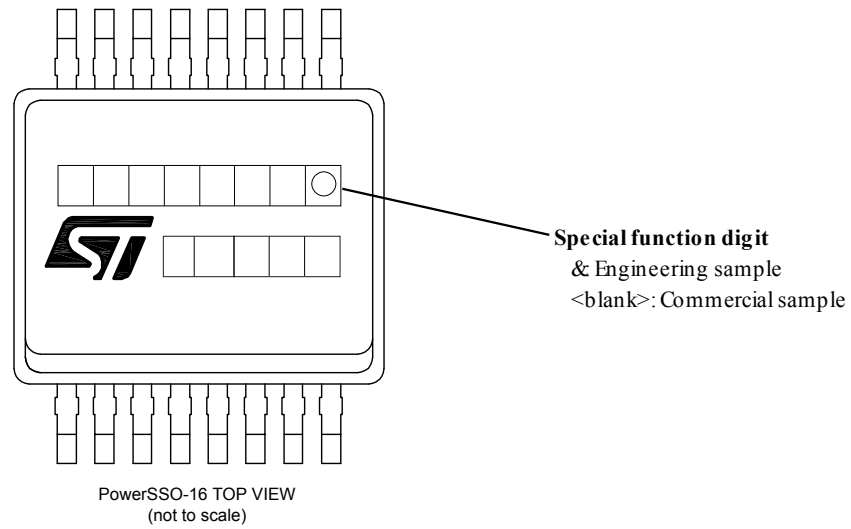
Figure 49. PowerSSO-16 schematic drawing of leader and trailer tape



GAPG2004151511CFT

7.3 PowerSSO-16 marking information

Figure 50. PowerSSO-16 marking information



GADG0310161234SMD

Parts marked as '&' are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

Revision history

Table 19. Document revision history

Date	Revision	Changes
11-Sep-2018	1	Initial release.
24-Sep-2020	2	Updated cover page, <i>Figure 1. Block diagram</i> , <i>Table 3. Absolute maximum ratings</i> . Updated Main electrical characteristics, <i>Section 2.4 Waveforms</i> and <i>Section 3 Protections</i> . Added <i>Application information</i> .
17-Sep-2021	3	Added: <ul style="list-style-type: none"> • <i>Section 5 Maximum demagnetization energy (Vcc = 16 V)</i>; • <i>Section 6 Package and PCB thermal data</i>. Updated: <ul style="list-style-type: none"> • <i>Figure 12. Application diagram</i>; • <i>Figure 16. Analog HSD – open-load detection in off-state</i>; • <i>Table 4. Thermal data</i>; • <i>Table 6. Switching</i>; • <i>Table 9. Current Sense</i>; • <i>Section 7.1 PowerSSO-16 package information</i>. Minor text changes in: <ul style="list-style-type: none"> • <i>Table 3. Absolute maximum ratings</i>; • <i>Table 5. Power section</i>.
26-Jan-2022	4	Updated features list in cover page. Updated <i>Table 8. Protections</i> and <i>Table 9. Current Sense</i> . Updated <i>Figure 12. Application diagram</i> , <i>Figure 13. Simplified internal structure</i> , <i>Section 4.2 Immunity against transient electrical disturbances</i> and <i>Section 4.3 MCU I/Os protection</i> .
16-Jun-2022	5	Added <i>Section 2.5 Electrical characteristics (curves)</i> . Minor text changes.
24-Aug-2022	6	Updated <i>Figure 1. Block diagram</i> . Minor text changes.

Contents

1	Block diagram and pin description	3
2	Electrical specification	5
2.1	Absolute maximum ratings	5
2.2	Thermal data	6
2.3	Main electrical characteristics	7
2.4	Waveforms	17
2.5	Electrical characteristics (curves)	19
3	Protections	23
3.1	Power limitation	23
3.2	Thermal shutdown	23
3.3	Current limitation	23
3.4	Negative voltage clamp	23
4	Application information	24
4.1	GND protection network against reverse battery	24
4.1.1	Diode (DGND) in the ground line	25
4.2	Immunity against transient electrical disturbances	25
4.3	MCU I/Os protection	27
4.4	CS - analog current sense	27
4.4.1	Principle of Current Sense signal generation	28
4.4.2	Short to VCC and OFF-state open-load detection	30
5	Maximum demagnetization energy (Vcc = 16 V)	31
6	Package and PCB thermal data	32
6.1	PowerSSO-16 thermal data	32
7	Package information	35
7.1	PowerSSO-16 package information	35
7.2	PowerSSO-16 packing information	37
7.3	PowerSSO-16 marking information	39
	Revision history	40

List of tables

Table 1.	Pin functions	3
Table 2.	Suggested connections for unused and not connected pins	4
Table 3.	Absolute maximum ratings	5
Table 4.	Thermal data	6
Table 5.	Power section	7
Table 6.	Switching	8
Table 7.	Logic inputs	9
Table 8.	Protections	10
Table 9.	Current Sense	11
Table 10.	Truth table	15
Table 11.	Current sense multiplexer addressing	16
Table 12.	ISO 7637-2 - electrical transient conduction along supply line	25
Table 13.	Current Sense pin levels in off-state	30
Table 14.	PCB properties	32
Table 15.	Thermal parameters	34
Table 16.	PowerSSO-16 mechanical data	36
Table 17.	Reel dimensions	37
Table 18.	PowerSSO-16 carrier tape dimensions	38
Table 19.	Document revision history	40

List of figures

Figure 1.	Block diagram	3
Figure 2.	Configuration diagram (top view)	4
Figure 3.	Current and voltage conventions	5
Figure 4.	Switching time and pulse skew	14
Figure 5.	Current Sense timings (current sense mode)	14
Figure 6.	t_{DSTKON}	15
Figure 7.	Latch-off mode - Intermittent short circuit	17
Figure 8.	Auto-restart mode - Intermittent short circuit	17
Figure 9.	Auto-restart mode - Permanent short circuit	18
Figure 10.	Standby mode activation	18
Figure 11.	Standby state diagram	18
Figure 12.	OFF-state output current	19
Figure 13.	Standby current	19
Figure 14.	$I_{GND(ON)}$ vs I_{out}	19
Figure 15.	Logic input high level voltage	19
Figure 16.	Logic input low level voltage	19
Figure 17.	High level logic input current	19
Figure 18.	Low level logic input current	20
Figure 19.	Logic input hysteresis voltage	20
Figure 20.	FaultRST input clamp voltage	20
Figure 21.	Undervoltage shutdown	20
Figure 22.	On-state resistance vs T_C	20
Figure 23.	On-state resistance vs V_{CC}	20
Figure 24.	Turn-on voltage slope	21
Figure 25.	Turn-off voltage slope	21
Figure 26.	W_{ON} vs T_C	21
Figure 27.	W_{OFF} vs T_C	21
Figure 28.	I_{LIMH} vs T_C	21
Figure 29.	OFF-state open-load voltage detection threshold	21
Figure 30.	V_{SENSE} clamp vs T_C	22
Figure 31.	V_{SENSEH} vs T_C	22
Figure 32.	Application diagram	24
Figure 33.	Simplified internal structure	24
Figure 34.	M0-9 application schematic	26
Figure 35.	Current Sense and diagnostic – block diagram	27
Figure 36.	Current Sense block diagram	28
Figure 37.	Analog HSD – open-load detection in off-state	29
Figure 38.	Open-load / short to V_{CC} condition	29
Figure 39.	Maximum turn off current versus inductance	31
Figure 40.	Maximum turn off energy versus inductance	31
Figure 41.	PowerSSO-16 on two-layer PCB (2s0p to JEDEC JESD 51-5)	32
Figure 42.	PowerSSO-16 on four-layer PCB (2s2p to JEDEC JESD 51-7)	32
Figure 43.	$R_{thj-amb}$ vs PCB copper area in open box free air condition (one channel on)	33
Figure 44.	PowerSSO-16 thermal impedance junction ambient single pulse (one channel on)	33
Figure 45.	Thermal fitting model of a double-channel HSD in PowerSSO-16	34
Figure 46.	PowerSSO-16 package dimensions	35
Figure 47.	PowerSSO-16 reel 13"	37
Figure 48.	PowerSSO-16 carrier tape	38
Figure 49.	PowerSSO-16 schematic drawing of leader and trailer tape	38
Figure 50.	PowerSSO-16 marking information	39

IMPORTANT NOTICE – READ CAREFULLY

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgment.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, refer to www.st.com/trademarks. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2022 STMicroelectronics – All rights reserved