



## STM32L412xx/422xB device errata

### Applicability

This document applies to the part numbers of STM32L412xx/422xB devices and the device variants as stated in this page. It gives a summary and a description of the device errata, with respect to the device datasheet and reference manual RM0394. Deviation of the real device behavior from the intended device behavior is considered to be a device limitation. Deviation of the description in the reference manual or the datasheet from the intended device behavior is considered to be a documentation erratum. The term “*errata*” applies both to limitations and documentation errata.

**Table 1. Device summary**

Reference	Part numbers
STM32L412xx	STM32L412C8, STM32L412CB, STM32L412K8, STM32L412KB, STM32L412R8, STM32L412RB, STM32L412T8, STM32L412TB
STM32L422xB	STM32L422CB, STM32L422KB, STM32L422RB, STM32L422TB

**Table 2. Device variants**

Reference	Silicon revision codes	
	Device marking <sup>(1)</sup>	REV_ID <sup>(2)</sup>
STM32L412xx	A	0x1000
STM32L422xB	A	0x1000

1. Refer to the device datasheet for how to identify this code on different types of package.
2. REV\_ID[15:0] bitfield of DBGMCU\_IDCODE register.

# 1 Summary of device errata

The following table gives a quick reference to the STM32L412xx/422xB device limitations and their status:

A = limitation present, workaround available

N = limitation present, no workaround available

P = limitation present, partial workaround available

“-” = limitation absent

Applicability of a workaround may depend on specific conditions of target application. Adoption of a workaround may cause restrictions to target application. Workaround for a limitation is deemed partial if it only reduces the rate of occurrence and/or consequences of the limitation, or if it is fully effective for only a subset of instances on the device or in only a subset of operating modes, of the function concerned.

**Table 3. Summary of device limitations**

Function	Section	Limitation	Status
			Rev. A
Core	2.1.1	Interrupted loads to SP can cause erroneous behavior	A
	2.1.2	VDIV or VSQRT instructions might not complete correctly when very short ISRs are used	A
	2.1.3	Store immediate overlapping exception return operation might vector to incorrect interrupt	A
System	2.2.1	Internal voltage reference corrupted upon Stop mode entry with temperature sensing enabled	A
	2.2.2	Full JTAG configuration without NJTRST pin cannot be used	A
	2.2.3	Current injection from V <sub>DD</sub> to V <sub>DDA</sub> through analog switch voltage booster	A
	2.2.4	Unstable LSI when it clocks RTC or CSS on LSE	P
	2.2.5	LSESYSDIS has no effects if set just before Stop entry	A
	2.2.6	PB8 and PB11 on 48-pin devices with SMPS remain software configurable	A
	2.2.7	FLASH_ECCR corrupted upon reset or power-down occurring during flash memory program or erase operation	A
	2.2.8	HSE oscillator long startup at low voltage	P
	2.2.9	LSE crystal oscillator may be disturbed by transitions on PC13	N
	2.2.10	SRAM write error	A
	2.2.11	Corrupted content of the backup domain due to a missed power-on reset after this domain supply voltage drop	A
	2.2.12	Debugging Sleep/Stop mode with WFE/WFI entry	A
FW	2.3.1	Code segment unprotected if non-volatile data segment length is zero	A
DMA	2.4.1	DMA disable failure and error flag omission upon simultaneous transfer error and global flag clear	A
QUADSPI	2.5.1	First nibble of data not written after dummy phase	A
	2.5.2	Wrong data from memory-mapped read after an indirect mode operation	A
	2.5.3	Memory-mapped read operations may fail when timeout counter is enabled	P
	2.5.4	Memory-mapped access in indirect mode clearing QUADSPI_AR register	P
	2.5.5	Transmission error flag (TEF) in memory space access with ADMODE = 0	N
ADC	2.6.3	New context conversion initiated without waiting for trigger when writing new context in ADC_JSQR with JQDIS = 0 and JQM = 0	A
	2.6.4	Two consecutive context conversions fail when writing new context in ADC_JSQR just after previous context completion with JQDIS = 0 and JQM = 0	A

Function	Section	Limitation	Status
			Rev. A
ADC	2.6.5	Unexpected regular conversion when two consecutive injected conversions are performed in Dual interleaved mode	A
	2.6.6	ADC_AWDy_OUT reset by non-guarded channels	A
	2.6.7	Injected data stored in the wrong ADC_JDRx registers	A
	2.6.8	ADC slave data may be shifted in Dual regular simultaneous mode	A
	2.6.9	Writing ADCx_JSQR when JADCSTART and JQDIS are set might lead to incorrect behavior	N
	2.6.10	Wrong ADC result if conversion done late after calibration or previous conversion	A
	2.6.11	Spurious temperature measurement due to spike noise	A
	2.6.12	Selected external ADC inputs unduly clamped to V <sub>DD</sub> when all analog peripherals are disabled	A
TSC	2.7.2	TSC signal-to-noise concern under specific conditions	A
TIM	2.10.1	One-pulse mode trigger not detected in master-slave reset + trigger configuration	P
	2.10.2	Consecutive compare event missed in specific conditions	N
	2.10.3	Output compare clear not working with external counter reset	P
LPTIM	2.11.1	Device may remain stuck in LPTIM interrupt when entering Stop mode	A
	2.11.2	ARRM and CMPM flags are not set when APB clock is slower than kernel clock	A
	2.11.3	Device may remain stuck in LPTIM interrupt when clearing event flag	A
	2.11.4	LPTIM events and PWM output are delayed by one kernel clock cycle	A
RTC and TAMP	2.12.1	RTC_MISR and TAMP_MISR can be read by non-privileged accesses when privilege-protected	N
	2.12.2	RTC configuration changes ignored at specific conditions	A
	2.12.3	Calibration formula changes when LPCAL is set	A
	2.12.4	Calendar initialization may fail in case of consecutive INIT mode entry	A
	2.12.5	Alarm flag may be repeatedly set when the core is stopped in debug	N
	2.12.6	A tamper event fails to trigger timestamp or timestamp overflow events during a few cycles after clearing TSF	N
	2.12.7	Spurious RTC alarm EXTI line event following RTC WUT interrupt	A
	2.12.8	RTC_REFIN and RTC_OUT on PB2 not operating in Stop 2 mode	P
	2.12.10	V <sub>BAT</sub> tamper limitation	A
	2.12.11	RTC_OUT redirection to PB2 does not release PC13	N
I2C	2.13.1	10-bit master mode: new transfer cannot be launched if first part of the address is not acknowledged by the slave	A
	2.13.3	Wrong data sampling when data setup time (t <sub>SU, DAT</sub> ) is shorter than one I2C kernel clock period	P
	2.13.4	Spurious bus error detection in master mode	A
	2.13.5	Last-received byte loss in reload mode	P
	2.13.6	Spurious master transfer upon own slave address match	P
	2.13.8	OVR flag not set in underrun condition	N
	2.13.9	Transmission stalled after first byte transfer	A
	2.13.10	SDA held low upon SMBus timeout expiry in slave mode	A

Function	Section	Limitation	Status
			Rev. A
USART	2.14.1	RTS is active while RE = 0 or UE = 0	A
	2.14.2	Receiver timeout counter wrong start in two-stop-bit configuration	A
	2.14.3	Data corruption due to noisy receive line	A
	2.14.4	Received data may be corrupted upon clearing the ABREN bit	A
	2.14.5	Noise error flag set while ONEBIT is set	N
LPUART	2.15.1	RTS is active while RE = 0 or UE = 0	A
	2.15.2	Possible LPUART transmitter issue when using low BRR[15:0] value	P
SPI	2.16.1	BSY bit may stay high when SPI is disabled	A
	2.16.2	BSY bit may stay high at the end of data transfer in slave mode	A
	2.16.3	SPI master communication failure at high SYSCLK frequency within the specified voltage range	A
USB	2.17.2	ESOF interrupt timing desynchronized after resume signaling	A
	2.17.3	Incorrect CRC16 in the memory buffer	N
	2.17.4	Buffer description table update completes after CTR interrupt triggers	A

The following table gives a quick reference to the documentation errata.

**Table 4. Summary of device documentation errata**

Function	Section	Documentation erratum
DMA	2.4.2	Byte and half-word accesses not supported
ADC	2.6.1	Writing ADC_JSQR when JADCSTART and JQDIS are set may lead to incorrect behavior
	2.6.2	ADEN bit cannot be set immediately after the ADC calibration is done
TSC	2.7.1	Inhibited acquisition in short transfer phase configuration
RNG	2.8.1	RNG clock error does not stop random numbers
AES	2.9.1	TAG computation in GCM encryption mode
	2.9.2	CCM authentication mode not compliant with NIST CMAC
	2.9.3	Datatype initial configuration in GCM mode
	2.9.4	Wait until BUSY is low when suspending GCM encryption
RTC and TAMP	2.12.9	Setting GPIO properties of PC13 used as RTC_ALARM open-drain output
I2C	2.13.2	Wrong behavior in Stop mode when wake-up from Stop mode is disabled in I2C
	2.13.7	START bit is cleared upon setting ADDRCF, not upon address match
USB	2.17.1	Possible packet memory overrun/underrun at low APB frequency

## 2 Description of device errata

The following sections describe the errata of the applicable devices with Arm® core and provide workarounds if available. They are grouped by device functions.

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### 2.1 Core

Reference manual and errata notice for the Arm® Cortex®-M4F core revision r0p1 is available from <http://infocenter.arm.com>.

#### 2.1.1 Interrupted loads to SP can cause erroneous behavior

This limitation is registered under Arm ID number 752770 and classified into “Category B”. Its impact to the device is minor.

##### Description

If an interrupt occurs during the data-phase of a single word load to the stack-pointer (SP/R13), erroneous behavior can occur. In all cases, returning from the interrupt will result in the load instruction being executed an additional time. For all instructions performing an update to the base register, the base register will be erroneously updated on each execution, resulting in the stack-pointer being loaded from an incorrect memory location.

The affected instructions that can result in the load transaction being repeated are:

- LDR SP, [Rn],#imm
- LDR SP, [Rn,#imm]!
- LDR SP, [Rn,#imm]
- LDR SP, [Rn]
- LDR SP, [Rn,Rm]

The affected instructions that can result in the stack-pointer being loaded from an incorrect memory address are:

- LDR SP,[Rn],#imm
- LDR SP,[Rn,#imm]!

As compilers do not generate these particular instructions, the limitation is only likely to occur with hand-written assembly code.

##### Workaround

Both issues may be worked around by replacing the direct load to the stack-pointer, with an intermediate load to a general-purpose register followed by a move to the stack-pointer.

#### 2.1.2 VDIV or VSQRT instructions might not complete correctly when very short ISRs are used

This limitation is registered under Arm ID number 776924 and classified into “Category B”. Its impact to the device is limited.

##### Description

The VDIV and VSQRT instructions take 14 cycles to execute. When an interrupt is taken a VDIV or VSQRT instruction is not terminated, and completes its execution while the interrupt stacking occurs. If lazy context save of floating point state is enabled then the automatic stacking of the floating point context does not occur until a floating point instruction is executed inside the interrupt service routine.

Lazy context save is enabled by default. When it is enabled, the minimum time for the first instruction in the interrupt service routine to start executing is 12 cycles. In certain timing conditions, and if there is only one or two instructions inside the interrupt service routine, then the VDIV or VSQRT instruction might not write its result to the register bank or to the FPSCR.

The failure occurs when the following condition is met:

1. The floating point unit is enabled
2. Lazy context saving is not disabled
3. A VDIV or VSQRT is executed
4. The destination register for the VDIV or VSQRT is one of s0 - s15
5. An interrupt occurs and is taken
6. The interrupt service routine being executed does not contain a floating point instruction
7. Within 14 cycles after the VDIV or VSQRT is executed, an interrupt return is executed

A minimum of 12 of these 14 cycles are utilized for the context state stacking, which leaves 2 cycles for instructions inside the interrupt service routine, or 2 wait states applied to the entire stacking sequence (which means that it is not a constant wait state for every access).

In general, this means that if the memory system inserts wait states for stack transactions (that is, external memory is used for stack data), then this erratum cannot be observed.

The effect of this erratum is that the VDIV or VSQRT instruction does not complete correctly and the register bank and FPSCR are not updated, which means that these registers hold incorrect, out of date, data.

### Workaround

A workaround is only required if the floating point unit is enabled. A workaround is not required if the stack is in external memory.

There are two possible workarounds:

- Disable lazy context save of floating point state by clearing LSPEN to 0 (bit 30 of the FPCCR at address 0xE000EF34).
- Ensure that every interrupt service routine contains more than 2 instructions in addition to the exception return instruction.

## 2.1.3 Store immediate overlapping exception return operation might vector to incorrect interrupt

This limitation is registered under Arm ID number 838869 and classified into “Category B (rare)”. Its impact to the device is minor.

### Description

The core includes a write buffer that permits execution to continue while a store is waiting on the bus. Under specific timing conditions, during an exception return while this buffer is still in use by a store instruction, a late change in selection of the next interrupt to be taken might result in there being a mismatch between the interrupt acknowledged by the interrupt controller and the vector fetched by the processor.

The failure occurs when the following condition is met:

1. The handler for interrupt A is being executed.
2. Interrupt B, of the same or lower priority than interrupt A, is pending.
3. A store with immediate offset instruction is executed to a bufferable location.
  - STR/STRH/STRB <Rt>, [<Rn>,#imm]
  - STR/STRH/STRB <Rt>, [<Rn>,#imm]!
  - STR/STRH/STRB <Rt>, [<Rn>],#imm
4. Any number of additional data-processing instructions can be executed.
5. A BX instruction is executed that causes an exception return.
6. The store data has wait states applied to it such that the data is accepted at least two cycles after the BX is executed.
  - Minimally, this is two cycles if the store and the BX instruction have no additional instructions between them.
  - The number of wait states required to observe this erratum needs to be increased by the number of cycles between the store and the interrupt service routine exit instruction.
7. Before the bus accepts the buffered store data, another interrupt C is asserted which has the same or lower priority as A, but a greater priority than B.

Example:

The processor should execute interrupt handler C, and on completion of handler C should execute the handler for B. If the conditions above are met, then this erratum results in the processor erroneously clearing the pending state of interrupt C, and then executing the handler for B twice. The first time the handler for B is executed it will be at interrupt C's priority level. If interrupt C is pending by a level-based interrupt which is cleared by C's handler then interrupt C will be pending again once the handler for B has completed and the handler for C will be executed.

As the STM32 interrupt C is level based, it eventually becomes pending again and is subsequently handled.

### Workaround

For software not using the memory protection unit, this erratum can be worked around by setting DISDEFWBUF in the Auxiliary Control Register.

In all other cases, the erratum can be avoided by ensuring a DSB occurs between the store and the BX instruction. For exception handlers written in C, this can be achieved by inserting the appropriate set of intrinsics or inline assembly just before the end of the interrupt function, for example:

ARMCC:

```
...
__schedule_barrier();
__asm{DSB};
__schedule_barrier();
}
```

GCC:

```
...
__asm volatile ("dsb 0xf" ::: "memory");
}
```

## 2.2 System

### 2.2.1 Internal voltage reference corrupted upon Stop mode entry with temperature sensing enabled

#### Description

When entering Stop mode with the temperature sensor channel and the associated ADC(s) enabled, the internal voltage reference may be corrupted.

The occurrence of the corruption depends on the supply voltage and the temperature.

The corruption of the internal voltage reference may cause:

- an overvoltage in  $V_{CORE}$  domain
- an overshoot / undershoot of internal clock (LSI, HSI, MSI) frequencies
- a spurious brown-out reset

The limitation applies to Stop 1 and Stop 2 modes.

#### Workaround

Before entering Stop mode:

- Disable the ADC(s) using the temperature sensor signal as input, and/or
- Disable the temperature sensor channel, by clearing the CH17SEL bit of the ADCx\_CCR register.

Disabling both the ADC(s) and the temperature sensor channel reduces the power consumption during Stop mode.

### 2.2.2 Full JTAG configuration without NJTRST pin cannot be used

#### Description

When using the JTAG debug port in Debug mode, the connection with the debugger is lost if the NJTRST pin (PB4) is used as a GPIO or for an alternate function other than NJTRST. Only the 4-wire JTAG port configuration is impacted.

### Workaround

Use the SWD debug port instead of the full 4-wire JTAG port.

## 2.2.3 Current injection from $V_{DD}$ to $V_{DDA}$ through analog switch voltage booster

### Description

With  $V_{DDA}$  below 2.4 V and  $V_{DD}$  above 3 V, a small current injected from VDD line to VDDA line may cause  $V_{DDA}$  to exceed its nominal value.

This current injection only occurs when the I/O analog switch voltage booster is disabled (the BOOSTEN bit of the SYSCFG\_CFGR1 register is cleared) and at least one of the analog peripherals (ADC, COMP, or OPAMP) is enabled.

### Workaround

Enable the I/O analog switch voltage booster, by setting the BOOSTEN bit of the SYSCFG\_CFGR1 register. when  $V_{DDA}$  is below 2.4 V and  $V_{DD}$  is above 3 V.

## 2.2.4 Unstable LSI when it clocks RTC or CSS on LSE

### Description

The LSI clock can become unstable (duty cycle different from 50 %) and its maximum frequency can become significantly higher than 32 kHz, when:

- LSI clocks the RTC, or it clocks the clock security system (CSS) on LSE (which holds when the LSECSSON bit set), and
- the  $V_{DD}$  power domain is reset while the backup domain is not reset, which happens:
  - upon exiting Shutdown mode
  - if  $V_{BAT}$  is separate from  $V_{DD}$  and  $V_{DD}$  goes off then on
  - if  $V_{BAT}$  is tied to  $V_{DD}$  (internally in the package for products not featuring the VBAT pin, or externally) and a short ( $< 1$  ms)  $V_{DD}$  drop under  $V_{DD}(\min)$  occurs

### Workaround

Apply one of the following measures:

- Clock the RTC with LSE or HSE/32, without using the CSS on LSE
- If LSI clocks the RTC or when the LSECSSON bit is set, reset the backup domain upon each  $V_{DD}$  power up (when the BORRSTF flag is set). If  $V_{BAT}$  is separate from  $V_{DD}$ , also restore the RTC configuration, backup registers and anti-tampering configuration.

## 2.2.5 LSESYSDIS has no effects if set just before Stop entry

### Description

The LSE clock disable is only effective two LSE clocks after setting the LSESYSDIS bit of the RCC\_BDCR register. If Stop 2 low-power mode is entered before that instant, the LSE clock is not effectively disabled and its propagation in the device leads to excessive consumption in Stop 2 mode.

### Workaround

Upon setting the LSESYSDIS bit of the RCC\_BDCR register, wait for at least two LSE clock periods before entering Stop 2 mode.



## 2.2.6 PB8 and PB11 on 48-pin devices with SMPS remain software configurable

### Description

On 48-pin devices with SMPS support, the non-bonded PB8 and PB11 GPIOs remain software configurable. Their software configuration as floating inputs may lead to increased power consumption.

### Workaround

Do not configure the PB8 and PB11 GPIOs as floating inputs.

## 2.2.7 FLASH\_ECCR corrupted upon reset or power-down occurring during flash memory program or erase operation

### Description

Reset or power-down occurring during a flash memory location program or erase operation, followed by a read of the same memory location, may lead to a corruption of the FLASH\_ECCR register content.

### Workaround

Under such condition, erase the page(s) corresponding to the flash memory location.

## 2.2.8 HSE oscillator long startup at low voltage

### Description

When  $V_{DD}$  is below 2.7 V, the HSE oscillator may take longer than specified to start up. Several hundred milliseconds might elapse before the HSERDY flag in the RCC\_CR register is set.

### Workaround

The following sequence is recommended:

1. Configure PH0 and PH1 as standard GPIOs in output mode and low-level state.
2. Enable the HSE oscillator.

## 2.2.9 LSE crystal oscillator may be disturbed by transitions on PC13

### Description

On LQFP and UFQFPN packages, the LSE crystal oscillator clock frequency can be incorrect when PC13 is toggling in input or output (for example when used for RTC\_OUT1).

The external clock input (LSE bypass) is not impacted by this limitation.

The WLCSP and UFBGA packages are not impacted by this limitation.

### Workaround

None.

Avoid toggling PC13 when LSE is used on LQFP and UFQFPN packages.

## 2.2.10 SRAM write error

### Description

In rare cases, system reset occurring in a critical instant may upset the SRAM state machine. The first SRAM read or write access after the system reset then restores the normal operation of the SRAM for any subsequent accesses. However, if it is a write access, it fails to write data.

### Workaround

Upon system reset, make a dummy read access to each 32-Kbyte SRAM instance used by the application, through one of the following methods:

1. Place a dummy variable initialization, which allows the compiler to create the assembly code.
2. Use this initialization assembly code:

```
MOV32  R0, #0x20000000 //SRAM1 address
LDR    R1, [R0, #+0]  //read access
MOV32  R0, #0x20008000 //SRAM2 instance
LDR    R1, [R0, #+0]  //dummy read, no consequence on R1 value
...
```

Follow the first method for SRAM instances with the parity check enabled. Follow the first or the second method for SRAM instances with the parity check disabled.

## 2.2.11 Corrupted content of the backup domain due to a missed power-on reset after this domain supply voltage drop

### Description

The backup domain reset may be missed upon a power-on following a power-off, if its supply voltage drops during the power-off phase hitting a window, which is few mV wide before it starts to rise again. In this critical window, the flip-flops are no longer able to safely retain the information and the backup domain reset has not yet been triggered. This window is located in the range between 100 mV and 700 mV, with the exact position depending mainly on the device and on the temperature.

This missed reset results in unpredictable values of the backup domain registers. This may cause a spurious behavior (such as driving the LSCO output pin on PA2 or influencing backup functions).

### Workaround

Apply one of the following measures:

- In the application, let the  $V_{DD}$  and  $V_{BAT}$  supply voltages fall to a level below 100 mV for more than 200 ms before a new power-on.
- If the above workaround cannot be applied, and the boot follows a power-on reset, erase the backup domain by software.

When the application is using shutdown mode, user needs to discriminate between the power-on reset or an exit from a shutdown mode.

For this purpose, at least one backup register must have been previously programmed with a BKP\_REG\_VAL value with 16 bits set and 16 bits cleared.

Robustness of this workaround can be significantly improved by using a CRC rather than registers. The registers are subject to backup domain reset.

The workaround consists of calculating the CRC of the backup registers: RCC\_BDCR and RTC registers, excluding bits modified by HW.

The CRC result can be stored in the backup register instead of a fixed value. This value needs to be updated for each modification of values covered by CRC, such as by using CRC peripheral.

At the very beginning of the boot code, insert the following software sequence:

1. Check the BORRSTF flag of the RCC\_CSR register. If set, the reset is caused by a power on, or is exiting from shutdown mode.
2. If BORRSTF flag is true, and the shutdown mode is used in the application, check that the backup register value is different from BKP\_REG\_VAL. When tamper detection is enabled, check that no tamper flag is set. If both conditions are met then the reset is caused by a power-on.
3. If the reset is caused by a power-on, apply the following sequence:
  - a. Enable the PWR clock in the RCC, by setting the PWREN bit.
  - b. Enable the backup domain access in the PWR, by setting the DBP bit.
  - c. Reset the backup domain, by:
    - i. Writing 0x0001 0000 in the RCC\_BDCR register, which sets the BDRST bit and clears other register bits that might not be reset.
    - ii. reading the RCC\_BDCR register, to make the reset time long enough
    - iii. writing 0x0000 0000 in the RCC\_BDCR register, to clear the BDRST bit
  - d. Clear the BORRSTF flag by setting the RMVF bit of the RCC\_CSR register.

## 2.2.12 Debugging Sleep/Stop mode with WFE/WFI entry

### Description

When the Sleep debug or Stop debug mode is enabled (DBG\_SLEEP bit or DBG\_STOP bit is set in the DBGMCU\_CR register), software debugging is permitted during Sleep or Stop mode. However, after wake-up, some unreachable instructions may be executed if the following conditions are met: • The application software has disabled the Prefetch queue. • The number of wait states configured for the flash memory interface is greater than zero. • The linker has placed the WFE or WFI instruction on a 4-byte aligned address (0x080xx xxx4).

### Workaround

Choose one of the following measures to apply:

- Add three NOPs after WFI/WFE instruction.
- Keep one AHB master active during Sleep (For example: keep DMA1 or DMA2 RCC clock enable bit set).
- Execute WFI/WFE instruction from routines inside the SRAM.

## 2.3 FW

### 2.3.1 Code segment unprotected if non-volatile data segment length is zero

#### Description

If during FW configuration the length of firewall-protected non-volatile data segment is set to zero through the LENG[21:8] bitfield of the FW\_NVDSL register, the firewall protection of code segment does not operate.

#### Workaround

Always set the LENG[21:8] bitfield of the FW\_NVDSL register to a non-zero value, even if no firewall protection of data in the non-volatile data segment is required.

## 2.4 DMA

### 2.4.1 DMA disable failure and error flag omission upon simultaneous transfer error and global flag clear

#### Description

Upon a data transfer error in a DMA channel x, both the specific TEIFx and the global GIFx flags are raised and the channel x is normally automatically disabled. However, if in the same clock cycle the software clears the GIFx flag (by setting the CGIFx bit of the DMA\_IFCR register), the automatic channel disable fails and the TEIFx flag is not raised.

This issue does not occur with ST's HAL software that does not use and clear the GIFx flag when the channel is active.

#### Workaround

Do not clear GIFx flags when the channel is active. Instead, use HTIFx, TCIFx, and TEIFx specific event flags and their corresponding clear bits.

### 2.4.2 Byte and half-word accesses not supported

#### Description

Some reference manual revisions may wrongly state that the DMA registers are byte- and half-word-accessible. Instead, the DMA registers must always be accessed through aligned 32-bit words. Byte or half-word write accesses cause an erroneous behavior.

ST's low-level driver and HAL software only use aligned 32-bit accesses to the DMA registers.

This is a description inaccuracy issue rather than a product limitation.

### Workaround

No application workaround is required.

## 2.5 QUADSPI

### 2.5.1 First nibble of data not written after dummy phase

#### Description

The first nibble of data to be written to the external flash memory is lost when the following condition is met:

- QUADSPI is used in indirect write mode.
- At least one dummy cycle is used.

#### Workaround

Use alternate bytes instead of dummy phase to add latency between the address phase and the data phase. This works only if the number of dummy cycles to substitute corresponds to a multiple of eight bits of data.

Example:

- To substitute one dummy cycle, send one alternate byte (only possible in DDR mode with four data lines).
- To substitute two dummy cycles, send one alternate byte in SDR mode with four data lines.
- To substitute four dummy cycles, send two alternate bytes in SDR mode with four data lines, or one alternate byte in SDR mode with two data lines.
- To substitute eight dummy cycles, send one alternate byte in SDR mode with one data line.

### 2.5.2 Wrong data from memory-mapped read after an indirect mode operation

#### Description

The first memory-mapped read in indirect mode can yield wrong data if the QUADSPI peripheral enters memory-mapped mode with bits ADDRESS[1:0] of the QUADSPI\_AR register both set.

#### Workaround

Before entering memory-mapped mode, apply the following measure, depending on access mode:

- Indirect read mode: clear the QUADSPI\_AR register then issue an abort request to stop reading and to clear the BUSY bit.
- Indirect write mode: clear the QUADSPI\_AR register.

**Caution:** *The QUADSPI\_DR register must not be written after clearing the QUADSPI\_AR register.*

### 2.5.3 Memory-mapped read operations may fail when timeout counter is enabled

#### Description

In memory-mapped mode with the timeout counter enabled (by setting the TCEN bit of the QUADSPI\_CR register), the QUADSPI peripheral may hang and memory-mapped read operation fail. This occurs if the timeout flag TOF is set at the same clock edge as a new memory-mapped read request.

#### Workaround

Disable the timeout counter. To raise the chip select, perform an abort at the end of each memory-mapped read operation.

## 2.5.4 Memory-mapped access in indirect mode clearing QUADSPI\_AR register

### Description

Memory-mapped accesses to the QUADSPI peripheral operating in indirect mode unduly clear the QUADSPI\_AR register to 0x00.

### Workaround

Adopt one of the following measures:

- Avoid memory-mapped accesses to the QUADSPI peripheral operating in indirect mode.
- After each memory-mapped access to the QUADSPI operating in indirect mode, write the QUADSPI\_AR register with a desired value

## 2.5.5 Transmission error flag (TEF) in memory space access with ADMODE = 0

### Description

The TEF (Transmission Error Flag) is designed to signal when memory is accessed outside of the memory address range. The controller calculates the address from the address register and the number of bytes to transfer to determine if the transaction hits the memory outside of the memory space.

However, if the previous transfer is closed to the end of the memory space and the number of bytes for the new transfer exceeds the memory size, even if no address is requested (ADMODE = 0), the TEF flag may be raised incorrectly. This is because the controller performs the check even if there are no address phases inside the transaction.

### Workaround

To avoid the incorrect TEF assertion, the software application can clear the address register QUADSPI\_AR when starting the transaction with ADMODE = 0.

Additionally, the HAL library driver has been updated to prevent this incorrect TEF assertion in this context.

## 2.6 ADC

### 2.6.1 Writing ADC\_JSQR when JADCSTART and JQDIS are set may lead to incorrect behavior

#### Description

Some reference manual revisions specify that the ADC\_JSQR register can be written when an injected conversion is ongoing (JADCSTART = 1). This may lead to unpredictable ADC behavior if the queues of context are not enabled (JQDIS = 1).

#### Workaround

No application workaround is required for this description inaccuracy issue.

### 2.6.2 ADEN bit cannot be set immediately after the ADC calibration is done

#### Description

Some reference manual revisions may not indicate that the ADEN bit cannot be set while the ADCAL bit is set and during a four ADC clock cycles after the ADCAL bit is cleared by hardware (end of the calibration).

Otherwise, if the ADEN bit is set during this four ADC clock cycle period, it will be reset by the calibration logic and the ADC will stay disabled. This is due to the fact that there is an internal reset of the ADEN bit four ADC clock cycles after the ADCAL bit is cleared by hardware.

#### Workaround

No application workaround is required for this description inaccuracy issue.

### 2.6.3 New context conversion initiated without waiting for trigger when writing new context in ADC\_JSQR with JQDIS = 0 and JQM = 0

#### Description

Once an injected conversion sequence is complete, the queue is consumed and the context changes according to the new ADC\_JSQR parameters stored in the queue. This new context is applied for the next injected sequence of conversions.

However, the programming of the new context in ADC\_JSQR (change of injected trigger selection and/or trigger polarity) may launch the execution of this context without waiting for the trigger if:

- the queue of context is enabled (JQDIS cleared to 0 in ADC\_CFGR), and
- the queue is never empty (JQM cleared to 0 in ADC\_CFGR), and
- the injected conversion sequence is complete and no conversion from previous context is ongoing

#### Workaround

Apply one of the following measures:

- Ignore the first conversion.
- Use a queue of context with JQM = 1.
- Use a queue of context with JQM = 0, only change the conversion sequence but never the trigger selection and the polarity.

### 2.6.4 Two consecutive context conversions fail when writing new context in ADC\_JSQR just after previous context completion with JQDIS = 0 and JQM = 0

#### Description

When an injected conversion sequence is complete and the queue is consumed, writing a new context in ADC\_JSQR just after the completion of the previous context and with a length longer than the previous context, may cause both contexts to fail. The two contexts are considered as one single context. As an example, if the first context contains element 1 and the second context elements 2 and 3, the first context is consumed followed by elements 2 and 3 and element 1 is not executed.

This issue may happen if:

- the queue of context is enabled (JQDIS cleared to 0 in ADC\_CFGR), and
- the queue is never empty (JQM cleared to 0 in ADC\_CFGR), and
- the length of the new context is longer than the previous one

#### Workaround

If possible, synchronize the writing of the new context with the reception of the new trigger.

### 2.6.5 Unexpected regular conversion when two consecutive injected conversions are performed in Dual interleaved mode

#### Description

In Dual ADC mode, an unexpected regular conversion may start at the end of the second injected conversion without a regular trigger being received, if the second injected conversion starts exactly at the same time than the end of the first injected conversion. This issue may happen in the following conditions:

- two consecutive injected conversions performed in Interleaved simultaneous mode (DUAL[4:0] of ADC\_CCR = 0b00011), or
- two consecutive injected conversions from master or slave ADC performed in Interleaved mode (DUAL[4:0] of ADC\_CCR = 0b00111)

#### Workaround

- In Interleaved simultaneous injected mode: make sure the time between two injected conversion triggers is longer than the injected conversion time.

- In Interleaved only mode: perform injected conversions from one single ADC (master or slave), making sure the time between two injected triggers is longer than the injected conversion time.

### 2.6.6 ADC\_AWDy\_OUT reset by non-guarded channels

#### Description

ADC\_AWDy\_OUT is set when a guarded conversion of a regular or injected channel is outside the programmed thresholds. It is reset after the end of the next guarded conversion that is inside the programmed thresholds. However, the ADC\_AWDy\_OUT signal is also reset at the end of conversion of non-guarded channels, both regular and injected.

#### Workaround

When ADC\_AWDy\_OUT is enabled, it is recommended to use only the ADC channels that are guarded by a watchdog.

If ADC\_AWDy\_OUT is used with ADC channels that are not guarded by a watchdog, take only ADC\_AWDy\_OUT rising edge into account.

### 2.6.7 Injected data stored in the wrong ADC\_JDRx registers

#### Description

When the AHB clock frequency is higher than the ADC clock frequency after the prescaler is applied (ratio > 10), if a JADSTP command is issued to stop the injected conversion (JADSTP bit set to 1 in ADC\_CR register) at the end of an injected conversion, exactly when the data are available, then the injected data are stored in ADC\_JDR1 register instead of ADC\_JDR2/3/4 registers.

#### Workaround

Before setting JADSTP bit, check that the JEOS flag is set in ADC\_ISR register (end of injected channel sequence).

### 2.6.8 ADC slave data may be shifted in Dual regular simultaneous mode

#### Description

In Dual regular simultaneous mode, ADC slave data may be shifted when all the following conditions are met:

- A read operation is performed by one DMA channel,
- OVRMOD = 0 in ADC\_CFGR register (Overrrun mode enabled).

#### Workaround

Apply one of the following measures:

- Set OVRMOD = 1 in ADC\_CFGR. This disables ADC\_DR register FIFO.
- Use two DMA channels to read data: one for slave and one for master.

### 2.6.9 Writing ADCx\_JSQR when JADCSTART and JQDIS are set might lead to incorrect behavior

#### Description

Writing the ADCx\_JSQR register when there is an on-going injected conversion (JADCSTART = 1) might lead to unpredictable ADC behavior if the queues of context are not enabled (JQDIS = 1).

#### Workaround

None.

## 2.6.10 Wrong ADC result if conversion done late after calibration or previous conversion

### Description

The result of an ADC conversion done more than 1 ms later than the previous ADC conversion or ADC calibration might be incorrect.

### Workaround

Perform two consecutive ADC conversions in single, scan or continuous mode. Reject the result of the first conversion and only keep the result of the second.

## 2.6.11 Spurious temperature measurement due to spike noise

### Description

Depending on the MCU activity, internal interference may cause temperature-dependent spike noise on the temperature sensor output to the ADC, resulting in occasional spurious (outlying) temperature measurement.

### Workaround

Perform a series of measurements and process the acquired data samples such as to obtain a mean value not affected by the outlying samples.

For this, it is recommended to use interquartile mean (IQM) algorithm with at least 64 samples. IQM is based on rejecting the quarters (quartiles) of sample population with the lowest and highest values and on computing the mean value only using the remaining (interquartile) samples.

The acquired sample values are first sorted from lowest to highest, then the sample sequence is truncated by removing the lowest and highest sample quartiles.

Example:

**Table 5. Measurement result after IQM post-processing**

Data	Sample												Mean
	1	2	3	4	5	6	7	8	9	10	11	12	
Acquired	17.2	10.92	9.56	2.12	9.82	10.72	10.6	3.5	9.46	9.78	9.5	1.1	8.69
Sorted	1.1	2.12	3.5	9.46	9.5	9.56	9.78	9.82	10.6	10.72	10.92	17.2	8.69
Truncated	-	-	-	9.46	9.5	9.56	9.78	9.82	10.6	-	-	-	9.79

The measurement result after the IQM post-processing in the example is 9.79. For consistent results, use a minimum of 64 samples. It is recommended to optimize the code performing the sort task such as to minimize its processing power requirements.

## 2.6.12 Selected external ADC inputs unduly clamped to $V_{DD}$ when all analog peripherals are disabled

### Description

When all analog peripherals are disabled, the GPIO(s) selected as ADC input(s) are unduly clamped (through a parasitic diode) to  $V_{DD}$  instead to  $V_{DDA}$ . As a consequence, the input voltage is limited to  $V_{DD} + 0.3$  V even if  $V_{DDA}$  is higher than  $V_{DD} + 0.3$  V.

*Note:* The selection of GPIOs as ADC inputs is done with the  $SQy$  and  $JSQy$  bitfields of the  $ADC\_SQRx$  and  $ADC\_JSQR$  registers, respectively.

### Workaround

Apply one of the following measures:

- Use  $V_{DDA}$  lower than  $V_{DD} + 0.3$  V.
- Keep at least one analog peripheral enabled if GPIOs are selected as ADC inputs.



- Deselect GPIOs as ADC inputs (by clearing ADC\_SQRx or/and ADC\_JSQR registers) when no analog peripheral is enabled.

## 2.7 TSC

### 2.7.1 Inhibited acquisition in short transfer phase configuration

#### Description

Some revisions of the reference manual may omit the information that the following configurations of the TSC\_CR register are forbidden:

- The PGPSC[2:0] bitfield set to 000 and the CTPL[3:0] bitfield to 0000 or 0001
- The PGPSC[2:0] bitfield set to 001 and the CTPL[3:0] bitfield to 0000

Failure to respect this restriction leads to an inhibition of the acquisition.  
 This is a documentation inaccuracy issue rather than a product limitation.

#### Workaround

No application workaround is required.

### 2.7.2 TSC signal-to-noise concern under specific conditions

#### Description

$V_{DD}$  equal to or greater than  $V_{DDA}$  may lead (depending on part) to some degradation of the signal-to-noise ratio on the TSC analog I/O group 2.

The lower are the sampling capacitor ( $C_S$ ) and the sensing electrode ( $C_X$ ) capacitances, the worse is the signal-to-noise ratio degradation.

#### Workaround

Apply one of the following measures:

- Maximize  $C_S$  capacitance.
- Use the analog I/O group 2 as active shield.

## 2.8 RNG

### 2.8.1 RNG clock error does not stop random numbers

#### Description

Some revisions of the reference manual may contain the following wrong statements to ignore:

- If the RNG clock frequency is too low, the RNG stops generating random numbers.
- The RNG operates only when the CECS flag is set to 0.

This is a documentation issue rather than a device limitation.

#### Workaround

No application workaround is required or applicable.

## 2.9 AES

### 2.9.1 TAG computation in GCM encryption mode

#### Description

Some revisions of the reference manual may omit the following application guidelines for the device to correctly compute GCM encryption authentication tags when the input data in the last block is inferior to 128 bits.

During GCM encryption payload phase and before inserting a last plaintext block smaller than 128 bits, apply the following steps:

1. Disable the AES peripheral by clearing the EN bit of the AES\_CR register.
2. Change the mode to CTR by writing 010 to the CHMOD[2:0] bitfield of the AES\_CR register.
3. Pad the last block (smaller than 128 bits) with zeros to have a complete block of 128 bits, then write it into AES\_DINR register.
4. Upon encryption completion, read the 128-bit ciphertext from the AES\_DOCTR register and store it as intermediate data.
5. Change again the mode to GCM by writing 011 to the CHMOD[2:0] bitfield of the AES\_CR register.
6. Select Final phase by writing 11 to the GCMPH[1:0] bitfield of the AES\_CR register.
7. In the intermediate data, set to zero the bits corresponding to the padded bits of the last block of payload, then insert the resulting data into AES\_DINR register.
8. Wait for operation completion, and read data on AES\_DOCTR. This data is to be discarded.
9. Apply the normal Final phase as described in the datasheet

This is a documentation issue rather than a product limitation.

#### Workaround

No further application workaround is required, provided that these guidelines are respected.

### 2.9.2 CCM authentication mode not compliant with NIST CMAC

#### Description

Some revisions of the reference manual may omit the information that setting the CHMOD[2:0] bitfield to 100 selects the CCM authentication mode. It is not compliant with NIST CMAC, as defined in Special Publication 800-38B. In order to fully implement the CCM chaining as specified in NIST Special Publication 800-38C, the payload must first be encrypted or decrypted with the AES peripheral set in CTR mode (CHMOD[2:0] = 010), then the message associated data and payload authenticated with the AES peripheral set in CCM mode (CHMOD[2:0] = 100).

This is a documentation issue rather than a product limitation.

#### Workaround

No further application workaround is required, provided that these guidelines are respected.

### 2.9.3 Datatype initial configuration in GCM mode

#### Description

Some revisions of the reference manual may omit the information that GCM generated TAG is not correct if data swapping is not disabled in GCM init phase (GCMPH[1:0] = 00) by setting the DATATYPE[1:0] bitfield of the AES\_CR register to zero.

This is a documentation issue rather than a product limitation.

#### Workaround

No further application workaround is required, provided that these guidelines are respected.

### 2.9.4 Wait until BUSY is low when suspending GCM encryption

#### Description

Some revisions of the reference manual may omit the information that when suspending the GCM encryption of a message, in the payload phase the BUSY flag of the AES\_SR register must be low before saving the AES\_SUSPxR registers in the memory.

This is a documentation issue rather than a product limitation.

## Workaround

No further application workaround is required, provided that these guidelines are respected.

## 2.10 TIM

### 2.10.1 One-pulse mode trigger not detected in master-slave reset + trigger configuration

#### Description

The failure occurs when several timers configured in one-pulse mode are cascaded, and the master timer is configured in combined reset + trigger mode with the MSM bit set:

OPM = 1 in TIMx\_CR1, SMS[3:0] = 1000 and MSM = 1 in TIMx\_SMCR.

The MSM delays the reaction of the master timer to the trigger event, so as to have the slave timers cycle-accurately synchronized.

If the trigger arrives when the counter value is equal to the period value set in the TIMx\_ARR register, the one-pulse mode of the master timer does not work and no pulse is generated on the output.

#### Workaround

None. However, unless a cycle-level synchronization is mandatory, it is advised to keep the MSM bit reset, in which case the problem is not present. The MSM = 0 configuration also allows decreasing the timer latency to external trigger events.

### 2.10.2 Consecutive compare event missed in specific conditions

#### Description

Every match of the counter (CNT) value with the compare register (CCR) value is expected to trigger a compare event. However, if such matches occur in two consecutive counter clock cycles (as consequence of the CCR value change between the two cycles), the second compare event is missed for the following CCR value changes:

- in edge-aligned mode, from ARR to 0:
  - first compare event: CNT = CCR = ARR
  - second (missed) compare event: CNT = CCR = 0
- in center-aligned mode while up-counting, from ARR-1 to ARR (possibly a new ARR value if the period is also changed) at the crest (that is, when TIMx\_RCR = 0):
  - first compare event: CNT = CCR = (ARR-1)
  - second (missed) compare event: CNT = CCR = ARR
- in center-aligned mode while down-counting, from 1 to 0 at the valley (that is, when TIMx\_RCR = 0):
  - first compare event: CNT = CCR = 1
  - second (missed) compare event: CNT = CCR = 0

This typically corresponds to an abrupt change of compare value aiming at creating a timer clock single-cycle-wide pulse in toggle mode.

As a consequence:

- In toggle mode, the output only toggles once per counter period (squared waveform), whereas it is expected to toggle twice within two consecutive counter cycles (and so exhibit a short pulse per counter period).
- In center mode, the compare interrupt flag does not rise and the interrupt is not generated.

*Note:* The timer output operates as expected in modes other than the toggle mode.

#### Workaround

None.

### 2.10.3 Output compare clear not working with external counter reset

#### Description

The output compare clear event (ocref\_clr) is not correctly generated when the timer is configured in the following slave modes: Reset mode, Combined reset + trigger mode, and Combined gated + reset mode.

The PWM output remains inactive during one extra PWM cycle if the following sequence occurs:

1. The output is cleared by the ocref\_clr event.
2. The timer reset occurs before the programmed compare event.

#### Workaround

Apply one of the following measures:

- Use BKIN (or BKIN2 if available) input for clearing the output, selecting the Automatic output enable mode (AOE = 1).
- Mask the timer reset during the PWM ON time to prevent it from occurring before the compare event (for example with a spare timer compare channel open-drain output connected with the reset signal, pulling the timer reset line down).

## 2.11 LPTIM

### 2.11.1 Device may remain stuck in LPTIM interrupt when entering Stop mode

#### Description

This limitation occurs when disabling the low-power timer (LPTIM).

When the user application clears the ENABLE bit in the LPTIM\_CR register within a small time window around one LPTIM interrupt occurrence, then the LPTIM interrupt signal used to wake up the device from Stop mode may be frozen in active state. Consequently, when trying to enter Stop mode, this limitation prevents the device from entering low-power mode and the firmware remains stuck in the LPTIM interrupt routine.

This limitation applies to all Stop modes and to all instances of the LPTIM. Note that the occurrence of this issue is very low.

#### Workaround

In order to disable a low power timer (LPTIMx) peripheral, do not clear its ENABLE bit in its respective LPTIM\_CR register. Instead, reset the whole LPTIMx peripheral via the RCC controller by setting and resetting its respective LPTIMxRST bit in the relevant RCC register.

### 2.11.2 ARRM and CMPM flags are not set when APB clock is slower than kernel clock

#### Description

When LPTIM is configured in one shot mode and APB clock is lower than kernel clock, there is a chance that ARRM and CMPM flags are not set at the end of the counting cycle defined by the repetition value REP[7:0]. This issue can only occur when the repetition counter is configured with an odd repetition value.

#### Workaround

To avoid this issue the following formula must be respected:

$$\{ARR, CMP\} \geq KER\_CLK / (2 * APB\_CLK),$$

where APB\_CLK is the LPTIM APB clock frequency, and KER\_CLK is the LPTIM kernel clock frequency. ARR and CMP are expressed in decimal value.

**Example:** The following example illustrates a configuration where the issue can occur:

- APB clock source (MSI) = 1 MHz , Kernel clock source (HSI) = 16 MHz
- Repetition counter is set with REP[7:0] = 0x3 (odd value)

The above example is subject to issue, unless the user respects:

$$\{CMP, ARR\} \geq 16 \text{ MHz} / (2 * 1 \text{ MHz})$$

→ ARR must be  $\geq 8$  and CMP must be  $\geq 8$

**Note:** *REP set to 0x3 means that effective repetition is REP+1 (= 4) but the user must consider the parity of the value loaded in LPTIM\_RCR register (=3, odd) to assess the risk of issue.*

### 2.11.3 Device may remain stuck in LPTIM interrupt when clearing event flag

#### Description

This limitation occurs when the LPTIM is configured in interrupt mode (at least one interrupt is enabled) and the software clears any flag in LPTIM\_ISR register by writing its corresponding bit in LPTIM\_ICR register. If the interrupt status flag corresponding to a disabled interrupt is cleared simultaneously with a new event detection, the set and clear commands might reach the APB domain at the same time, leading to an asynchronous interrupt signal permanently stuck high.

This issue can occur either during an interrupt subroutine execution (where the flag clearing is usually done), or outside an interrupt subroutine.

Consequently, the firmware remains stuck in the LPTIM interrupt routine, and the device cannot enter Stop mode.

#### Workaround

To avoid this issue, it is strongly advised to follow the recommendations listed below:

- Clear the flag only when its corresponding interrupt is enabled in the interrupt enable register.
- If for specific reasons, it is required to clear some flags that have corresponding interrupt lines disabled in the interrupt enable register, it is recommended to clear them during the current subroutine prior to those which have corresponding interrupt line enabled in the interrupt enable register.
- Flags must not be cleared outside the interrupt subroutine.

**Note:** *The standard clear sequence implemented in the HAL\_LPTIM\_IRQHandler in the STM32Cube is considered as the proper clear sequence.*

### 2.11.4 LPTIM events and PWM output are delayed by one kernel clock cycle

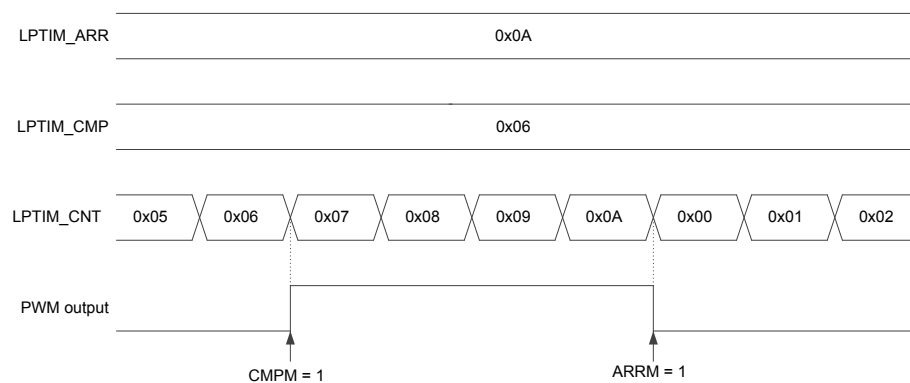
#### Description

The compare match event (CMPM), auto reload match event (ARRM), update event (UE), PWM output level and interrupts are updated with a delay of one kernel clock cycle.

Consequently, it is not possible to generate PWM with a duty cycle of 0% or 100%.

The following waveform gives the example of PWM output mode and the effect of the delay:

**Figure 1. Example of PWM output mode**



#### Workaround

Set the compare value to the desired value minus 1. For instance in order to generate a compare match when LPTIM\_CNT = 0x08, set the compare value to 0x07.

## 2.12 RTC and TAMP

### 2.12.1 RTC\_MISR and TAMP\_MISR can be read by non-privileged accesses when privilege-protected

#### Description

The RTC\_MISR register bits can be read by non-privileged accesses even if their corresponding feature is configured with privilege protection.

The TAMP\_MISR register bits can be read by non-privileged accesses even if the TAMPPRIV bit of the TAMP\_PRIVCR register is set.

#### Workaround

None.

### 2.12.2 RTC configuration changes ignored at specific conditions

#### Description

Writes to some register bits may be ignored if done within a short period after exiting Stop or Standby mode and entering Stop or Standby mode again.

The register is correctly written, but the bit value is not propagated in the RTC kernel if the duration in Run or Sleep mode is too short. This concerns the WUTE (wakeup timer enable) bit, the ALRAE and ALRBE (Alarm A and Alarm B enable) bits, the TAMPxE (Tamper x enable) bits, all bits of RTC\_CALR (the RTC calibration register), and the CWUTF (clear wakeup timer flag) bit.

The following paragraphs describe the failure mechanism for each function.

#### Enabling (or disabling) the wakeup timer:

1. The device is in Stop or Standby mode with the wakeup timer disabled (or enabled).
2. The device wakes up from low-power mode and enables (or disables) the wakeup timer.
3. The device enters Stop or Standby mode.

If the duration of the step 2 (device in Run or Sleep mode) is less than one RTCCLK period, the WUTE bit value change may not be taken into account.

#### Enabling (or disabling) alarm A or alarm B:

1. The device is in Stop or Standby mode with the alarm disabled (or enabled).
2. The device wakes up from low-power mode and enables (or disables) the alarm.
3. The device enters Stop or Standby mode.

If the duration of the step 2 (device in Run or Sleep mode) is less than two RTCCLK periods, the ALRAE or ALRBE bit value change may not be taken into account.

#### Enabling a tamper:

1. The device is in Stop or Standby mode with all tampers disabled.
2. The device wakes up from low-power mode and enables at least one tamper.
3. The device enters Stop or Standby mode.

If the duration of the step 2 (device in Run or Sleep mode) is less than two RTCCLK periods, the tamper may remain disabled.

#### Calibration register value change:

1. The device is in Stop or Standby mode with the RECALPF bit cleared.
2. The device wakes up from low-power mode and changes the RTC\_CALR value.
3. The device enters Stop or Standby mode.

If the duration of the step 2 (device in Run or Sleep mode) is less than two RTCCLK periods, the RTC\_CALR new value may not be taken into account.

#### Clearing wakeup timer flag:

1. The device is in Stop or Standby mode and WUTF is set.
2. The device wakes up from low-power mode and clears WUTF by setting the CWUTF bit of the RTC\_SCR register.
3. The device enters Stop or Standby mode.

If the duration of the step 2 (device in Run or Sleep mode) is less than two RTCCLK periods, the WUTF bit may be stuck low and cannot be set when the wakeup timer reaches zero again.

*Note:* The same failures occur if the DBP (disable backup domain write protection) bit of the PWR register is set before changing the RTC configuration, and is cleared soon after.

#### Workaround

Always keep the DBP bit set. When the device wakes up (step 2): clear the RSF flag of the RTC\_ICSR register and wait until it is set again before entering Stop or Standby mode. In case the BYPSHAD bit of the RTC\_CR register is set, clear it before the RSF flag is set. The BYPSHAD bit can then be set again by software.

### 2.12.3 Calibration formula changes when LPCAL is set

#### Description

When the LPCAL bit is set, the frequency calibration formula unduly becomes:

$$f_{CAL} = f_{RTCCLK} \times \left[ \frac{(2^{20} - 1)}{(2^{20} - 1 + CALM - CALP \times 512)} \right]$$

instead of:

$$f_{CAL} = f_{RTCCLK} \times \left[ \frac{2^{20}}{(2^{20} + CALM - CALP \times 512)} \right]$$

As a consequence, the RTC frequency in the application that keeps the LPCAL bit set (to reduce power consumption) is slightly different from the frequency measured with the LPCAL bit cleared.

#### Workaround

In an application keeping the LPCAL bit set, apply a compensation reflecting the difference of the frequency formulas.

*Note:* LPCAL remains set when a new calibration value is applied. Checking the calibration result is only for validation or test purposes.

### 2.12.4 Calendar initialization may fail in case of consecutive INIT mode entry

#### Description

If the INIT bit of the RTC\_ICSR register is set between one and two RTCCLK cycles after being cleared, the INITF flag is set immediately instead of waiting for synchronization delay (which should be between one and two RTCCLK cycles), and the initialization of registers may fail. Depending on the INIT bit clearing and setting instants versus the RTCCLK edges, it can happen that, after being immediately set, the INITF flag is cleared during one RTCCLK period then set again. As writes to calendar registers are ignored when INITF is low, a write occurring during this critical period might result in the corruption of one or more calendar registers.

#### Workaround

After exiting the initialization mode, clear the BYPSHAD bit (if set) then wait for RSF to rise, before entering the initialization mode again.

*Note:* It is recommended to write all registers in a single initialization session to avoid accumulating synchronization delays.

### 2.12.5 Alarm flag may be repeatedly set when the core is stopped in debug

#### Description

When the core is stopped in debug mode, the clock is supplied to subsecond RTC alarm downcounter even when the device is configured to stop the RTC in debug.

As a consequence, when the subsecond counter is used for alarm condition (the MASKSS[3:0] bitfield of the RTC\_ALRMASR and/or RTC\_ALRMBSSR register set to a non-zero value) and the alarm condition is met just before entering a breakpoint or printf, the ALRAF and/or ALRBF flag of the RTC\_SR register is repeatedly set by hardware during the breakpoint or printf, which makes any attempt to clear the flag(s) ineffective.

**Workaround**

None.

**2.12.6 A tamper event fails to trigger timestamp or timestamp overflow events during a few cycles after clearing TSF**

**Description**

With the timestamp on tamper event enabled (TAMPTS bit of the RTC\_CR register set), a tamper event is ignored if it occurs:

- within four APB clock cycles after setting the CTSF bit of the RTC\_SCR register to clear the TSF flag, while the TSF flag is not yet effectively cleared (it fails to set the TSOVF flag)
- within two ck\_apre cycles after setting the CTSF bit of the RTC\_SCR register to clear the TSF flag, when the TSF flag is effectively cleared (it fails to set the TSF flag and timestamp the calendar registers)

**Workaround**

None.

**2.12.7 Spurious RTC alarm EXTI line event following RTC WUT interrupt**

**Description**

As expected, WUT interrupt (if enabled in the RTC) generates an event on the EXTI line 20 of the event controller. However, it also causes a spurious event on the EXTI line 18 that should only respond to alarm interrupts and not to WUT interrupts.

**Workaround**

Upon EXTI 18 event, identify the source of interrupt by reading WUT and alarm interrupt flags.

**2.12.8 RTC\_REFIN and RTC\_OUT on PB2 not operating in Stop 2 mode**

**Description**

In Stop 2 low-power mode, the RTC\_REFIN function does not operate and the RTC\_OUT function does not operate if mapped on the PB2 pin.

**Workaround**

Apply one of the following measures:

- Use Stop 1 mode instead of Stop 2. This ensures the operation of both functions.
- Map RTC\_OUT to the PC13 pin. This ensures the operation of the RTC\_OUT function in either low-power mode. However, it has no effect to the RTC\_REFIN function.

**2.12.9 Setting GPIO properties of PC13 used as RTC\_ALARM open-drain output**

**Description**

Some reference manual revisions may omit the information that the PC13 GPIO must be set as input when the RTC\_OR register configures PC13 as open-drain output of the RTC\_ALARM signal.

*Note:* Enabling the internal pull-up function through the PC13 GPIO settings allows sparing an external pull-up resistor. This is a documentation issue rather than a product limitation.

**Workaround**

No application workaround is required provided that the described GPIO setting is respected.



### 2.12.10 V<sub>BAT</sub> tamper limitation

#### Description

Tamper functionality in V<sub>BAT</sub> mode may be compromised with false tamper events when a pin that contains an alternate analog configuration is used. Only GPIOs with two power supplies (V<sub>DD</sub> and V<sub>DDA</sub>) are affected by this issue therefore pins with alternate analog configuration only are affected; pins with no analog functionality are not having this problem.

#### Workaround

Short V<sub>DD</sub> fall time to zero causes the V<sub>BAT</sub> to be engaged rapidly and correctly. Avoid lingering V<sub>DD</sub> below 500 mV.

### 2.12.11 RTC\_OUT redirection to PB2 does not release PC13

#### Description

When the RTC\_OUT\_RMP of RTC\_CR is used to redirect RTC output to PB2, PC13 is not freed to be used as GPIO, or RTC input. However, it can still be used as RTC\_ALARM output as described in the reference manual.

#### Workaround

None. Use different GPIO mapping.

## 2.13 I2C

### 2.13.1 10-bit master mode: new transfer cannot be launched if first part of the address is not acknowledged by the slave

#### Description

An I<sup>2</sup>C-bus master generates STOP condition upon non-acknowledge of I<sup>2</sup>C address that it sends. This applies to 7-bit address as well as to each byte of 10-bit address.

When the MCU set as I<sup>2</sup>C-bus master transmits a 10-bit address of which the first byte (5-bit header + 2 MSBs of the address + direction bit) is not acknowledged, the MCU duly generates STOP condition but it then cannot start any new I<sup>2</sup>C-bus transfer. In this spurious state, the NACKF flag of the I2C\_ISR register and the START bit of the I2C\_CR2 register are both set, while the START bit should normally be cleared.

#### Workaround

In 10-bit-address master mode, if both NACKF flag and START bit get simultaneously set, proceed as follows:

1. Wait for the STOP condition detection (STOPF = 1 in I2C\_ISR register).
2. Disable the I2C peripheral.
3. Wait for a minimum of three APB cycles.
4. Enable the I2C peripheral again.

### 2.13.2 Wrong behavior in Stop mode when wake-up from Stop mode is disabled in I2C

#### Description

The correct use of the I2C peripheral, if the wake-up from Stop mode by I2C is disabled (WUPEN = 0), is to disable it (PE = 0) before entering Stop mode, and re-enable it when back in Run mode.

Some reference manual revisions may omit this information.

Failure to respect the above while the MCU operating as slave or as master in multi-master topology enters Stop mode during a transfer ongoing on the I<sup>2</sup>C-bus may lead to the following:

1. BUSY flag is wrongly set when the MCU exits Stop mode. This prevents from initiating a transfer in master mode, as the START condition cannot be sent when BUSY is set.
2. If clock stretching is enabled (NOSTRETCH = 0), the SCL line is pulled low by I2C and the transfer stalled as long as the MCU remains in Stop mode.  
The occurrence of such condition depends on the timing configuration, peripheral clock frequency, and I<sup>2</sup>C-bus frequency.

This is a description inaccuracy issue rather than a product limitation.

#### Workaround

No application workaround is required.

### 2.13.3 Wrong data sampling when data setup time ( $t_{SU, DAT}$ ) is shorter than one I2C kernel clock period

#### Description

The I<sup>2</sup>C-bus specification and user manual specify a minimum data setup time ( $t_{SU, DAT}$ ) as:

- 250 ns in Standard mode
- 100 ns in Fast mode
- 50 ns in Fast mode Plus

The device does not correctly sample the I<sup>2</sup>C-bus SDA line when  $t_{SU, DAT}$  is smaller than one I2C kernel clock (I<sup>2</sup>C-bus peripheral clock) period: the previous SDA value is sampled instead of the current one. This can result in a wrong receipt of slave address, data byte, or acknowledge bit.

#### Workaround

Increase the I2C kernel clock frequency to get I2C kernel clock period within the transmitter minimum data setup time. Alternatively, increase transmitter's minimum data setup time. If the transmitter setup time minimum value corresponds to the minimum value provided in the I<sup>2</sup>C-bus standard, the minimum I2CCLK frequencies are as follows:

- In Standard mode, if the transmitter minimum setup time is 250 ns, the I2CCLK frequency must be at least 4 MHz.
- In Fast mode, if the transmitter minimum setup time is 100 ns, the I2CCLK frequency must be at least 10 MHz.
- In Fast-mode Plus, if the transmitter minimum setup time is 50 ns, the I2CCLK frequency must be at least 20 MHz.

### 2.13.4 Spurious bus error detection in master mode

#### Description

In master mode, a bus error can be detected spuriously, with the consequence of setting the BERR flag of the I2C\_SR register and generating bus error interrupt if such interrupt is enabled. Detection of bus error has no effect on the I<sup>2</sup>C-bus transfer in master mode and any such transfer continues normally.

#### Workaround

If a bus error interrupt is generated in master mode, the BERR flag must be cleared by software. No other action is required and the ongoing transfer can be handled normally.

### 2.13.5 Last-received byte loss in reload mode

#### Description

If in master receiver mode or slave receive mode with SBC = 1 the following conditions are all met:

- I<sup>2</sup>C-bus stretching is enabled (NOSTRETCH = 0)
- RELOAD bit of the I2C\_CR2 register is set
- NBYTES bitfield of the I2C\_CR2 register is set to N greater than 1
- byte N is received on the I<sup>2</sup>C-bus, raising the TCR flag
- N - 1 byte is not yet read out from the data register at the instant TCR is raised,

then the SCL line is pulled low (I<sup>2</sup>C-bus clock stretching) and the transfer of the byte N from the shift register to the data register inhibited until the byte N-1 is read and NBYTES bitfield reloaded with a new value, the latter of which also clears the TCR flag. As a consequence, the software cannot get the byte N and use its content before setting the new value into the NBYTES field.

For I2C instances with independent clock, the last-received data is definitively lost (never transferred from the shift register to the data register) if the data N - 1 is read within four APB clock cycles preceding the receipt of the last data bit of byte N and thus the TCR flag raising. Refer to the product reference manual or datasheet for the I2C implementation table.

#### Workaround

- In master mode or in slave mode with SBC = 1, use the reload mode with NBYTES = 1.
- In master receiver mode, if the number of bytes to transfer is greater than 255, do not use the reload mode. Instead, split the transfer into sections not exceeding 255 bytes and separate them with repeated START conditions.
- Make sure, for example through the use of DMA, that the byte N - 1 is always read before the TCR flag is raised. Specifically for I2C instances with independent clock, make sure that it is always read earlier than four APB clock cycles before the receipt of the last data bit of byte N and thus the TCR flag raising.

The last workaround in the list must be evaluated carefully for each application as the timing depends on factors such as the bus speed, interrupt management, software processing latencies, and DMA channel priority.

### 2.13.6 Spurious master transfer upon own slave address match

#### Description

When the device is configured to operate at the same time as master and slave (in a multi-master I<sup>2</sup>C-bus application), a spurious master transfer may occur under the following condition:

- Another master on the bus is in process of sending the slave address of the device (the bus is busy).
- The device initiates a master transfer by bit set before the slave address match event (the ADDR flag set in the I2C\_ISR register) occurs.
- After the ADDR flag is set:
  - the device does not write I2C\_CR2 before clearing the ADDR flag, or
  - the device writes I2C\_CR2 earlier than three I2C kernel clock cycles before clearing the ADDR flag

In these circumstances, even though the START bit is automatically cleared by the circuitry handling the ADDR flag, the device spuriously proceeds to the master transfer as soon as the bus becomes free. The transfer configuration depends on the content of the I2C\_CR2 register when the master transfer starts. Moreover, if the I2C\_CR2 is written less than three kernel clocks before the ADDR flag is cleared, the I2C peripheral may fall into an unpredictable state.

#### Workaround

Upon the address match event (ADDR flag set), apply the following sequence.

Normal mode (SBC = 0):

1. Set the ADDRCONF bit.
2. Before Stop condition occurs on the bus, write I2C\_CR2 with the START bit low.

Slave byte control mode (SBC = 1):

1. Write I2C\_CR2 with the slave transfer configuration and the START bit low.
2. Wait for longer than three I2C kernel clock cycles.
3. Set the ADDRCF bit.
4. Before Stop condition occurs on the bus, write I2C\_CR2 again with its current value.

The time for the software application to write the I2C\_CR2 register before the Stop condition is limited, as the clock stretching (if enabled), is aborted when clearing the ADDR flag.

Polling the BUSY flag before requesting the master transfer is not a reliable workaround as the bus may become busy between the BUSY flag check and the write into the I2C\_CR2 register with the START bit set.

### 2.13.7 START bit is cleared upon setting ADDRCF, not upon address match

#### Description

Some reference manual revisions may state that the START bit of the I2C\_CR2 register is cleared upon slave address match event.

Instead, the START bit is cleared upon setting, by software, the ADDRCF bit of the I2C\_ICR register, which does not guarantee the abort of master transfer request when the device is being addressed as slave. This product limitation and its workaround are the subject of a separate erratum.

#### Workaround

No application workaround is required for this description inaccuracy issue.

### 2.13.8 OVR flag not set in underrun condition

#### Description

In slave transmission with clock stretching disabled (NOSTRETCH = 1 in the I2C\_CR1 register), an underrun condition occurs if the current byte transmission is completed on the I<sup>2</sup>C bus, and the next data is not yet written in the TXDATA[7:0] bitfield. In this condition, the device is expected to set the OVR flag of the I2C\_ISR register and send 0xFF on the bus.

However, if the I2C\_TXDR is written within the interval between two I2C kernel clock cycles before and three APB clock cycles after the start of the next data transmission, the OVR flag is not set, although the transmitted value is 0xFF.

#### Workaround

None.

### 2.13.9 Transmission stalled after first byte transfer

#### Description

When the first byte to transmit is not prepared in the TXDATA register, two bytes are required successively, through TXIS status flag setting or through a DMA request. If the first of the two bytes is written in the I2C\_TXDR register in less than two I2C kernel clock cycles after the TXIS/DMA request, and the ratio between APB clock and I2C kernel clock frequencies is between 1.5 and 3, the second byte written in the I2C\_TXDR is not internally detected. This causes a state in which the I2C peripheral is stalled in master mode or in slave mode, with clock stretching enabled (NOSTRETCH = 0). This state can only be released by disabling the peripheral (PE = 0) or by resetting it.

#### Workaround

Apply one of the following measures:

- Write the first data in I2C\_TXDR before the transmission starts.
- Set the APB clock frequency so that its ratio with respect to the I2C kernel clock frequency is lower than 1.5 or higher than 3.

### 2.13.10 SDA held low upon SMBus timeout expiry in slave mode

#### Description

For the slave mode, the SMBus specification defines  $t_{\text{TIMEOUT}}$  (detect clock low timeout) and  $t_{\text{LOW:SEXT}}$  (cumulative clock low extend time) timeouts. When one of them expires while the I2C peripheral in slave mode drives SDA low to acknowledge either its address or a data transmitted by the master, the device is expected to report such an expiry and release the SDA line.

However, although the device duly reports the timeout expiry, it fails to release SDA. This stalls the I<sup>2</sup>C bus and prevents the master from generating RESTART or STOP condition.

#### Workaround

When a timeout is reported in slave mode (TIMEOUT bit of the I2C\_ISR register is set), apply this sequence:

1. Wait until the frame is expected to end.
2. Read the STOPF bit of the I2C\_ISR register. If it is low, reset the I2C kernel by clearing the PE bit of the I2C\_CR1 register.
3. Wait for at least three APB clock cycles before enabling again the I2C peripheral.

## 2.14 USART

### 2.14.1 RTS is active while RE = 0 or UE = 0

#### Description

The RTS line is driven low as soon as RTSE bit is set, even if the USART is disabled (UE = 0) or the receiver is disabled (RE = 0), that is, not ready to receive data.

#### Workaround

Upon setting the UE and RE bits, configure the I/O used for RTS into alternate function.

### 2.14.2 Receiver timeout counter wrong start in two-stop-bit configuration

#### Description

In two-stop-bit configuration, the receiver timeout counter starts counting from the end of the second stop bit of the last character instead of starting from the end of the first stop bit.

#### Workaround

Subtract one bit duration from the value in the RTO bitfield of the USARTx\_RTOR register.

### 2.14.3 Data corruption due to noisy receive line

#### Description

In all modes, except synchronous slave mode, the received data may be corrupted if a glitch to zero shorter than the half-bit occurs on the receive line within the second half of the stop bit.

#### Workaround

Apply one of the following measures:

- Either use a noiseless receive line, or
- add a filter to remove the glitches if the receive line is noisy.

#### 2.14.4 Received data may be corrupted upon clearing the ABREN bit

##### Description

The USART receiver may miss data or receive corrupted data when the auto baud rate feature is disabled by software (ABREN bit cleared in the USART\_CR2 register) after an auto baud rate detection, while a reception is ongoing.

##### Workaround

Do not clear the ABREN bit.

#### 2.14.5 Noise error flag set while ONEBIT is set

##### Description

When the ONEBIT bit is set in the USART\_CR3 register (one sample bit method is used), the noise error (NE) flag must remain cleared. Instead, this flag is set upon noise detection on the START bit.

##### Workaround

None.

*Note: Having noise on the START bit is contradictory with the fact that the one sample bit method is used in a noise free environment.*

### 2.15 LPUART

#### 2.15.1 RTS is active while RE = 0 or UE = 0

##### Description

The RTS line is driven low as soon as RTSE bit is set, even if the LPUART is disabled (UE = 0) or the receiver is disabled (RE = 0), that is, not ready to receive data.

##### Workaround

Upon setting the UE and RE bits, configure the I/O used for RTS into alternate function.

#### 2.15.2 Possible LPUART transmitter issue when using low BRR[15:0] value

##### Description

The LPUART transmitter bit length sequence is not reset between consecutive bytes, which could result in a jitter that cannot be handled by the receiver device. As a result, depending on the receiver device bit sampling sequence, a desynchronization between the LPUART transmitter and the receiver device may occur resulting in data corruption on the receiver side.

This happens when the ratio between the LPUART kernel clock and the baud rate programmed in the LPUART\_BRR register (BRR[15:0]) is not an integer, and is in the three to four range. A typical example is when the 32.768 kHz clock is used as kernel clock and the baud rate is equal to 9600 baud, resulting in a ratio of 3.41.

##### Workaround

Apply one of the following measures:

- On the transmitter side, increase the ratio between the LPUART kernel clock and the baud rate. To do so:
  - Increase the LPUART kernel clock frequency, or
  - Decrease the baud rate.
- On the receiver side, generate the baud rate by using a higher frequency and applying oversampling techniques if supported.

## 2.16 SPI

### 2.16.1 BSY bit may stay high when SPI is disabled

#### Description

The BSY flag may remain high upon disabling the SPI while operating in:

- master transmit mode and the TXE flag is low (data register full).
- master receive-only mode (simplex receive or half-duplex bidirectional receive phase) and an SCK strobing edge has not occurred since the transition of the RXNE flag from low to high.
- slave mode and NSS signal is removed during the communication.

#### Workaround

When the SPI operates in:

- master transmit mode, disable the SPI when TXE = 1 and BSY = 0.
- master receive-only mode, ignore the BSY flag.
- slave mode, do not remove the NSS signal during the communication.

### 2.16.2 BSY bit may stay high at the end of data transfer in slave mode

#### Description

BSY flag may sporadically remain high at the end of a data transfer in slave mode. This occurs upon coincidence of internal CPU clock and external SCK clock provided by master.

In such an event, if the software only relies on BSY flag to detect the end of SPI slave data transaction (for example to enter low-power mode or to change data line direction in half-duplex bidirectional mode), the detection fails.

As a conclusion, the BSY flag is unreliable for detecting the end of data transactions.

#### Workaround

Depending on SPI operating mode, use the following means for detecting the end of transaction:

- When NSS hardware management is applied and NSS signal is provided by master, use NSS flag.
- In SPI receiving mode, use the corresponding RXNE event flag.
- In SPI transmit-only mode, use the BSY flag in conjunction with a timeout expiry event. Set the timeout such as to exceed the expected duration of the last data frame and start it upon TXE event that occurs with the second bit of the last data frame. The end of the transaction corresponds to either the BSY flag becoming low or the timeout expiry, whichever happens first.

Prefer one of the first two measures to the third as they are simpler and less constraining.

Alternatively, apply the following sequence to ensure reliable operation of the BSY flag in SPI transmit mode:

1. Write last data to data register.
2. Poll the TXE flag until it becomes high, which occurs with the second bit of the data frame transfer.
3. Disable SPI by clearing the SPE bit mandatorily before the end of the frame transfer.
4. Poll the BSY bit until it becomes low, which signals the end of transfer.

**Note:** *The alternative method can only be used with relatively fast CPU speeds versus relatively slow SPI clocks or/and long last data frames. The faster is the software execution, the shorter can be the duration of the last data frame.*

### 2.16.3 SPI master communication failure at high SYSCLK frequency within the specified voltage range

#### Description

The SPI peripheral configured as master may spuriously generate an extra clock pulse when:

- the CPHA bit of the SPIx\_CR1 register is set, and
- the BR[2:0] bitfield of the SPIx\_CR1 register is at 001 ( $f_{PCLK}$  divided by four), and
- the SPI clock is about to be suspended or stopped (which occurs at the end of a data frame), and
- the SYSCLK frequency exceeds the values as per the following table

This leads to a de-synchronization of the SPI data flow.

**Table 6. Maximum  $f_{SYSCLK}$  for safe SPI operation**

SPI instance	$f_{SYSCLK(max)}$ [MHz]	
	Range 1	Range 2
SPI1	66.7	>26 (OK)
SPI2	54.0	23.5

#### Workaround

Depending on the application constraints, apply one of the following measures:

- Set the SYSCLK frequency to within the limits in the table.
- Choose a combination of AHB and APB prescaler settings that allows setting the BR[2:0] bitfield to a value other than 001 ( $f_{PCLK}/4$ ).
- Use another SPI instance on another APB if this can avoid setting BR[2:0] to 001. If the other instance is available on the same pins through the GPIO alternate function, the same application hardware can be used.

## 2.17 USB

### 2.17.1 Possible packet memory overrun/underrun at low APB frequency

#### Description

Some data sheet and/or reference manual revisions may omit the information that 10 MHz minimum APB clock frequency is required to avoid USB data overrun/underrun issues.

Operating the USB peripheral with lower APB clock frequency may lead to:

- Overrun for *out* transactions - the USB peripheral fails to store the received data into the PBM before the next byte is received on the USB (PBM overrun). The USB cell detects an internal error condition, discards the last received byte, stops writing into the PBM, sends no acknowledge (forcing the host to retry the transaction), and informs the application by setting the PMAOVR flag/interrupt.
- Underrun for *in* transactions - the USB peripheral fails to read from the PBM the next byte to transmit before the transmission of the previous one is completed on the USB. The USB cell detects an internal error condition, stops reading from PBM, generates a bit stuffing error on the USB (forcing the host to retry the transaction), and informs the application by setting the PMAOVR flag/interrupt.

This is a documentation issue rather than a device limitation.

#### Workaround

No application workaround is required if the minimum APB clock frequency of 10 MHz is respected.



### 2.17.2 ESOF interrupt timing desynchronized after resume signaling

#### Description

Upon signaling resume, the device is expected to allow full 3 ms of time to the host or hub for sending the initial SOF (start of frame) packet, without triggering SUSP interrupt. However, the device only allows two full milliseconds and unduly triggers SUSP interrupt if it receives the initial packet within the third millisecond.

#### Workaround

When the device initiates resume (remote wake-up), mask the SUSP interrupt by setting the SUSPM bit for 3 ms, then unmask it by clearing SUSPM.

### 2.17.3 Incorrect CRC16 in the memory buffer

#### Description

Memory buffer locations are written starting from the address contained in the ADDRn\_RX for a number of bytes corresponding to the received data packet length, CRC16 inclusive (that is, data payload length plus two bytes), or up to the last allocated memory location defined by BL\_SIZE and NUM\_BLOCK, whichever comes first. In the former case, the CRC16 checksum is written wrongly, with its least significant byte going to both memory buffer byte locations expected to receive the least and the most significant bytes of the checksum.

Although the checksum written in the memory buffer is wrong, the underlying CRC checking mechanism in the USB peripheral is fully functional.

#### Workaround

Ignore the CRC16 data in the memory buffer.

### 2.17.4 Buffer description table update completes after CTR interrupt triggers

#### Description

During OUT transfers, the correct transfer interrupt (CTR) is triggered a little before the last USB SRAM accesses have completed. If the software responds quickly to the interrupt, the full buffer contents may not be correct.

#### Workaround

Software should ensure that a small delay is included before accessing the SRAM contents. This delay should be 800 ns in Full Speed mode and 6.4  $\mu$ s in Low Speed mode.

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## Revision history

**Table 7. Document revision history**

Date	Version	Changes
17-Oct-2018	1	Initial release.
10-Jun-2021	2	<p>Added errata:</p> <ul style="list-style-type: none"> <li>• Current injection from <math>V_{DD}</math> to <math>V_{DDA}</math> through analog switch voltage booster</li> <li>• FLASH_ECCR corrupted upon reset or power-down occurring during flash memory program or erase operation</li> <li>• HSE oscillator long startup at low voltage</li> <li>• Selected external ADC inputs unduly clamped to <math>V_{DD}</math> when all analog peripherals are disabled</li> <li>• TSC signal-to-noise concern under specific conditions</li> <li>• Device may remain stuck in LPTIM interrupt when clearing event flag</li> <li>•</li> <li>•</li> <li>• RTC_MISR and TAMP_MISR can be read by non-privileged accesses when privilege-protected</li> <li>• RTC configuration changes ignored at specific conditions</li> <li>• Calibration formula changes when LPCAL is set</li> <li>• Calendar initialization may fail in case of consecutive INIT mode entry</li> <li>• Setting GPIO properties of PC13 used as RTC_ALARM open-drain output</li> <li>• <i>CRC error in SPI slave mode if internal NSS changes before CRC</i></li> <li>• SPI master communication failure at high SYSCLK frequency within the specified voltage range</li> </ul> <p>Modified errata:</p> <ul style="list-style-type: none"> <li>• VDIV or VSQRT instructions might not complete correctly when very short ISRs are used</li> <li>• Internal voltage reference corrupted upon Stop mode entry with temperature sensing enabled</li> <li>• Full JTAG configuration without NJTRST pin cannot be used</li> <li>• Inhibited acquisition in short transfer phase configuration</li> <li>• Device may remain stuck in LPTIM interrupt when entering Stop mode</li> <li>• Wrong behavior in Stop mode when wake-up from Stop mode is disabled in I2C</li> <li>• Wrong data sampling when data setup time (<math>t_{SU;DAT}</math>) is shorter than one I2C kernel clock period</li> <li>• Last-received byte loss in reload mode</li> </ul> <p>Removed erratum <i>First double-word of Flash memory corrupted upon reset or power down while programming</i> (superseded with the erratum FLASH_ECCR corrupted upon reset or power-down occurring during flash memory program or erase operation).</p>
19-May-2022	3	<p>Added erratum SRAM write error.</p> <p>Added Section Important security notice.</p>
23-Feb-2023	4	<p>Added erratum LSE crystal oscillator may be disturbed by transitions on PC13.</p> <p>Modified erratum:</p> <ul style="list-style-type: none"> <li>• SRAM write error</li> <li>• SPI master communication failure at high SYSCLK frequency within the specified voltage range - now applicable to high <math>f_{SYSCLK}</math> condition not only to the specific case of high <math>f_{PCLK} = f_{SYSCLK}</math>. Re-qualified to A and a workaround described.</li> </ul>
23-Oct-2023	5	<p>Added errata:</p> <ul style="list-style-type: none"> <li>• Section 2.2.11: Corrupted content of the backup domain due to a missed power-on reset after this domain supply voltage drop</li> <li>• Section 2.12.10: <math>V_{BAT}</math> tamper limitation</li> </ul>

Date	Version	Changes
		Modified erratum: Section 2.2.9: LSE crystal oscillator may be disturbed by transitions on PC13
22-Nov-2024	6	Added part numbers of STM32L422xB. Added errata: <ul style="list-style-type: none"> <li>• <b>System:</b> Debugging Sleep/Stop mode with WFE/WFI entry</li> <li>• <b>DMA:</b> DMA disable failure and error flag omission upon simultaneous transfer error and global flag clear</li> <li>• Byte and half-word accesses not supported</li> <li>• <b>QUADSPI:</b> Memory-mapped read operations may fail when timeout counter is enabled</li> <li>• Memory-mapped access in indirect mode clearing QUADSPI_AR register</li> <li>• Transmission error flag (TEF) in memory space access with ADMODE = 0</li> <li>• <b>ADC:</b> <ul style="list-style-type: none"> <li>• Writing ADC_JSQR when JADCSTART and JQDIS are set may lead to incorrect behavior</li> <li>• ADEN bit cannot be set immediately after the ADC calibration is done</li> <li>• New context conversion initiated without waiting for trigger when writing new context in ADC_JSQR with JQDIS = 0 and JQM = 0</li> <li>• Two consecutive context conversions fail when writing new context in ADC_JSQR just after previous context completion with JQDIS = 0 and JQM = 0</li> <li>• Unexpected regular conversion when two consecutive injected conversions are performed in Dual interleaved mode</li> <li>• ADC_AWDy_OUT reset by non-guarded channels</li> <li>• Injected data stored in the wrong ADC_JDRx registers</li> <li>• ADC slave data may be shifted in Dual regular simultaneous mode</li> </ul> </li> <li>• <b>RNG:</b> RNG clock error does not stop random numbers</li> <li>• <b>AES:</b> TAG computation in GCM encryption mode</li> <li>• CCM authentication mode not compliant with NIST CMAC</li> <li>• Datatype initial configuration in GCM mode</li> <li>• Wait until BUSY is low when suspending GCM encryption</li> <li>• <b>TIM:</b> One-pulse mode trigger not detected in master-slave reset + trigger configuration</li> <li>• Consecutive compare event missed in specific conditions</li> <li>• Output compare clear not working with external counter reset</li> <li>• <b>LPTIM:</b> ARRM and CMPM flags are not set when APB clock is slower than kernel clock</li> <li>• LPTIM events and PWM output are delayed by one kernel clock cycle</li> <li>• <b>RTC and TAMP:</b> Alarm flag may be repeatedly set when the core is stopped in debug</li> <li>• A tamper event fails to trigger timestamp or timestamp overflow events during a few cycles after clearing TSF</li> <li>• V<sub>BAT</sub> tamper limitation (moved from System)</li> <li>• RTC_OUT redirection to PB2 does not release PC13 (moved from System)</li> <li>• <b>I2C:</b> START bit is cleared upon setting ADDRCONF, not upon address match</li> <li>• OVR flag not set in underrun condition</li> <li>• Transmission stalled after first byte transfer</li> <li>• SDA held low upon SMBus timeout expiry in slave mode</li> <li>• <b>USART:</b> Receiver timeout counter wrong start in two-stop-bit configuration</li> <li>• Data corruption due to noisy receive line</li> <li>• Received data may be corrupted upon clearing the ABREN bit</li> <li>• Noise error flag set while ONEBIT is set</li> <li>• <b>LPUART:</b> RTS is active while RE = 0 or UE = 0</li> <li>• Possible LPUART transmitter issue when using low BRR[15:0] value</li> <li>• <b>SPI:</b> BSY bit may stay high when SPI is disabled</li> <li>• <b>USB:</b> Possible packet memory overrun/underrun at low APB frequency</li> <li>• ESOF interrupt timing desynchronized after resume signaling</li> </ul>

Date	Version	Changes
		<ul style="list-style-type: none"> <li>• Incorrect CRC16 in the memory buffer</li> <li>• Buffer description table update completes after CTR interrupt triggers</li> </ul> <p>Modified errata:</p> <ul style="list-style-type: none"> <li>• Corrupted content of the backup domain due to a missed power-on reset after this domain supply voltage drop (added missing second workaround bullet point)</li> </ul> <p>Removed errata:</p> <ul style="list-style-type: none"> <li>• <b>RTC and TAMP:</b> <i>Internal tamper flags not output on RTC_OUT1 and RTC_OUT2</i></li> <li>• <i>Notification of illegal access to secured registers is not reliable</i></li> <li>• <b>SPI:</b> <i>Wrong CRC in full-duplex mode handled by DMA with imbalanced setting of data counters</i></li> <li>• <i>CRC error in SPI slave mode if internal NSS changes before CRC</i></li> </ul>

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