ST25R3916 ST25R3917
ST25R3918 ST25R3920

Errata sheet

ST25R3916, ST25R3917, ST25R3918, and ST25R3920 device limitations

Silicon identification

This errata sheet applies to the ST25R3916, ST25R3917, ST25R3918, and ST25R3920 products.

Identification by SPI or I²C

The part can be identified by reading the product revision code in the IC identity register at address 3Fh.

The limitations described in this document apply to product revision 3.1, which corresponds to an IC identity register readout of 2Ah.

1 Summary of silicon limitations

The following table gives a quick reference to all documented limitations.

Legend of Table 1:

- A = limitation present, workaround available
- N = limitation present, no workaround available
- P = limitation present, partial workaround available
- '-' limitation absent or fixed

Table 1. Summary of silicon limitations

Links to silicon limitations		Workaround			
		ST25R3916 revision 3.1	ST25R3917 revision 3.1	ST25R3918 revision 3.1	ST25R3920 revision 3.1
Section 1.1: System limitations	Section 1.1.1: Direct command, change AM modulation state, does not change resistive modulation state (applicable when bit res_am = 1)	N	N	N	N
Section 1.2: Interrupt and associated reporting limitations	Section 1.2.1: Missing I_rxe interrupt	A	A	A	A
	Section 1.2.2: PPON2 timer	A	A	N	A
	Section 1.2.3: Serial peripheral interface (SPI)	A	A	A	A

1.1 System limitations

1.1.1 Direct command, change AM modulation state, does not change resistive modulation state (applicable when bit res_am = 1)

Description

The device allows amplitude modulation (AM) using the concepts of regulation and resistive-based modulation. The direct command, change AM modulation state, switches the AM modulation state from unmodulated to modulated, and vice versa. This command is not needed during normal operation but can be used, for instance, to measure the AM modulation index. The command only affects the regulator state and not the resistive modulation state.

Workaround

None

1.2 Interrupt and associated reporting limitations

1.2.1 Missing I_rxe interrupt

Description

Rarely, on corrupted frames I_rxs gets signaled but I_rxe is not signaled.

Workaround

Treat all reception error interrupts as I_rxe and implement a timeout on I_rxe.

1.2.2 PPON2 timer

Description

In AP2P mode, if I_txe is not read out before I_gpe, the PPON2 timer is not started, and therefore I_ppon2 is not signaled.

Workaround

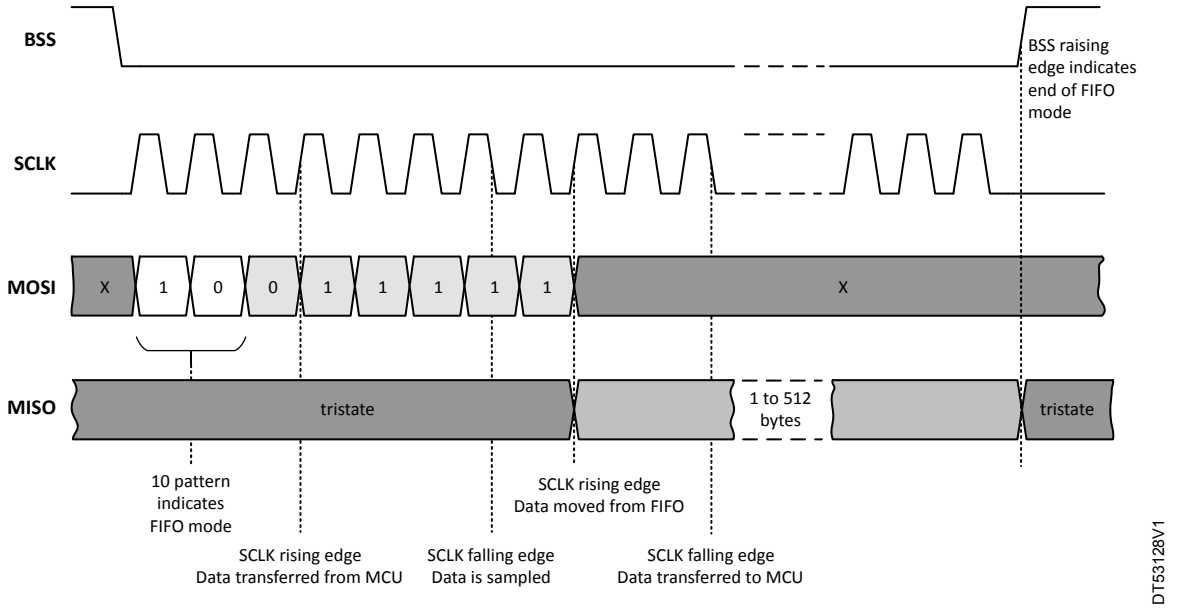
Use an MCU timer to cover the PPON2 timeout.

1.2.3 Serial peripheral interface (SPI)

Description

During the read operation of the interrupt status register, under specific bit patterns of the MOSI line identified as X in Figure 1, the interrupt flags might not be valid, and the interrupt line stays high.

Figure 1. SPI communication: FIFO reading



Workaround

The MOSI line must be driven low after the interrupt status register address bits, as shown in Figure 2 and Figure 3, for reading single and multiple bytes.

Figure 2. SPI communication: reading a single byte

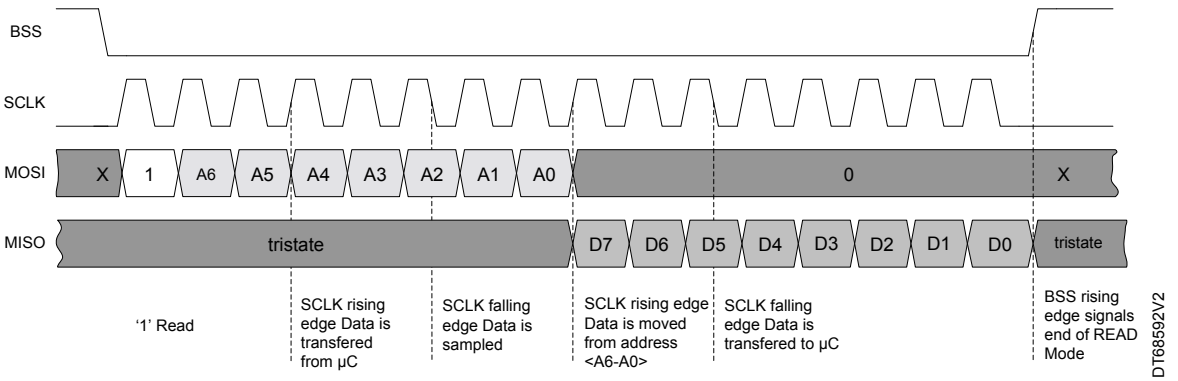
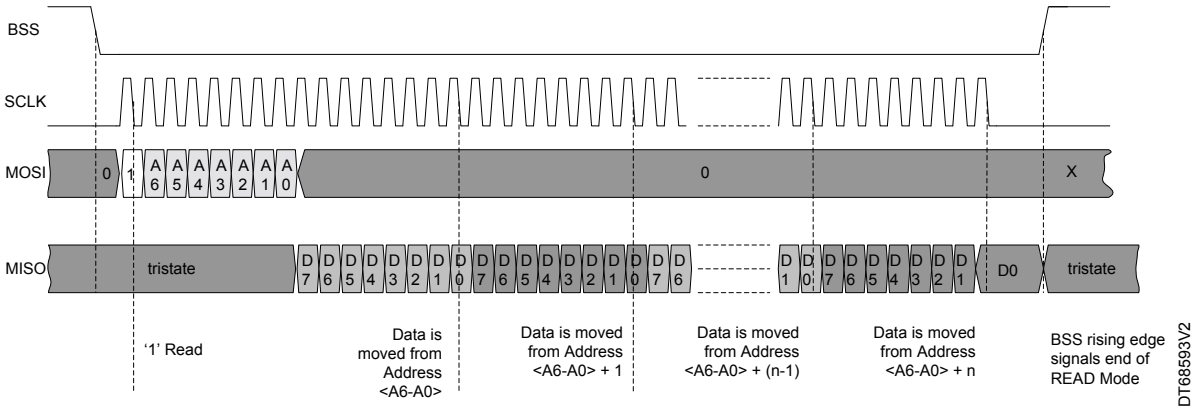


Figure 3. SPI communication: reading multiple bytes



Revision history

Table 2. Document revision history

Date	Revision	Changes
29-Nov-2019	1	Initial release.
03-Jul-2020	2	Added ST25R3920 root part number
01-Oct-2020	3	Added: • Section 1.2.1: Missing I_rxe interrupt • Section 1.2.2: PPON2 timer Updated: • Table 1. Summary of silicon limitations
27-Jan-2025	4	Added: • Added ST25R3918 root part number • Section 1.2: Interrupt and associated reporting limitations • Section 1.2.3: Serial peripheral interface (SPI) Updated: • Table 1. Summary of silicon limitations

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