STM32WL33xx device errata

Applicability

This document applies to the part numbers of STM32WL33xx devices and the device variants as stated in this page.

It gives a summary and a description of the device errata, with respect to the device datasheet and reference manual RM0511.

Deviation of the real device behavior from the intended device behavior is considered to be a device limitation. Deviation of the description in the reference manual or the datasheet from the intended device behavior is considered to be a documentation erratum. The term *"errata"* applies both to limitations and documentation errata.

Table 1. Device summary

Reference	Part numbers
STM32WL33xx	STM32WL33C8, STM32WL33CB, STM32WL33CC, STM32WL33K8, STM32WL33KB, STM32WL33KC

Table 2. Device variants

Reference	Silicon revision codes	
	Device marking(1)	DIE_ID(2)
STM32WL33Cx	Z	0x0120
STM32WL33Kx		

1. *Refer to the device datasheet for how to identify this code on different types of package.*
2. *Register system controller (SYSCFG) - DIE_ID register.*

1 Summary of device errata

The following table gives a quick reference to the STM32WL33xx device limitations and their status:

A = limitation present, workaround available

N = limitation present, no workaround available

P = limitation present, partial workaround available

"-" = limitation absent

Applicability of a workaround may depend on specific conditions of target application. Adoption of a workaround may cause restrictions to target application. Workaround for a limitation is deemed partial if it only reduces the rate of occurrence and/or consequences of the limitation, or if it is fully effective for only a subset of instances on the device or in only a subset of operating modes, of the function concerned.

Table 3. Summary of device limitations

Function	Section	Limitation	Status
			Rev. Z
System	2.2.1	MR_SUBG: aborting a TX command may lead to unpredictable behavior in some conditions	A
	2.2.2	MR_SUBG: the data buffer manager threshold status flags can be wrongly reported in some conditions	A
	2.2.3	MR_SUBG: the POSTAMBLE feature does not work with 4-(G)FSK modulation	A
	2.2.4	MR_SUBG: the "whitening before FEC" feature is not functional	A
	2.2.5	MR_SUBG: a continuous wave (CW) transmission cannot be stopped in a specific PA ramp configuration	A
	2.2.6	MR_SUBG: selectivity degradation for some channels	A
	2.5.1	LCD internal reference not working	A
	2.2.8	UART bootloader protocol does not work for VFQFPN32 package	N
ADC	2.3.1	Parts with untrimmed ADC compensation values	N
COMP	2.4.1	COMP internal reference voltage not working	P
LCD	2.2.7	MR_SUBG: CS_F flag is ignored by the sequencer in some cases	A

2 Description of device errata

The following sections describe the errata of the applicable devices with Arm® core and provide workarounds if available. They are grouped by device functions.

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2.1 Core

Reference manual and errata notice for the Arm® Cortex®-M0+ core revision r0p1 is available from http://infocenter.arm.com.

2.2 System

2.2.1 MR_SUBG: aborting a TX command may lead to unpredictable behavior in some conditions

Description

Issuing an SABORT on a TX command may lead to unpredictable event on AHB if it happens during the DBM prefetch phase..

This may lead to an AHB protocol violation.

Workaround

The SW must ensure the Radio FSM state reaches the TX state before to send the SABORT command.

2.2.2 MR_SUBG: the data buffer manager threshold status flags can be wrongly reported in some conditions

Description

The TX_ALMOST_EMPTY_x_F and RX_ALMOST_FULL_x_F flags can be raised inappropriately if the DATABUFFER_THR is modified between 2 commands.

This may lead to an AHB protocol violation.

Workaround

These flags must be cleared before the start of a new command.

2.2.3 MR_SUBG: the POSTAMBLE feature does not work with 4-(G)FSK modulation

Description

The POSTAMBLE pattern is limited to 010101... or 101010... whatever the selected modulation. The HW does not automatically adapt the POSTAMBLE pattern when the 4-(G)FSK modulation is selected (as for the PREAMBLE).

This causes a constant frequency deviation during the POSTAMBLE period. This frequency depends on the selected constellation mapping.

Workaround

Build the POSTAMBLE by software. This solution requires almost all of the frame to be built by software (from LENGTH, if present in the frame, to the POSTAMBLE):

- Only fixed length configuration can be used (FIX_VAR_LEN=0) on transceiver
- The hardware CRC must be disabled (to build in software)
- PCKLEN must be programmed with the full frame length (from LENGTH if present, to POSTAMBLE)
- If the receiver expects the length in the frame, a “LENGTH” bit field can be added by software when building the frame in the data buffer. In this case, the value must not be aligned on the PCKLEN value but on the PAYLOAD value.

2.2.4 MR_SUBG: the “whitening before FEC” feature is not functional

Description

The HW feature implemented to revert the order of a FEC + whitening sequence to have whitening first and then FEC is not functional. The frame generated when this feature is activated (PCKT_CTRL[10] = WHIT_BF_FEC = 1) does not fit with the expected frame.

The PCKT_CTRL[10] bit must be kept to 0 as this HW feature cannot be used.

Workaround

The feature can be built through a mixed SW/HW solution: the whitening (in transmission) / dewhitening (in reception) shall be done by SW while the FEC may be done by HW.

Note: CRC and LENGTH information, if required to be present in the frame, shall be managed by SW (PCKT_CONFIG[2:0] = CRC_MODE[2:0] = 3’b000 and PCKT_CONFIG[11] = FIX_VAR_LEN = 0), as they both need to be (de)whitened.

2.2.5 MR_SUBG: a continuous wave (CW) transmission cannot be stopped in a specific PA ramp configuration

Description

When PA_CONFIG[14] = PA_RAMP_ENABLE bit is set to 1 and PA_CONFIFG[1:0] = PA_RAMP_STEP_WIDTH[1:0] is different from zero, it is not possible to stop a CW transmission through the SABORT command. This limitation does not impact other configurations.

Need to take care of PA_CONFIG setting before generating a CW transmission.

Workaround

To modify the power ramp shape (smaller/larger steps) on a CW transmission, the user can modify the data rate parameter. The PA steps are managed as a ratio of a bit period, and so is impacted by the data rate selection. On the other hand, the data rate information has no impact on the CW, as it does not modulate any data.

2.2.6 MR_SUBG: selectivity degradation for some channels

Description

When the SMPS is on, for carriers which are multiples of fXO/12 or fXO/6, the sensitivity can be strongly degraded. (fXO is the HSE crystal frequency, nominally 48 MHz).

This causes sensitivity degradation.

Workaround

Several workarounds are possible:

1. Change the crystal frequency in the range 47 MHz-50 MHz.
2. Use the Bypass-on-the-fly feature.
3. Change the SMPS internal clock frequency via the KRM feature.

2.2.7 MR_SUBG: CS_F flag is ignored by the sequencer in some cases

Description

The FAST_RX_TERM_F flag is raised 16 µs after the Fast Termination counter expiration (to let the radio exit RX state and reach IDLE state). If enough power reaches the antenna during the first 250 ns of this phase, the CS_F is also raised .

In this scenario, both CS_F and FAST_RX_TERM_F will be raised, but the CS_F, that is raised first, shall be ignored, the relevant flag is the FAST_RX_TERM_F.

The programmed sequence is not correctly handled in this case.

Workaround

This behavior requires some precaution when building scenarios through the Sequencer. For instance, if the CS_F is defined as a match event in NextAction1Mask and the FAST_RX_TERM_F is defined as a match event in the other NextAction2Mask in a SeqAction0, there is the need to add the FAST_RX_TERM_F as a match event in the SeqAction1 to move to SeqACtion2 (which is the actual state that shall be reached because of the FAST_RX_TERM_F).

2.2.8 UART bootloader protocol does not work for VFQFPN32 package

Description

Note: This limitation applies only to parts with a traceability code dated before week 21 of 2024.

The UART bootloader is configured to use the following USART pins:

- USART_RX = PA15
- USART_TX = PA1

The PA15 (USART_RX) function is not available in the VFQFPN32 package.

This means that that the UART bootloader protocol is not usable for the part numbers listed below:

- STM32WL33K8
- STM32WL33KB
- STM32WL33KC

Workaround

None.

2.3 ADC

2.3.1 Parts with untrimmed ADC compensation values

Description

Note: This limitation applies only to parts with a traceability code dated before week 21 of 2024.

Untrimmed parts contain the default value 0xFFFFFFFF for gain and offset compensation data, resulting in suboptimal ADC performance.

The APIs listed below are used to retrieve the compensation data. These APIs return 0xFFFFFFFF if there is no calibration point.

- `LL_ADC_GET_CALIB_GAIN_FOR_VINPX_3V6(void)`
- `LL_ADC_GET_CALIB_OFFSET_FOR_VINPX_3V6(void)`
- `LL_ADC_GET_CALIB_GAIN_FOR_VINPX_2V4(void)`
- `LL_ADC_GET_CALIB_OFFSET_FOR_VINPX_2V4(void)`
- `LL_ADC_GET_CALIB_GAIN_FOR_VINPX_1V2(void)`
- `LL_ADC_GET_CALIB_OFFSET_FOR_VINPX_1V2(void)`
- `LL_ADC_GET_CALIB_GAIN_FOR_VINMX_3V6(void)`
- `LL_ADC_GET_CALIB_OFFSET_FOR_VINMX_3V6(void)`
- `LL_ADC_GET_CALIB_GAIN_FOR_VINMX_1V2(void)`
- `LL_ADC_GET_CALIB_OFFSET_FOR_VINMX_1V2(void)`
- `LL_ADC_GET_CALIB_GAIN_FOR_VINMX_2V4(void)`
- `LL_ADC_GET_CALIB_OFFSET_FOR_VINMX_2V4(void)`
- `LL_ADC_GET_CALIB_GAIN_FOR_VINDIFF_3V6 (void)`
- `LL_ADC_GET_CALIB_OFFSET_FOR_VINDIFF_3V6(void)`
- `LL_ADC_GET_CALIB_GAIN_FOR_VINDIFF_2V4(void)`
- `LL_ADC_GET_CALIB_OFFSET_FOR_VINDIFF_2V4(void)`

- `LL_ADC_GET_CALIB_GAIN_FOR_VINDIFF_1V2(void)`
- `LL_ADC_GET_CALIB_OFFSET_FOR_VINDIFF_1V2(void)`

Workaround

None.

2.4 COMP

2.4.1 COMP internal reference voltage not working

Description

The COMP negative input can use an internal generated voltage. This voltage is generated as a fraction of the battery voltage instead of 1.2 V internal voltage.

This causes the internal COMP generated voltage to be battery-level dependent.

Workaround

Take into account the dependance, or do not use this feature.

2.5 LCD

2.5.1 LCD internal reference not working

Description

The internal reference is not working, the LCD generates a wrong LCD supply voltage.

This causes the LCD to not work.

Workaround

Use the external reference on PB15 pin, setting VSEL = 1 in the LCD control register (LCD_CR) . The voltage has to be between 2.62 V and 3.6 V.

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Revision history

Table 4. **Document revision history**

Date	Version	Changes
26-Oct-2023	1	Initial release.
05-Feb-2024	2	Added errata: • Section 2.2.8: UART bootloader protocol does not work for VFQFPN32 package.
17-Apr-2024	3	Added errata: • Section 2.3.1: Parts with untrimmed ADC compensation values.
17-Sep-2024	3	Added a note concerning errata applicability to device trace codes in: • Section 2.2.8: UART bootloader protocol does not work for VFQFPN32 package • Section 2.3.1: Parts with untrimmed ADC compensation values.

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