VD55G1

Errata sheet

Limitations of the VD55G1

Introduction

This document covers the known limitations of the VD55G1, and workarounds, when available.

1 I2C/I3C

1.1 Repeated start

There is a limitation in the case of `Read from Random Location` that must always be initiated with a `Start` condition (not a repeated start).

Workaround

Always initiate `Read from Random Location` with `Start` condition (not a repeated start).

1.2 I3C image readout

GPIO to start image readout cannot be triggered once at the beginning at the frame. GPIO is triggered every line to read a line.

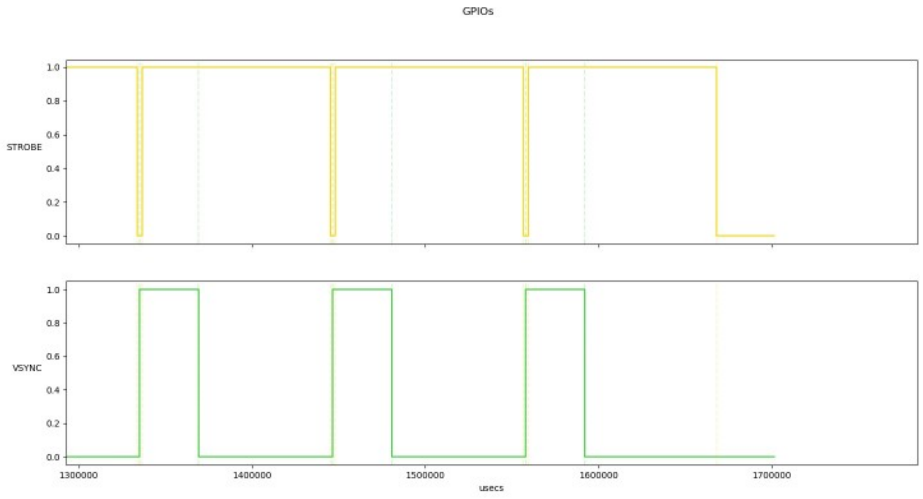
Workaround

None

2 GPIOs

2.1 Extra strobe sent in overlap

When the exposure overlaps over frames, a strobe/integration is present after the last frame readout.

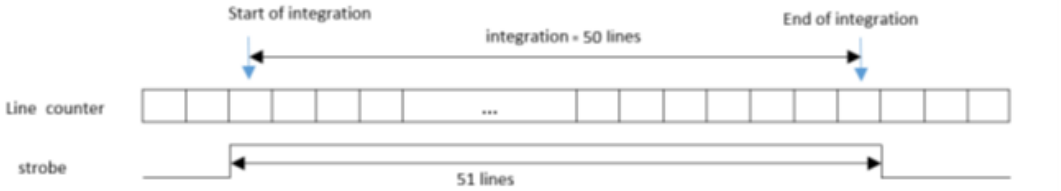


Workaround

None

2.2 Strobe signal does not match exposure register

The strobe signal length is the integration time plus 1 line. As represented in the figure below, the strobe signal begins a half-line time before, and ends a half-line time after the integration.



Workaround

None

2.3 PWM strobe edge synchronization

PWM is not synchronized with strobe output. This means that the PWM and strobe edge are not aligned. If the number of PWM cycles in the strobe envelope is low, it can affect the actual duty cycle.

Workaround

None

2.4 GPIOs in STANDBY state

The control of GPIOs while in SW STBY state is not supported.

Workaround

None

2.5 VSYNC start delay does not support negative values

VSYNC start delay is a signed value of the delay to apply in lines.

This register accepts only values [0-127]. Values [128-255] are not supported.

3 PLL

3.1 Fractional part

The fractional part of the PLL does not work. The PLL device cannot generate any MIPI frequency from the input clock.

Workaround

The output clock must always be a multiple of the input clock. For example, 1200 Mbps for a 12 MHz clock.

3.2 MIPI data rate 751-780 Mbps

The pixel clock exceeds it specification range (> 150 MHz) when using the MIPI data-rate in the range [750, 780].

Workaround

None. Do not use the MIPI data rate of [750, 780].

3.3 MIPI data rate 400-450 and 800-900 Mbps

The charge pumps are not correctly set in the range [400-450] and [800-900] Mbps. In this range, the sensor cannot reach the saturation level, but a column FPN is visible.

Workaround

None, do not use the MIPI data rate of [400-450] and [800-900] Mbps.

4 Autoexposure

4.1 Dual autoexposure

If the dual autoexposure feature is activated, the minimum frame margin is not enough.

Workaround

Add 25 lines to the minimum frame length.

5 QVGA at 480 fps cannot support all features

QVGA at 480 fps is very aggressive in terms of frame rate and cannot be guaranteed in all conditions.

Workaround

QVGA @480fps can be achieved with the following dedicated settings:

- WRITE_REG8 STREAM_STATICS_OIF_ULPM 'h01 # MIPI in ULPM
- WRITE_REG8 DBG_FULL_READ_OFFSET_9BIT 'h1F # 31
- WRITE_REG8 DBG_FW_LATCH_TIME 'h0A # 10
- WRITE_REG8 STREAM_STATICS_FORMAT_CTRL 'h08 # RAW8
- WRITE_REG8 STREAM_STATICS_VT_CTRL 'h04 # VT 9 bits
- WRITE_REG8 STREAM_CTX0_READOUT_CTRL 'h06 # 0x06: (XYBIN_X2)
- WRITE_REG8 STREAM_STATICS_LINE_LENGTH 'h03D2 # 978 pixels - 9 bits
- WRITE_REG8 EXPO_MANUAL_COARSE_EXP 'h00C8 # 200 lines
- WRITE_REG8 STREAM_CTX0_Y_HEIGHT 'h01E0 # 480 lines
- WRITE_REG8 STREAM_CTX0_X_WIDTH 'h0280 # 640 lines
- WRITE_REG8 STREAM_CTX0_FRAME_LENGTH 'h013F # 319 lines
- WRITE_REG8 CHANNEL_STATS_ROI_REDUCE_FACTOR 'h10 # 16 lines removed to the stats ROI

6 Low power

The device enables the low power as soon as the interframe is long enough. The interframe is computed as below:

$$Low\ \ power\ \ Inter\ \ Frame\ \ =\ \ Frame\ \ length - Coarse\ \ Integration - Output\ \ Y\ \ size - 100$$

Note: Coarse integration time must be doubled when in subtraction mode.

As soon as the **Low power Interframe** exceeds a value of 509, the sensor activates the low power. The formula to find the maximum integration time to be always in low power is the following:

$$Max\ \ integration\ \ time\ \ for\ \ low\ \ power\ \ =\ \ Frame\ \ length - 509 - Output\ \ Y\ \ size - 100$$

For example, the application should limit the integration time to 6.79 ms to always have the benefit of this low-power mechanism with the following configuration:

Table 1. Low-power configuration

MIPI data rate	1200 Mbps
Line time	7.52 us (Line length = 1128)
Output resolution	804x704
Frame rate	60 fps (frame length = 2216)
Max integration time for low power	6.79 ms (coarse integration = 903)

6.1 Missing frames

The device misses frames when switching (on the fly) between low power feasible and low power.

Workaround 1

Always keep the integration time below the `Max integration time for low power`. One easy way is to use the EXPOSURE_USER_MAX_COARSE_INTEGRATION_LINES register.

Workaround 2

The application can disable the low power mechanism with ENABLE_LOW_POWER_MODE register.

Table 2. ENABLE_LOW_POWER_MODE register definition

Register name	ENABLE_LOW_POWER_MODE
Register address	0x976
Register size	8 bits
Register values	0: Low power disabled 1: Low power enabled (Default)

7 Slave mode

When using the slave mode of the GPIO_0, polarity cannot be changed.

Workaround

None

Revision history

Table 3. **Document revision history**

Date	Version	Changes
29-Nov-2024	1	Initial release

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