ACCORDO5

Automotive Infotainment SoC for Instrument Clusters

Optimized Bill-Of-Materials, Automotive Quality, Phone Projection support

The instrument cluster market is transforming from traditional mechanical to digital instrument displays providing to the end user a unique new experience. ST's Accordo5 offers a cost-effective solution for digital instrument clusters both for automotive and motorcycle applications.

ST's Accordo5 system-on-chip provides a powerful multi-core application architecture with an embedded microcontroller managing CAN interfaces, video decoder capabilities, best-in class 3D graphics and a hardware cryptographic engine.
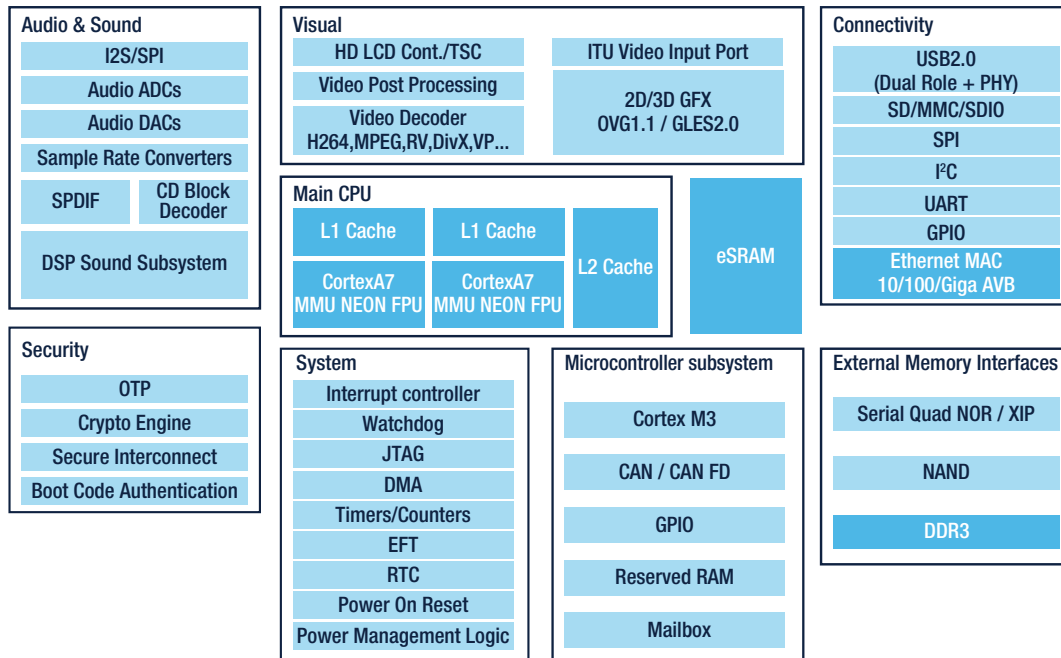
KEY FEATURES & BENEFITS

- Single or dual ARM Cortex A7 up to 650 MHz
- Full HD display with 4 layers overlay
- 3D GPU, OpenGL ES2.0, OpenVG1.1
- Multi-standard Video decoder (including H264)
- Flexible sound subsystem with integrated Audio DSP
- Isolated and secure CAN subsystem powered by ARM Cortex M3
- Video input Port for Rear Video Camera
- Integrated power management logic
- Secure boot and and hardware accelerated crypto
- Gb ETH with AVB
- USB 2.0, SD/SDIO, CAN/CAN-FD, SPI, I2C, UART
- Stand-by power ~20 µA
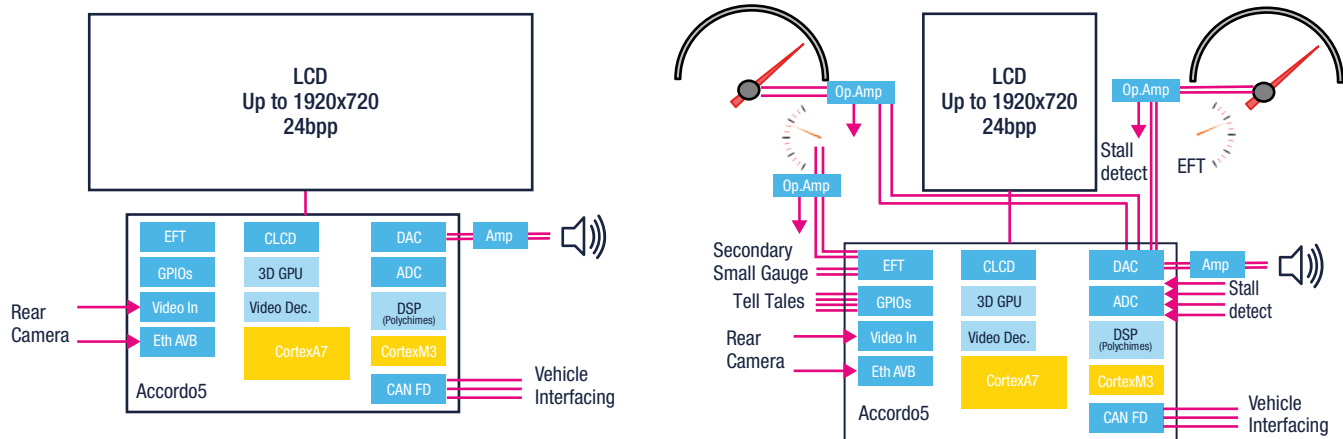- Industry's most optimized system Bill-Of-Materials

SOFTWARE OFFERING

- Linux OS kernel + BSP
- Standard Yocto tools
- FreeRTOS for Cortex M3
- Bootloader toolset
- MCAL for AUTOSAR support
- TouchGFX and 3rd party HMI design tools supported

Accordo5 block diagram

Audio & Sound
- I2S/SPI
- Audio ADCs
- Audio DACs
- Sample Rate Converters
- SPDIF
- CD Block Decoder
- DSP Sound Subsystem

Visual
- HD LCD Cont./TSC
- ITU Video Input Port
- Video Post Processing
- 2D/3D GFX OVG1.1 / GLES2.0
- Video Decoder H264,MPEG,RV,DivX,VP...

Connectivity
- USB2.0 (Dual Role + PHY)
- SD/MMC/SDIO
- SPI
- I²C
- UART
- GPIO
- Ethernet MAC 10/100/Giga AVB

Main CPU
- L1 Cache
- L1 Cache
- L2 Cache
- CortexA7 MMU NEON FPU
- CortexA7 MMU NEON FPU
- eSRAM

Security
- OTP
- Crypto Engine
- Secure Interconnect
- Boot Code Authentication

System
- Interrupt controller
- Watchdog
- JTAG
- DMA
- Timers/Counters
- EFT
- RTC
- Power On Reset
- Power Management Logic

Microcontroller subsystem
- Cortex M3
- CAN / CAN FD
- GPIO
- Reserved RAM
- Mailbox

External Memory Interfaces
- Serial Quad NOR / XIP
- NAND
- DDR3

Example solution

Operating conditions

- ARM_VDD: 1.20V ±5%
- VDD_IO_3V3: 3.3V ±10%
- VDD_IO_1V8: 1.8V ±10%
- VDDQ (DDR3L): 1.35V ± 5%
- Junction temperature up to +125 °C
- Automotive Grade AEC-Q100 grade 3

PACKAGE INFORMATION

- 529-ball LFBGA (19 x 19 x 1.7 mm) package with 0.8 mm pitch

Part number	A7 cores	Memory Width
STA1275	1	16-bit
STA1295	2	32-bit

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