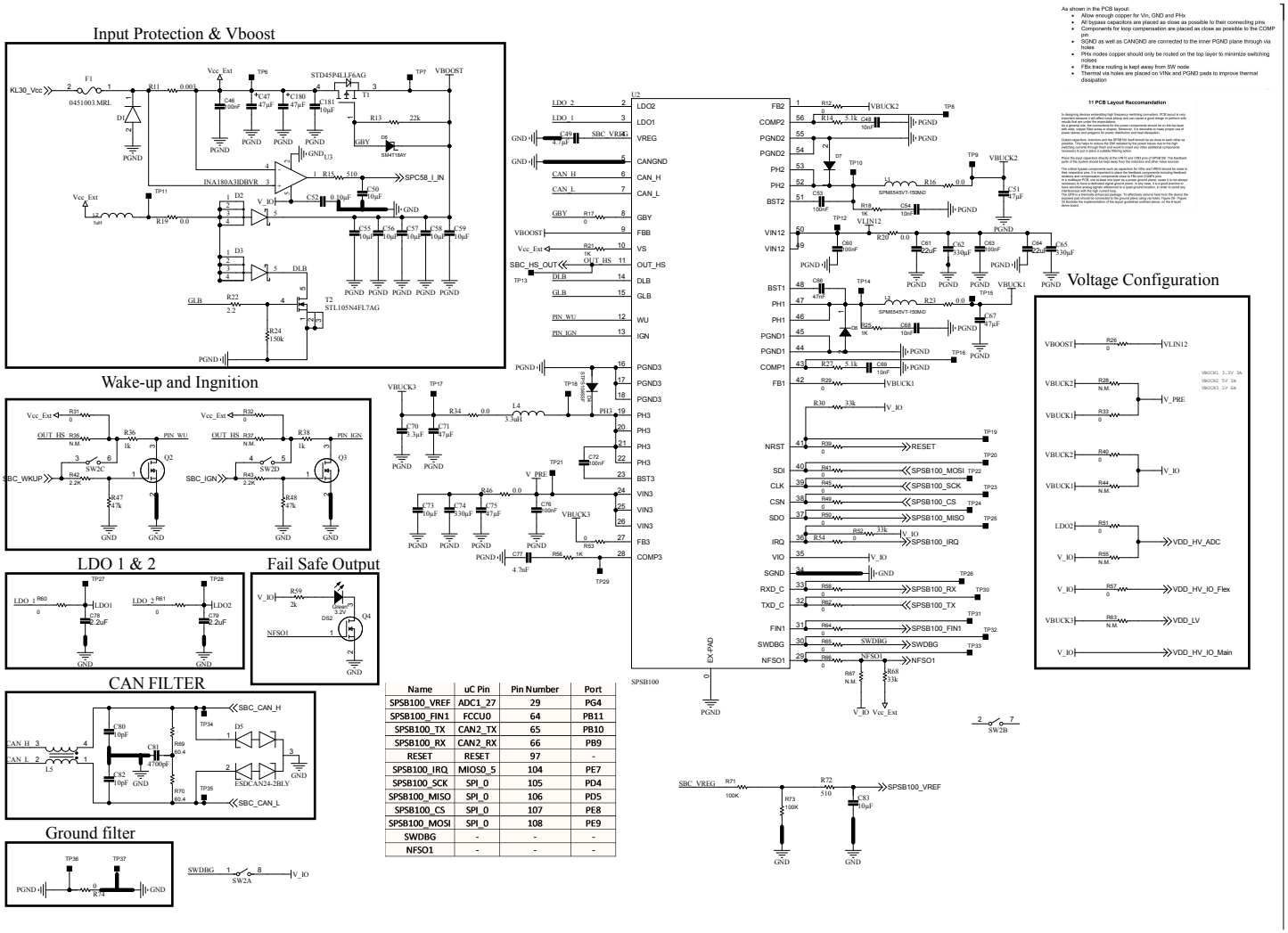
Schematic diagrams

Figure 1. AEK-POW-BMSLV circuit schematic (1 of 11)



Name	uC Pin	Pin Number	Port
SPSB100_VREF	ADC1_27	29	PG4
SPSB100_FIN1	FCCU0	64	PB11
SPSB100_TX	CAN2_TX	65	PB10
SPSB100_RX	CAN2_RX	66	PB9
RESET	RESET	97	-
SPSB100_IRQ	MIOS0_5	104	PE7
SPSB100_SCK	SPI_0	105	PD4
SPSB100_MISO	SPI_0	106	PD5
SPSB100_CS	SPI_0	107	PE8
SPSB100_MOSI	SPI_0	108	PE9
SWDBG	-	-	-
NFSO1	-	-	-

Figure 2. AEK-POW-BMSLV circuit schematic (2 of 11)

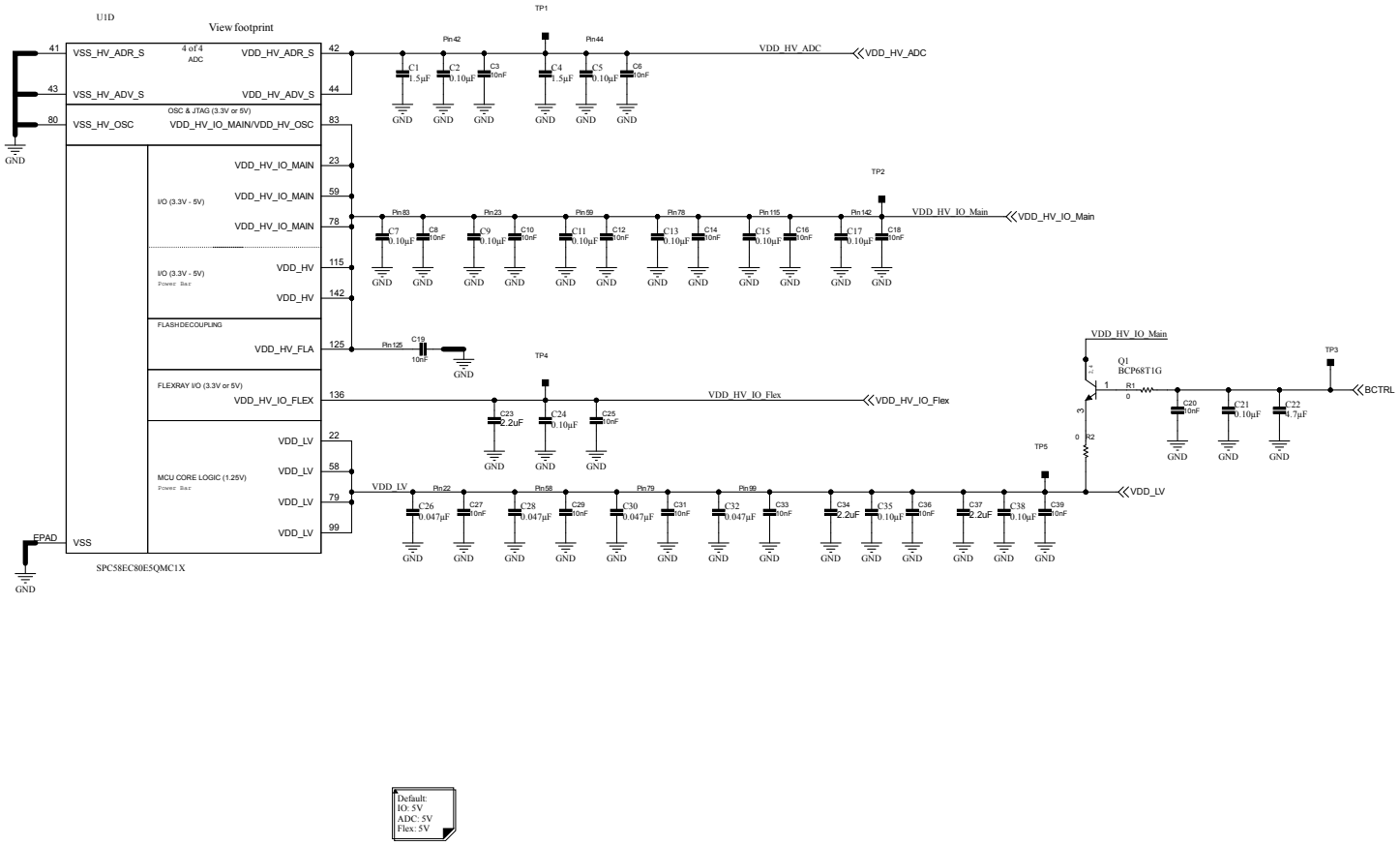
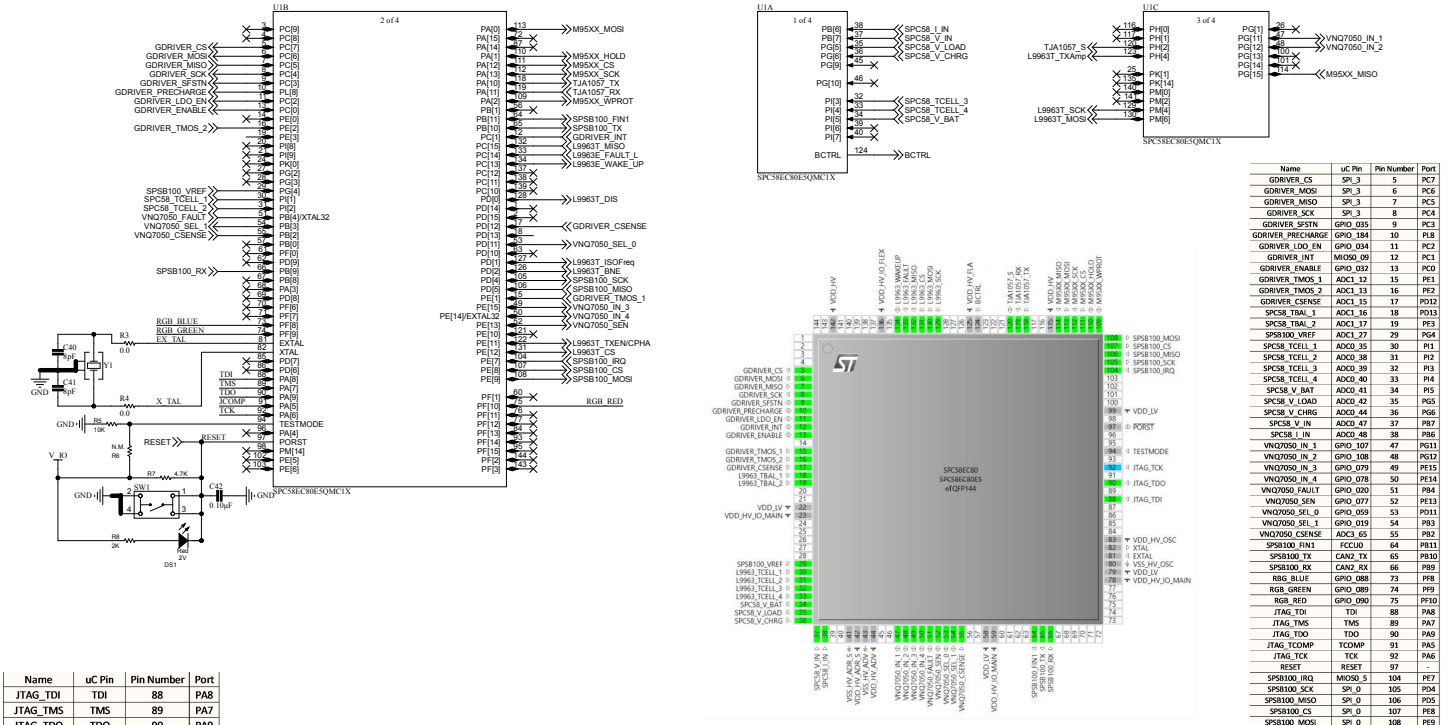


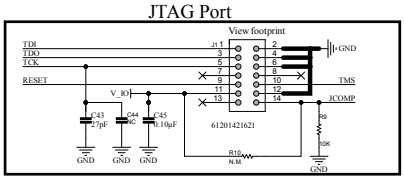
Figure 3. AEK-POW-BMSLV circuit schematic (3 of 11)



Name	uC Pin	Pin Number	Port
GDRIVER_CS	SPI_3	5	PC7
GDRIVER_MOSI	SPI_3	6	PC6
GDRIVER_MISO	SPI_3	7	PC5
GDRIVER_SCK	SPI_3	8	PC4
GDRIVER_SFSTN	GPIO_035	9	PC3
GDRIVER_PRECHARGE	GPIO_184	10	PL8
GDRIVER_LDO_EN	GPIO_034	11	PC2
GDRIVER_INT	MIOSO_09	12	PC1
GDRIVER_ENABLE	GPIO_032	13	PC0
GDRIVER_TMOS_1	ADC1_12	15	PE1
GDRIVER_TMOS_2	ADC1_13	16	PE2
GDRIVER_CSENSE	ADC1_15	17	PD12
SPC58_TBAI_1	ADC1_16	18	PD13
SPC58_TBAI_2	ADC1_17	19	PE3
SPSB100_VREF	ADC1_27	29	PG4
SPC58_TCELL_1	ADC0_35	30	PI1
SPC58_TCELL_2	ADC0_38	31	PI2
SPC58_TCELL_3	ADC0_39	32	PI3
SPC58_TCELL_4	ADC0_40	33	PI4
SPC58_V_BAT	ADC0_41	34	PI5
SPC58_V_LOAD	ADC0_42	35	PG5
SPC58_V_CHRG	ADC0_44	36	PG6
SPC58_V_IN	ADC0_47	37	PB7
SPC58_I_IN	ADC0_48	38	PB6
VNQ7050_IN_1	GPIO_107	47	PG11
VNQ7050_IN_2	GPIO_108	48	PG12
VNQ7050_IN_3	GPIO_079	49	PE15
VNQ7050_IN_4	GPIO_078	50	PE14
VNQ7050_FAULT	GPIO_020	51	PB4
VNQ7050_SEN	GPIO_077	52	PE13
VNQ7050_SEL_0	GPIO_059	53	PD11
VNQ7050_SEL_1	GPIO_019	54	PB3
VNQ7050_CSENSE	ADC3_65	55	PB2
SPSB100_FIN1	FCCU0	64	PB11
SPSB100_TX	CAN2_TX	65	PB10
SPSB100_RX	CAN2_RX	66	PB9
RBG_BLUE	GPIO_088	73	PF8
RGB_GREEN	GPIO_089	74	PF9
RGB_RED	GPIO_090	75	PF10
JTAG_TDI	TDI	88	PA8
JTAG_TMS	TMS	89	PA7
JTAG_TDO	TDO	90	PA9
JTAG_TCOMP	TCOMP	91	PA5
JTAG_TCK	TCK	92	PA6
RESET	RESET	97	-
SPSB100_IRQ	MIOSO_5	104	PE7
SPSB100_SCK	SPI_0	105	PD4
SPSB100_MISO	SPI_0	106	PD5
SPSB100_CS	SPI_0	107	PE8
SPSB100_MOSI	SPI_0	108	PE9
M95XX_WPROT	GPIO_002	109	PA2
M95XX_HOLD	GPIO_001	110	PA1
M95XX_CS	SPI_2	111	PA12
M95XX_SCK	SPI_2	112	PA13
M95XX_MOSI	SPI_2	113	PA0
M95XX_MISO	SPI_2	114	PG15
L9963_SCK	SPI_1	129	PM4
L9963_MOSI	SPI_1	130	PM6
L9963_CS	SPI_1	131	PE12
L9963_MISO	SPI_1	132	PC15
L9963_FAULT	MIOSO_27	133	PC14
L9963_WAKEUP	GPIO_045	134	PC13

Name	uC Pin	Pin Number	Port
JTAG_TDI	TDI	88	PA8
JTAG_TMS	TMS	89	PA7
JTAG_TDO	TDO	90	PA9
JTAG_TCOMP	TCOMP	91	PA5
JTAG_TCK	TCK	92	PA6

JTAG Port



Debug RGB

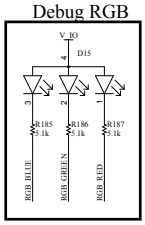


Figure 4. AEK-POW-BMSLV circuit schematic (4 of 11)

Pin Name	uC Pin	Pin Number	Port
SPC58_TBAL_1	ADC1_16	18	PD13
SPC58_TBAL_2	ADC1_17	19	PE3
SPC58_TCELL_1	ADC0_35	30	PI1
SPC58_TCELL_2	ADC0_38	31	PI2
SPC58_TCELL_3	ADC0_39	32	PI3
SPC58_TCELL_4	ADC0_40	33	PI4
L9963_SCK	SPI_1	129	PM4
L9963_MOSI	SPI_1	130	PM6
L9963_CS	SPI_1	131	PE12
L9963_MISO	SPI_1	132	PC15
L9963_FAULT	MIOS0_27	133	PC14
L9963_WAKEUP	GPIO_045	134	PC13

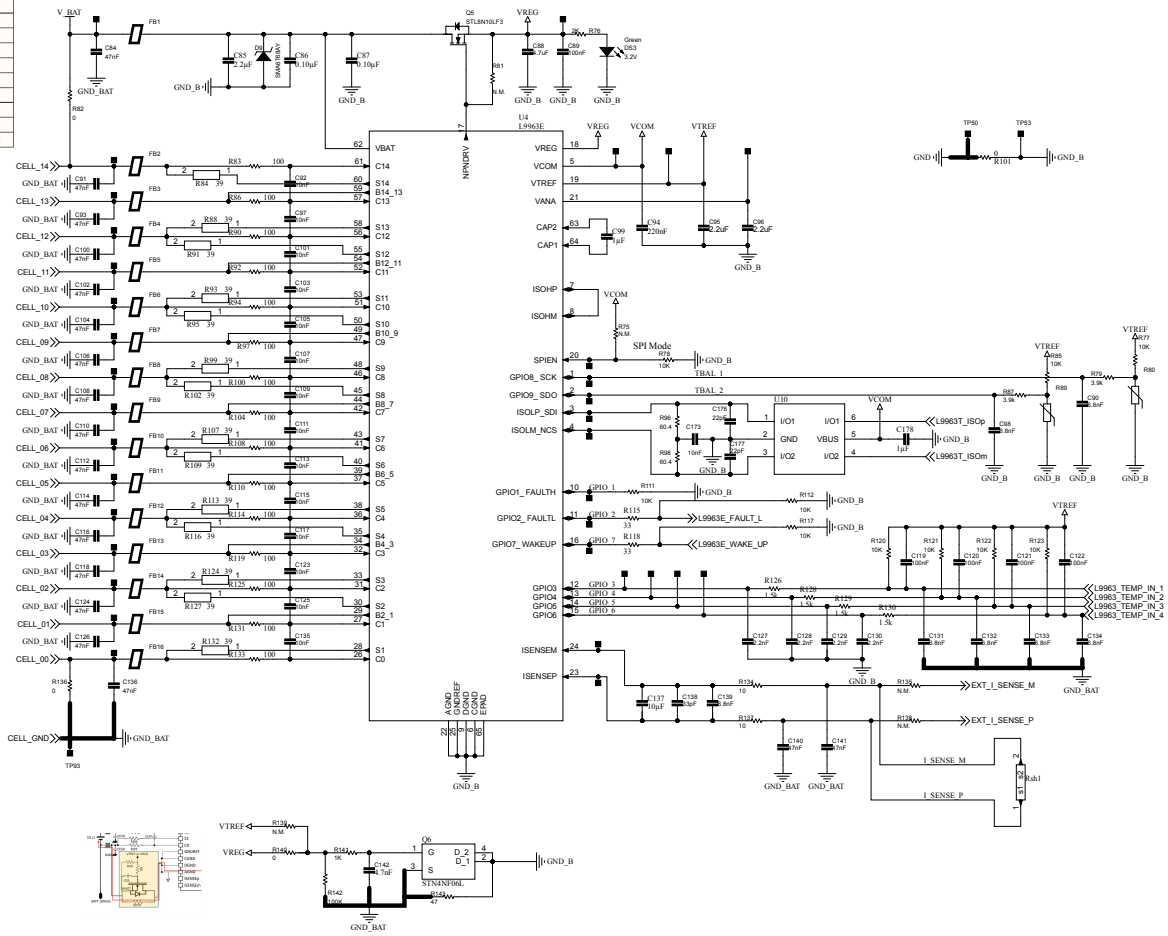


Figure 5. AEK-POW-BMSLV circuit schematic (5 of 11)

DISABLE				
DIS	Digital Input/Output (Open Drain)	Local	High	Transceiver Disable Input. Pull it up with external resistor connected to VIO. When DIS is high, L9963 enters in low power mode. When DIS is low, L99637 is enabled and working in Normal mode. It can be either pulled-down by the MCU to enable the unit, or pulled down internally when a wakeup condition occurs, in order to interrupt the MCU. Pin is internally pulled up with 100 kΩ resistor. Input filtered with RC filter having $f_{CUT\_pu\_dis}$ cut frequency.

ISOLATED SPI				
ISOP	Analog Input/Output	Global	-	Isolated SPI Positive terminal
ISOM	Analog Input/Output	Global	-	Isolated SPI Negative terminal
TXAMP	Digital Input	Local	-	Isolated SPI TX amplitude selection. Set low to select low amplitude/low threshold. Set high to select high amplitude/high threshold. Internally pulled up with a 150 kΩ resistor.
ISOFREQ	Digital Input	Local	-	Isolated SPI speeding frequency selection. Pull high to set high frequency. Pull down to set low frequency. Internally pulled down (active).

SPI				
SDO	Digital Output (Push-Pull)	Local	-	SPI Serial Data Output. Needs external pull up/pull down resistor to define inactive level.

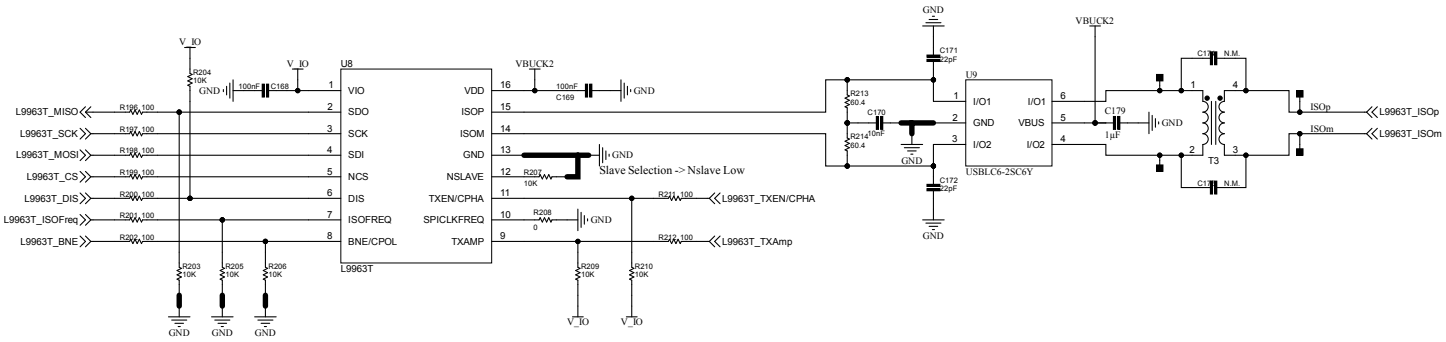


Figure 6. **AEK-POW-BMSLV circuit schematic (6 of 11)**

Pin Name	uC Pin	Pin Number	Port
M95XX_WPROT	GPIO_002	109	PA2
M95XX_HOLD	GPIO_001	110	PA1
M95XX_CS	SPI_2	111	PA12
M95XX_SCK	SPI_2	112	PA13
M95XX_MOSI	SPI_2	113	PA0
M95XX_MISO	SPI_2	114	PG15

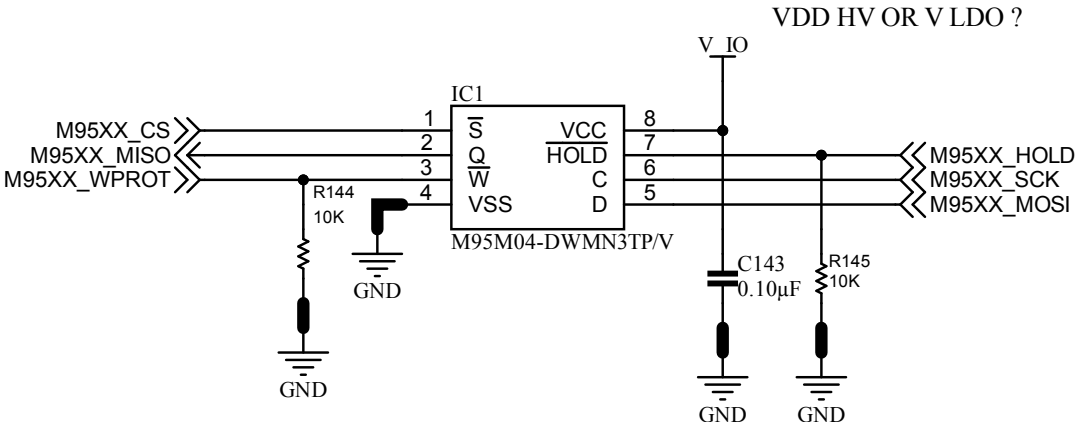
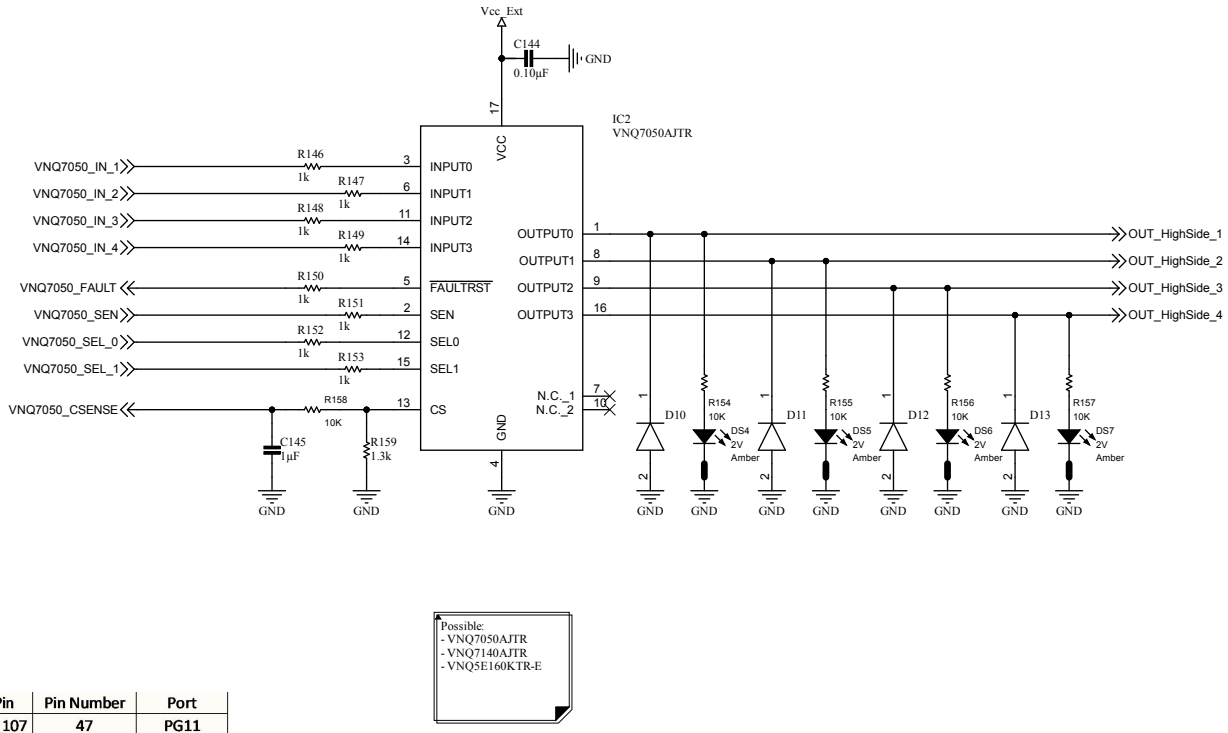


Figure 7. **AEK-POW-BMSLV circuit schematic (7 of 11)**



Pin Name	uC Pin	Pin Number	Port
VNQ7050_IN_1	GPIO_107	47	PG11
VNQ7050_IN_2	GPIO_108	48	PG12
VNQ7050_IN_3	GPIO_079	49	PE15
VNQ7050_IN_4	GPIO_078	50	PE14
VNQ7050_FAULT	GPIO_020	51	PB4
VNQ7050_SEN	GPIO_077	52	PE13
VNQ7050_SEL_0	GPIO_059	53	PD11
VNQ7050_SEL_1	GPIO_019	54	PB3
VNQ7050_CSENSE	ADC3_65	55	PB2

Figure 8. AEK-POW-BMSLV circuit schematic (8 of 11)

Opamp Temp 1 - 4

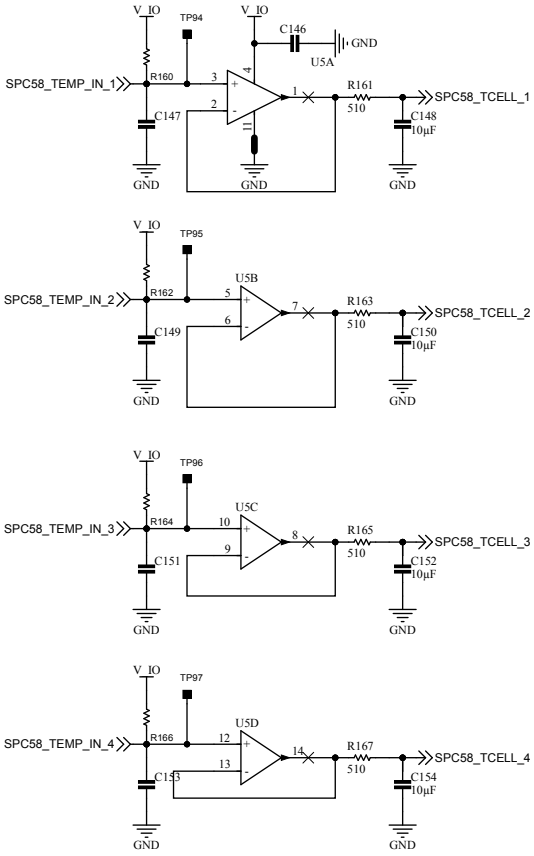


Figure 9. **AEK-POW-BMSLV circuit schematic (9 of 11)**

Opamp

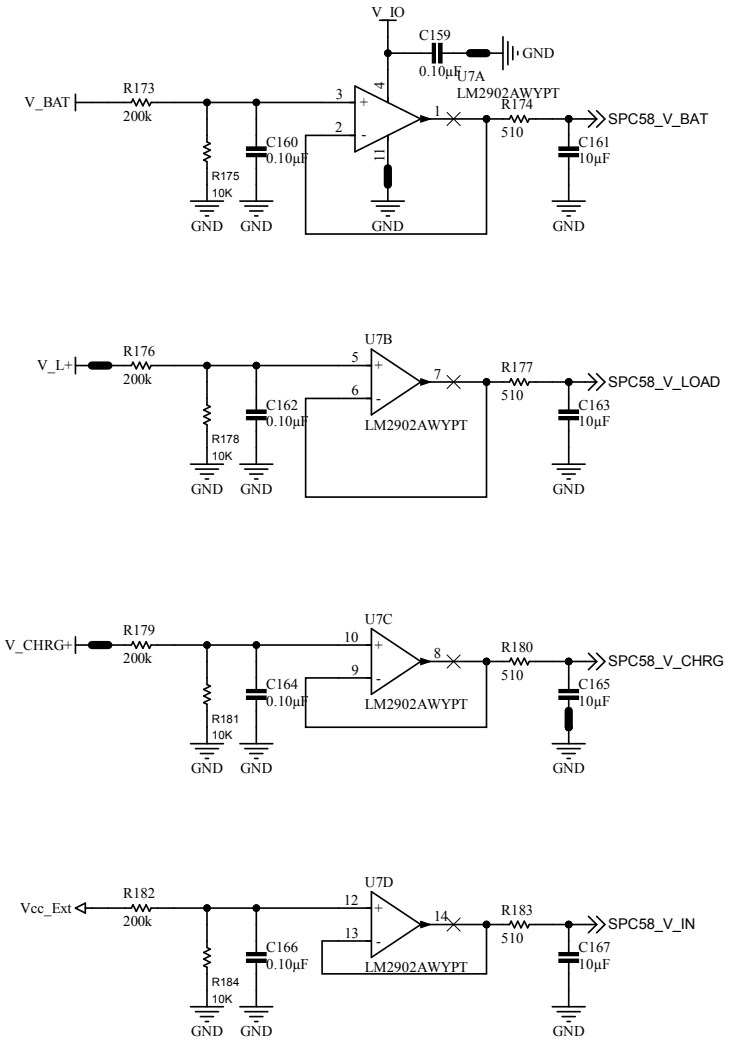
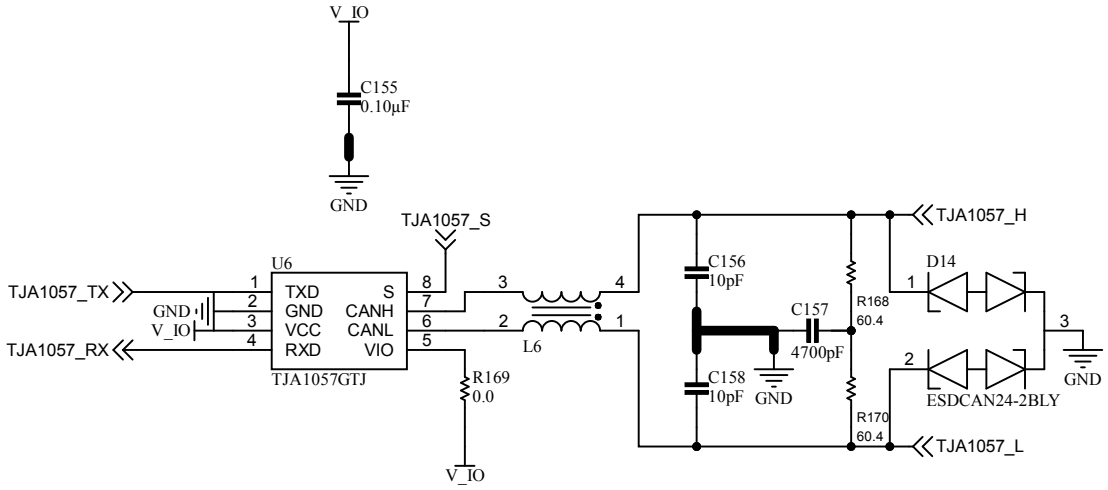
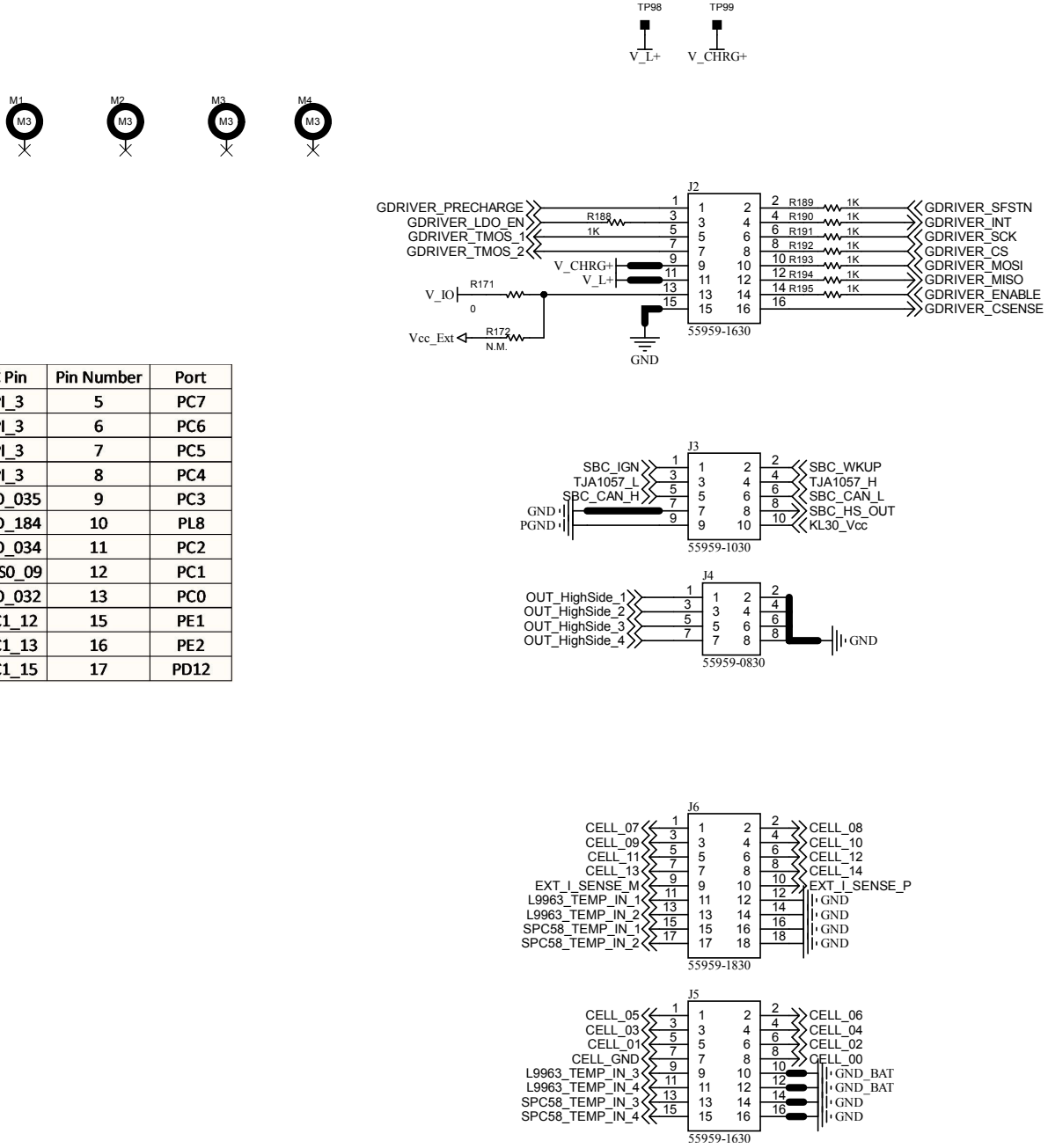


Figure 10. **AEK-POW-BMSLV circuit schematic (10 of 11)**



Name	uC Pin	Pin Number	Port
TJA1057_TX	CAN2_TX	118	PA10
TJA1057_RX	CAN2_RX	119	PA11
TJA1057_S	GPIO_114	120	PH2

Figure 11. **AEK-POW-BMSLV circuit schematic (11 of 11)**



Pin Name	uC Pin	Pin Number	Port
GDRIVER_CS	SPI_3	5	PC7
GDRIVER_MOSI	SPI_3	6	PC6
GDRIVER_MISO	SPI_3	7	PC5
GDRIVER_SCK	SPI_3	8	PC4
GDRIVER_SFSTN	GPIO_035	9	PC3
GDRIVER_PRECHARGE	GPIO_184	10	PL8
GDRIVER_LDO_EN	GPIO_034	11	PC2
GDRIVER_INT	MIOS0_09	12	PC1
GDRIVER_ENABLE	GPIO_032	13	PC0
GDRIVER_TMOS_1	ADC1_12	15	PE1
GDRIVER_TMOS_2	ADC1_13	16	PE2
GDRIVER_CSENSE	ADC1_15	17	PD12

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