Potential isolation issue between CPU1 and CPU2 on STM32WB5x, STM32WB3x, STM32WB1x, and STM32WL5x

Overview

This security advisory pertains to a potential isolation issue between CPU1 and CPU2 for the further listed affected products.

Affected products

Product	Version	Type	Note
STM32WB5x devices	Any	Silicon product	-
STM32WB3x devices	Any	Silicon product	-
STM32WB1x devices	Any	Silicon product	-
STM32WL5x devices	Any	Silicon product	-

Description

Software running on the CPU1 subsystem can interfere with the CPU2 subsystem thus breaking the isolation between those subsystems, even when the system security flag is enabled (the ESE bit is set to 1).

Impact

If an attacker can introduce and execute software on CPU1, they can use CPU1 to take control over the CPU2 subsystem software execution.

For example, when two different application owners execute software on CPU1 and CPU2, respectively, the isolation is not guaranteed and the CPU1 software can access to or interfere with the CPU2 subsystem.

Remediation

Do not use the CPU2 subsystem to store or manage assets that must be isolated from the CPU1 subsystem.

Credit

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The individuals above contacted ST separately.

Contact information

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SA0024 - Rev 1 - December 2024
For further information contact your local STMicroelectronics sales office.

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Revision history

Table 1. Document revision history

Date	Version	Changes
17-Dec-2024	1	Initial version.

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