



**ESD protection with ultra-low capacitance
for high bandwidth applications**

Introduction

This article is addressed to engineers and designers considering ESD protection solutions in the high-speed digital data transmission world.

The document offers:

- an explanation of the vital role of ESD protection devices
- a comparison of the considerable benefits of the diode array solution compared to the single diode per line solutions
- a comprehensive description of the importance of transparent presence of protection devices that can thus ensure digital data transmission integrity through ultra-low capacitance and very high bandwidth characteristics

STMicroelectronics offers a broad portfolio of ESD protection devices for many applications. This article spotlights the technical advantages of the DVIULC6-4SC6 product. This product offers protection beyond the current standards. At the same time the DVIULC6-4SC6 ensures unprecedented levels of transparency that ensure digital data transmission integrity.

Market trends

The next generation of computer and consumer products will use data serialization at much higher transmissions speeds. Protection against electrostatic discharge (ESD) is vital for such products.

Protection devices must offer compliance with ESD protection standards. Equally important is that protection devices must not compromise the integrity of data transmission.

The new generation of ESD protection devices must provide data transmission transparency through

- greater bandwidth
- reduced capacitance
- consistent characteristics across production batches

For multi-line protection devices it is also vitally important for all line protection circuits to have symmetrical characteristics.

This technical article will show that the DVIULC6-4SC6 product provides a positive response to all these market requirements.

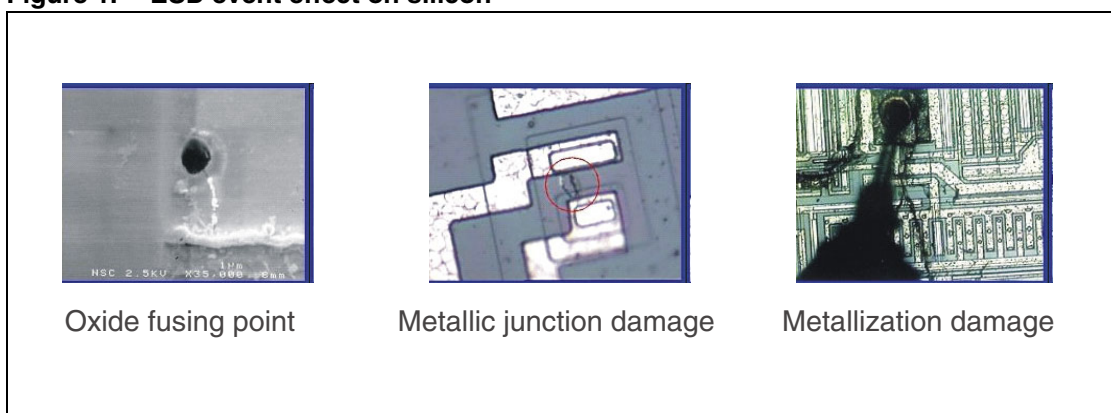
1 Why is ESD protection needed?

As shown in Figure 1, an ESD event can easily destroy an IC in several ways, resulting in one or more of these problems:

- junction leakage
- short circuits or burn-out
- dielectric rupture
- resistor-metal interface rupture
- resistor-metal fusing

Soft errors requiring shutdown and restart can be induced by ESD strike in the same time.

Figure 1. ESD event effect on silicon



These are the reasons why IC suppliers still recommend designing ESD protection devices to protect main chip sets. However, mainly driven by compact design trend, the implementation of external ESD protection will pose several challenges such as:

- highest level of ESD protection in the smallest possible size
- negligible effect on high speed digital and analog signal quality

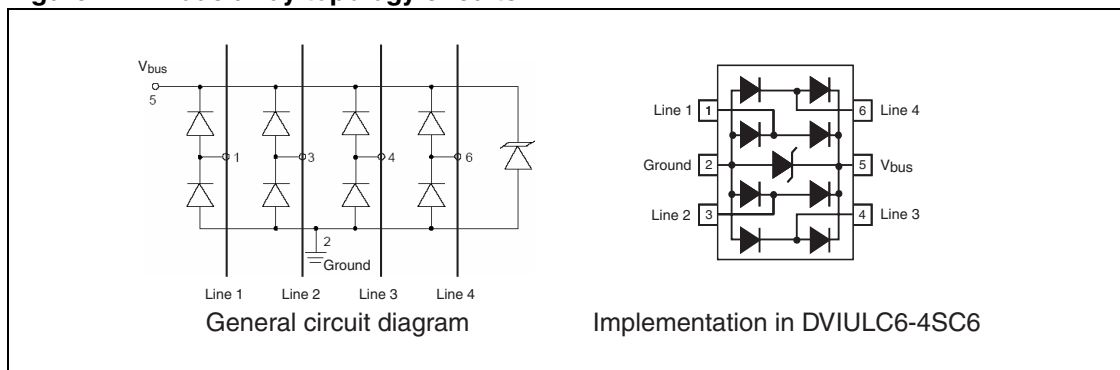
STMicroelectronics' DVIULC6-4SC6 responds to these requirements.

2 Diode arrays improve protection

Current line protection uses one diode to suppress ESD events. The diode array clamping concept uses two diodes conducting the positive and negative ESD events to ground. This configuration offers improved protection and highly significant benefits (ultra-low capacitance and high bandwidth) in the transparency of the protection solution during normal operations.

Figure 2 shows a general circuit diagram for a diode array protecting four lines together with the diode array configuration of the DVIULC6-4SC6.

Figure 2. Diode array topology circuits



2.1 Measured characteristics

Figure 3 shows the test setup used to evaluate the remaining output voltages at the output of the protection device after an ESD event.

Figure 3. ESD event test setup for DVIULC6-4SC6

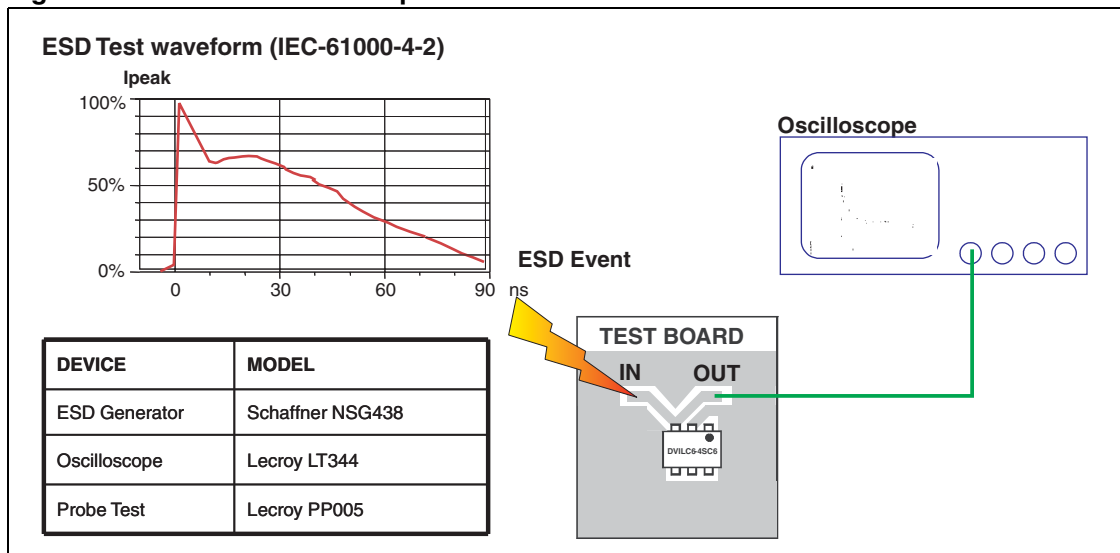


Figure 4. Output voltage when negative (-15kV) discharge applied to DVIULC6-4SC6

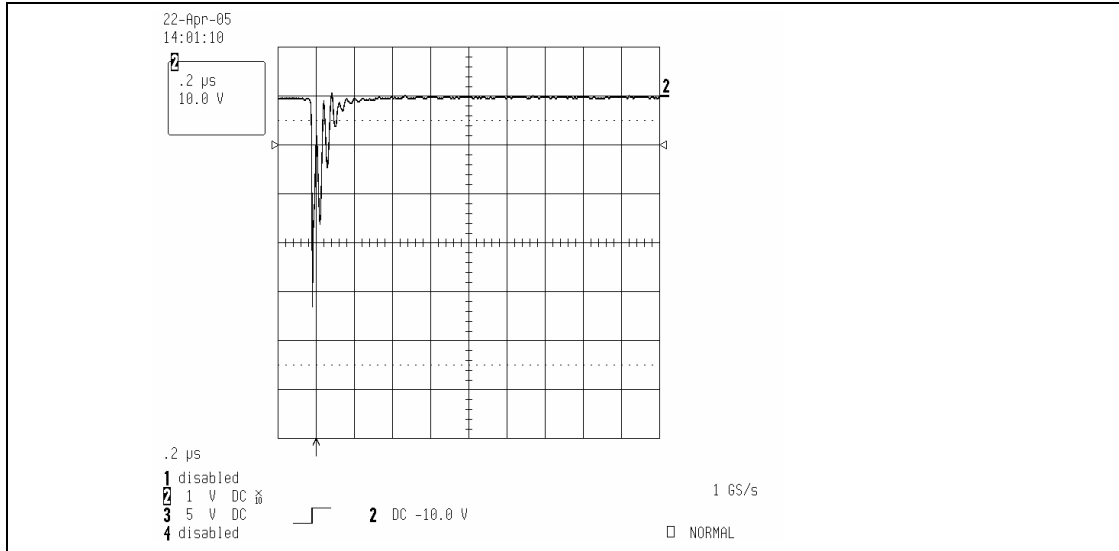
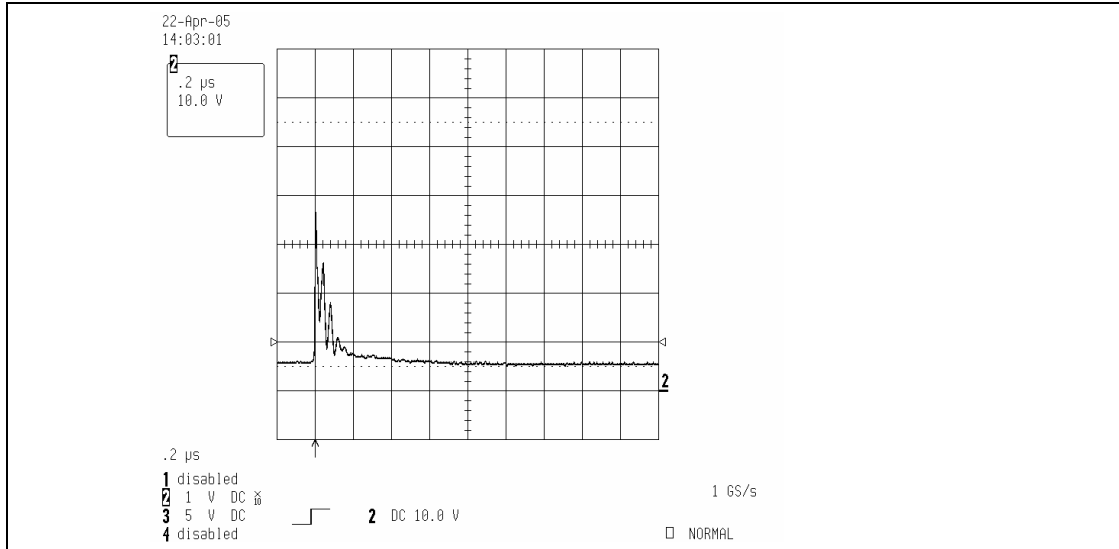


Figure 5. Output voltage when positive (+15kV) discharge applied to DVIULC6-4SC6



The test circuit was subjected to the industry standard IEC-61000-4-2 level 4 standard air discharge (see [Figure 3](#) for the test discharge waveform). The test result in [Figure 4](#) shows that diode array reduces the perceived discharge from a peak of -15 kV to a peak of 43 V for negative ESD event. The test result in [Figure 5](#) shows that diode array reduces the perceived discharge from a peak of +15 kV to a peak of 36 V for negative ESD event.

The lowest remaining voltage value reduces ESD damage risks, limits energy levels through the core chip set and also avoids any uncontrolled latch up effect. Another advantage offered by a silicon solution is the protection reliability. This solution can withstand multiple ESD events without any shift in electrical characteristics.

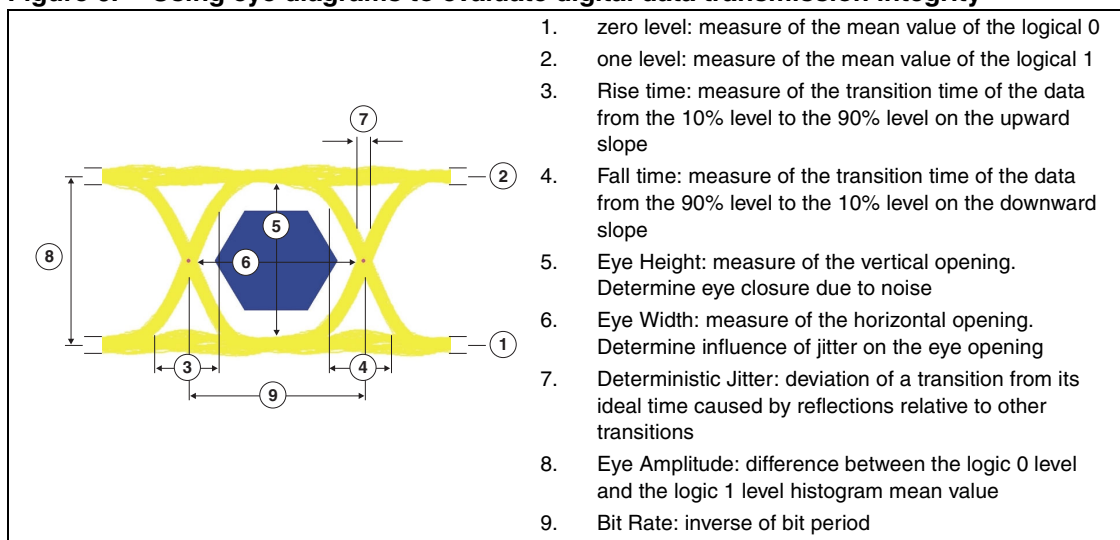
The tests show that the diode array topology is one of the best ESD protection solutions that complies with the most severe level of IEC61000-4-2 standard (level 4, 15 Kv air discharge & 8Kv contact discharge). The DVIULC6-4SC6 can handle contact and air discharges more severe than those expected in the IEC61000-4-2 standard level 4.

3 High speed data transparency

In addition to providing in excess of industry standard requirements for ESD protection, there is also an essential requirement of transparency to the protected application. That is, the presence of the protection device must have negligible impact on the normal performance of the protected application. For high speed data transparency this means that the protection device must be optimized for line capacitance and bandwidth. In addition, for multi-line protection, the device must present symmetrical characteristics in line capacitance and cut-off frequency to avoid un-equalized data channels and crosstalk.

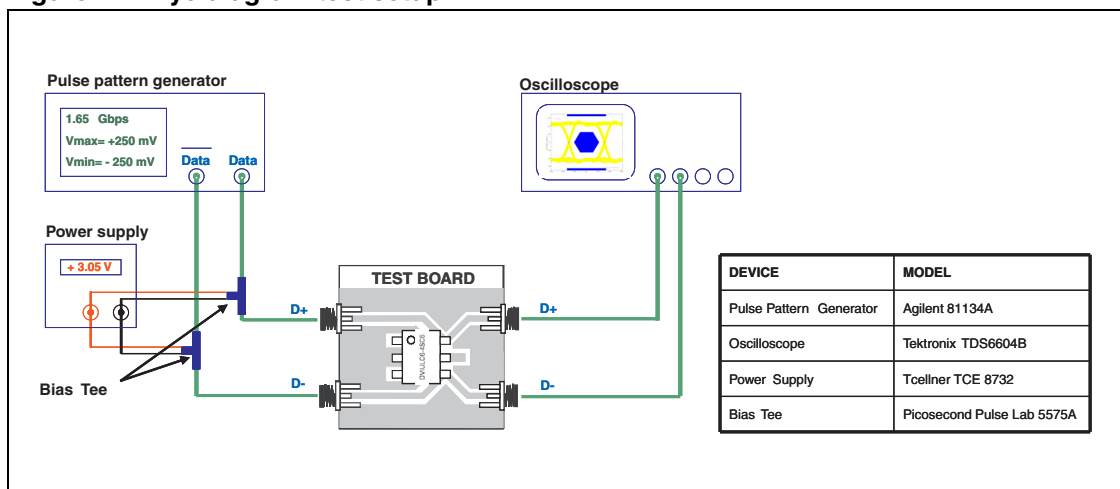
The line capacitance and bandwidth effects on digital data transmission integrity can be evaluated using the eye diagram technique. For anyone not familiar with the eye diagram technique, [Figure 6](#) offers an explanation of the critical points.

Figure 6. Using eye diagrams to evaluate digital data transmission integrity



[Figure 7](#) illustrates the eye diagram test setup typically used in the DVI standard.

Figure 7. Eye diagram test setup



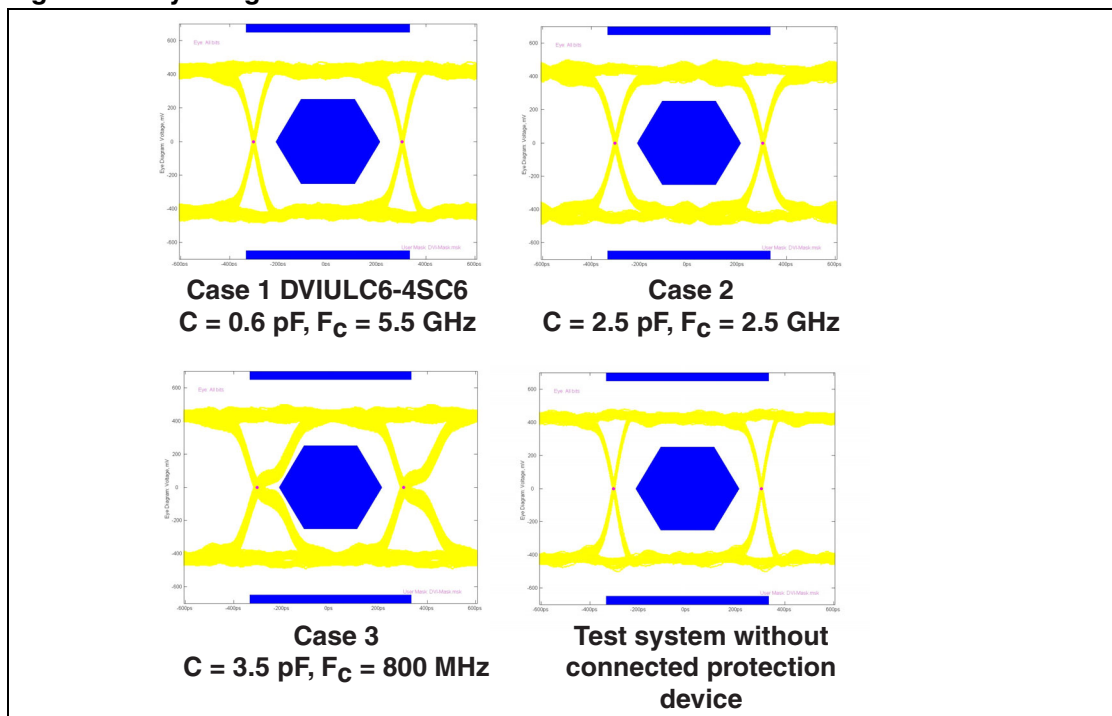
3.1 Measured characteristics

The eye diagrams for three different test cases are shown in *Figure 8*. The fourth eye diagram in *Figure 8* is for the test circuit only (generator and test board) without any connected protection device. The three test cases used to illustrate the importance of transparency are:

- Case 1 DVIULC6-4SC6 - 0.6 pF diode array protection with cutoff frequency⁽¹⁾ = 5.5 GHz
- Case 2 2.5 pF diode array protection with cutoff frequency^(1.) = 2.5 GHz
- Case 3 3.5 pF diode array protection with cutoff frequency^(1.) = 800 MHz

1. That frequency at which the signal strength drops to -3 dB of it's base value (See Figure 9.)

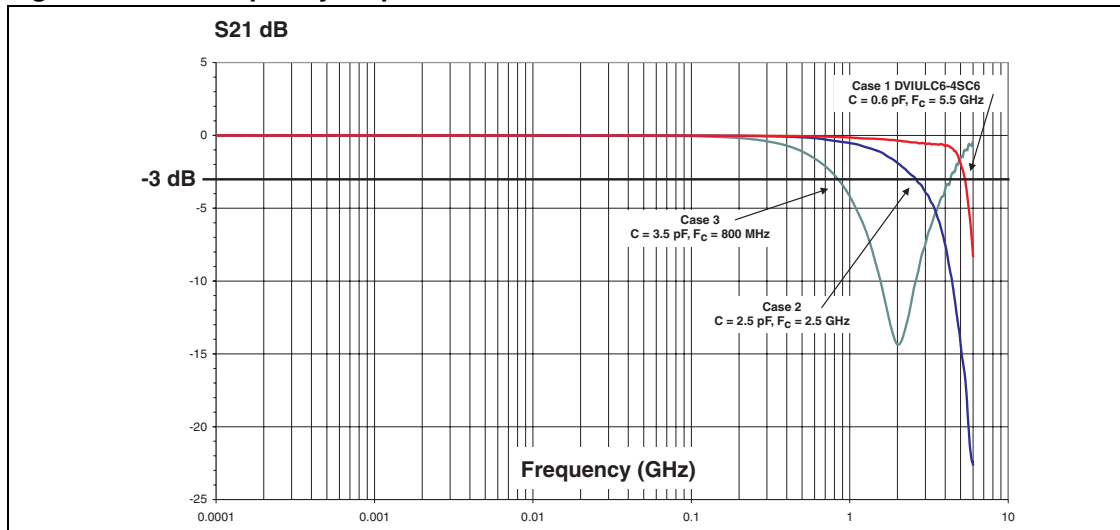
Figure 8. Eye diagram results for 1.65 Gb/s data transmission tests on 3 test cases



The eye diagram results in Figure 8. show that the DVIULC6-4SC6 device (test case 1) has the least effect on digital data transmission integrity. The eye diagram for test case 2 shows an increase in the variation of the received signal values (increased variation in the mean values for logical 1 and logical 0, and an increase in rise times and fall times). The eye diagram for test case 3 shows significant signal degradation; rise times and fall times show significant variation; the bit period value shows significant variation; transition time shows significant variation.

Test cases 2 and 3 indicate risk of data errors at the reception side. The DVIULC6-4SC6 tests (test case 1) show that risk of data error is minimized.

Figure 9. S21 frequency responses for the three test cases



3.2 Transparent effect on rise and fall times

Table 1. Effect of line capacitance and cutoff frequency on data rise and fall times

	Minimum rise time (ps) 10-90%	Minimum fall time (ps) 10-90%	DVI standard compliance	Rise and fall time variation ⁽¹⁾
Test bench without protection device in the test board		126	++	0 %
Case 1: DVIULC6-4SC6C C = 0.6 pF and F _c = 5.5 GHz diode array protection	133	136	++	8 %
Case 2: C = 2.5 pF and F _c = 2.5 GHz diode array protection	146	151	+	20 %
Case 3: C = 3.5 pF and F _c = 800 MHz diode array protection	306	308	-	244 %

1. Percentage variation in minimum rise and fall times with protection device connected compared with rise and fall times for test bench without protection device.

According to the DVI standard (Rev 1.0, 99 April 2nd), minimum rise times and fall times have to be less than 242 ps. [Table 1](#) shows that the DVIULC6-4SC6 solution complies with this standard.

The ultra low capacitance (0.6 pF) of the DVIULC6-4SC6 offers greater margins in designing the board and choosing the semiconductor devices to use. The DVIULC6-4SC6 results show extremely low impact on the rise and fall times of the signal (less than 8 % variation) and introduction of negligible delays for optimum data transmission signal integrity. With an insertion loss less than -0.2 dB in the 0 - 1.2 GHz frequency range and a cutoff frequency better than 5.5 GHz, this 0.6 pF diode array protection device is transparent to the application and minimizes the introduction of signal distortion and mismatching.

3.3 Symmetrical characteristics

Table 2. DVIULC6-4SC6 - Symmetrical line capacitance characteristics

	Line pin 1	Line pin 2	Line pin 3	Line pin 4	Delta
Line to GND capacitance	0.574 pF	0.579 pF	0.576 pF	0.569 pF	0.010 pF
Line to Line capacitance	0.286 pF	0.289 pF	0.289 pF	0.286 pF	0.003 pF

Table 2 shows the regular, repeatable values and symmetry of the line capacitance values for the DVIULC-4SC6. In addition to the unprecedented low values, the minimized delta value of line capacitances ensures that data transmission signal integrity is maintained by minimizing crosstalk and differential delay values.

4 Conclusion

The new STMicroelectronics' DVIULC6-4SC6 diode array ESD protection device in SO23-6L package provides the best solution for optimum ESD protection in high speed data transmission applications. In addition, the ultra low capacitance and high bandwidth silicon structure minimizes the risk of signal degradation.

For more information, please visit www.st.com website.

5 Revision history

Date	Revision	Changes
09-Jan-2006	1	Initial release.

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