Self-test configuration for SPC58 H line devices

Introduction

This document provides the guidelines about how to configure the self-test control unit (STCU2) and start the self-test execution.

The STCU2, on SPC58EHx/SPC58NHx devices, manages both memory and logic built-in self-test (MBIST and LBIST) of the device. The MBISTs and LBISTs can detect latent failures which affect the volatile memories and the logic modules.

The reader should have a clear understanding of the usage of self-test. See Section 4.2: Reference documents for additional details.

1 Overview

The SPC58EHx/SPC58NHx support both the MBIST and LBIST. They include:

- 105 memory cuts (from 0 to 104)
- LBIST0 (the safety LBIST)

The reader can consult the complete list on the chapter 7 (device configuration) of the SPC58NHx/SPC58EHx reference manual.

See Section 4.2: Reference documents for additional details.

2 Self-test configuration

Self-test can run either in online or offline mode.

2.1 MBIST configuration

To reach the best trade-off in terms of consumption and execution time, we recommend to divide the MBISTs into 15 splits. The MBIST partitions belonging to the same split run in parallel.

The 15 splits run in sequential mode. For examples:

- all MBIST partitions belonging to the split_0 start in parallel
- after their execution, all MBIST partitions belonging to the split_1 start in parallel
- and so forth

The Section 4.2: Reference documents shows the complete list of the MBISTs and splits.

2.2 LBIST configuration

In offline mode, only the LBIST0 runs , that is the safey bist (to guarantee the ASIL D). It's the first BIST in the self-test configuration (pointer 0 in LBIST_CTRL register).

The number of patterns configured for this test is 5000 (as trade-off between the coverage and the time execution)

2.3 DCF list for offline configuration

MBISTs and LBIST0 can be executed in offline up to 100 Mhz as max frequency. The appendix reports the list of the DCF to be configured in order to start up the MBIST and LBIST during the boot phase (offline mode). They take around 130 ms.

2.4 Online mode configuration

In online mode the MBIST split list remains the same with some limitations due to the life cycle. All MBISTs can run in online mode only in ST production and Failure Analysis (FA).

In other life cycles, HSM /MBIST and FLASH MBIST are not accessible.

In this case, the maximum frequency for MBIST is 200 Mhz, provided by the sys_clock.

3 Summary

In SPC58EHx/SPC58NHx devices both MBIST and LBIST tests can run. In offline mode, only LBIST0 and all MBISTs tests can be executed according to the split configuration.

4 Other information

4.1 Acronyms

Table 1. **Acronyms**

Acronym	Name
MBIST	Memory built-in-self-test
LBIST	Logic built-in self-test
STCU2	Self-test control unit
HSM	Hardware system module
LC	Life Cycle
DCF	Device Configuration Format (DCF) Records
UTest	User Test flash block
FA	Failure Analysis

4.2 Reference documents

Table 2. **Reference documents**

Doc name	ID	Title
RM0452	028528	SPC58 H Line - 32 bit Power Architecture automotive MCU Triple z4 cores 200 MHz, 10 MBytes Flash, HSM, ASIL-D
AN4551	026636	SPC574K72xx self-test procedures

The split and DCF setting are contained in Microsoft Excel® workbook files attached to this document. It is necessary to locate the paperclip symbol on the left side of the PDF window and you click it. A double-click on the Excel file helps to open it.

Revision history

Table 3. **Document revision history**

Date	Revision	Changes
03-Sep-2020	1	Initial release.
05-Oct-2020	2	Updated Introduction.
13-Jul-2021	3	Updated the files excel in attached.
08-Aug-2024	4	Document status changed from ST Restricted to public. Updated title on cover page.

Contents