Serial flash discovery parameters for page EEPROMs

Introduction

The SFDP (serial flash discoverable parameter) standard provides a consistent method of describing the functional and feature capabilities of page EEPROMs in a standard set of internal parameter tables. These tables can be interrogated by the host system software to enable the adjustments needed to accommodate divergent features, according to the vendor.

STMicroelectronics SFDP table information aligns with JEDEC standard JESD216. Refer to JEDEC standard JESD216D for a complete overview of the SFDP table definition.

Table 1. Applicable products

Root part number reference	Commercial part numbers
M95P32-E M95P32-I	M95P32-xxxxx
M95P16-E M95P16-I	M95P16-xxxxx
M95P08-E M95P08-I	M95P08-xxxxx

1 SFDP header

The SFDP header is located at address 0x0000 of the SFDP data structure.

Table 2. Header structure

Description	Address	Bits	Value	Dword	Comment
SFDP signature	00h	7:0	53h	Header0	-
	01h	7:0	46h		-
	02h	7:0	44h		-
	03h	7:0	50h		-
SFDP version minor	04h	7:0	08h		Minor revision 8 = JESD216D
SFDP version major	05h	7:0	01h		Major revision 1 = JESD216D
Number of parameter headers	06h	7:0	00h		Only 1 parameter header as defined in basic table
SFDP access control	07h	7:0	FFh		Access SFDP with 1s-1s-1s
Parameter ID LSB	08h	7:0	00h	Header1	Jedec ID => 00h for basic table
Parameter minor revision	09h	7:0	08h		Minor revision 8 = JESD216D
Parameter major revision	0Ah	7:0	01h		Major revision 1 = JESD216D
Parameter length (in DW)	0Bh	7:0	14h		20 parameters Dword-Basic table.
Parameter table pointer	0Ch	7:0	10h		-
-	0Dh	7:0	00h		-
-	0Eh	7:0	00h		-
Parameter ID MSB	0Fh	7:0	FFh		Jedec ID => FFh for basic table

2 SFDP basic properties

Table 3. **Parameters**

Description	Address	Bits	Value	Dword	Comment
Erase granularity	10h	1:0	01b	Dword1	4-Kbyte granularity
Write granularity		2	1b		More than 64 page buffers
WREN required for writing to volatile status register		3	0b		-
WREN code for writing to volatile status register		4	1b		-
Reserved		7:5	111b		-
4-Kbyte sector erase opcode	11h	15:8	20h		-
1-1-2 fast read	12h	16	1b		Support read in dual output
Number of address bytes		18:17	00b		3 address bytes
DTR mode		19	0b		DTR not supported
1-2-2 fast read		20	0b		Dual input address not supported
1-4-4 fast read		21	0b		Quad input address not supported
1-1-4 fast read		22	1b		Quad output read supported
Unused		23	1b		-
Unused	13h	24:31	FFh		-
Memory size in bits	14h	7:0	FFh	Dword2	01FFFFFFh = 32 Mbit 00FFFFFFh = 16 Mbit 07FFFFFh = 8 Mbit
	15h	15:8	FFh		
	16h	23:16	FFh		
	17h	31:24	01h		
1-4-4 Fast read dummy clock cycles and mode bits	18h	7:0	00h	Dword3	Not supported
1-4-4 fast read opcode	19h	15:8	00h		Not supported
1-1-4 fast read dummy clock cycles and mode bits	1Ah	23:16	08h		8 dummy clock cycles and no mode bit
1-1-4 fast read opcode	1Bh	31:24	6Bh		-
1-1-2 fast read dummy clock cycles and mode bits	1Ch	7:0	08h	Dword4	8 dummy clock cycles and no mode bit
1-1-2 fast read opcode	1Dh	15:8	3Bh		-
1-2-2 fast read dummy clock cycles and mode bits	1Eh	23:16	00h		Not supported
1-2-2 fast read opcode	1Fh	31:24	00h		Not supported
2-2-2 and 4-4-4 fast read	20h	7:0	EEh	Dword5	Not supported
Reserved	21h	15:8	FFh		-
Reserved	22h	23:16	FFh		-
Reserved	23h	31:24	FFh		-
Reserved	24h	7:0	FFh	Dword6	-
Reserved	25h	15:8	FFh		-
2-2-2 fast read dummy clock cycles and mode bits	26h	23:16	00h		Not supported
2-2-2 fast read opcode	27h	31:24	00h		Not supported

Description	Address	Bits	Value	Dword	Comment
Reserved	28h	7:0	FFh	Dword7	-
Reserved	29h	15:8	FFh		-
2-2-2 fast read dummy clock cycles and mode bits	2Ah	23:16	00h		Not supported
2-2-2 fast read opcode	2Bh	31:24	00h		Not supported
Erase type 1 size	2Ch	7:0	09h	Dword8	512 bytes = 1 page
Erase type 1 opcode	2Dh	15:8	DBh		Page erase
Erase type 2 size	2Eh	23:16	0Ch		4 Kbytes = 1 sector
Erase type 2 opcode	2Fh	31:24	20h		Sector erase
Erase type 3 size	30h	7:0	10h	Dword9	64 Kbytes = 1 block
Erase type 3 opcode	31h	15:8	D8h		Block erase
Erase type 4 size	32h	23:16	00h		Not defined
Erase type 4 opcode	33h	31:24	00h		Not defined
Multiplier for max chip erase time	34h to 37h	3:0	0100b = 4	Dword10	Max chip erase = 2 x (0100b+1) x CE typ
Typ page erase time		8:4	00000b		(00000b + 1) x units = 1 ms
Units		10:9	00b		1ms
Typ sector erase time		15:11	00001b = 1		(00001b + 1) x units = 2 ms
Units		17:16	00b		1 ms
Typ block erase time		22:18	00011b = 3		(00100b + 1) x units = 4 ms
Units		24:23	00b		1 ms
Typ erase type 4 time		29:25	00000b		Not defined
Units		31:30	00b		Not defined
Multiplier for max page program time	38h to 3Bh	3:0	0000b	Dword11	Max page program = 2 x (0000b+1) x PGPR = 2 ms
Page size		7:4	1001b = 9		Page size 9h => 512 bytes
Page program typ time		12:8	10011b = 19		(01111b + 1) x units = 1 ms
units		13	1b		64 µs
First byte program typ time		17:14	1011b = 11		(1011b + 1) x units = 96 µs
units		18	1b		8 µs
Byte program typ time		22:19	0001b = 1		(0001b + 1) x units = 2 µs
units		23	0b		1 µs
Chip erase typ time		28:24	00000b		(00000b + 1) x units = 16 ms
units		30:20	00b		16 ms
Reserved		31	1b		-
Erase/program suspend/resume	3Ch	7:0	00h	Dword12	Not supported
	3Dh	15:8	00h		
	3Eh	23:16	00h		
	3Fh	31:24	00h		
Suspend/resume instructions	40h	7:0	00h	Dword13	Not supported
	41h	15:8	00h		
	42h	23:16	00h		

Description	Address	Bits	Value	Dword	Comment
Suspend/resume instructions	43h	31:24	00h	Dword13	Not supported
Reserved	44h	1:0	00b	Dword14	-
Status register polling		7:2	000001b		WIP is bit(0) of status register
Exit deep power down max delay	45h to 47h	12:8	11101b		(11101b + 1) x units = 30 µs
Units		14:13	01b		1 µs
Exit deep power down instruction		22:15	ABh		-
Enter deep power down instruction		30:23	B9h		-
Deep power down supported		31	0b		-
4-4-4 disable sequence	48h to 4Ah	3:0	0000b	Dword15	Not supported
4-4-4 enable sequence		8:4	00000b		
0-4-4 mode support		9	0b		
0-4-4 mode exit method		15:10	000000b		
0-4-4 mode entry method		19:16	0000b		
Quad enable requirements		22:20	000b		
Hold or reset disable		23	0b		
Reserved	4Bh	31:24	00h		-
Non volatile register and WREN	4Ch to 4Eh	6:0	0010001b	Dword16	Std status register format with WREN
Reserved		7	0b		-
Software reset		13:8	010000b		Enable 66h + reset 99h
Exit 4-byte addressing		23:14	0000000000b		Not supported
Enter 4-byte addressing	4Fh	31:24	00h		Not supported
(1S-8S-8S) fast read and (1S-1S-8S) fast read	50h	7:0	00h	Dword17	Not supported
	51h	7:0	00h		
	52h	7:0	00h		
	53h	7:0	00h		
Reserved	54h to 57h	7:0	00h	Dword18	-
Reserved		15:8	00h		-
Reserved		17:16	00b		-
Variable output driver strength		22:18	00000b		Not supported
Jedec SPI reset		23	0b		Not supported
Data strobe in STR		25:24	00b		Not supported
Data strobe QPI STR		26	0b		Not supported
Data strobe QPI DTR		27	0b		Not supported
Reserved		28	0b		-
Octal DTR		30:29	00b		Not supported
Byte order in 8D mode		31	0b		Not supported
Octal disable sequence	58h to 5Bh	3:0	0000b	Dword19	Not supported
Octal enable sequence		7:4	00000b		
0-8-8 mode supported		9	0b		
0-8-8 exit mode		15:10	000000b		
0-8-8 entry mode		19:16	0000b		

Description	Address	Bits	Value	Dword	Comment
Octal enable requirements	58h to 5Bh	22:20	000b	Dword19	Not supported
Reserved		31:23	000000000b		-
Maximum speed 4s-4s-4s no data strobe	5Ch	3:0	1111b	Dword20	Not supported
Maximum speed 4s-4s-4s with data strobe		7:4	1111b		Not supported
Maximum speed 4s-4d-4d no data strobe	5Dh	11:8	1111b		Not supported
Maximum speed 4s-4d-4d with data strobe		15:12	1111b		Not supported
Maximum speed 8s-8s-8s no data strobe	5Eh	19:16	1111b		Not supported
Maximum speed 8s-8s-8s with data strobe		23:20	1111b		Not supported
Maximum speed 8s-8s-8s no data strobe	5Fh	27:24	1111b		Not supported
Maximum speed 8s-8s-8s with data strobe		31:28	1111b		Not supported
-	60h to 1FFh	-	FFh	-	-

Revision history

Table 4. **Document revision history**

Date	Version	Changes
06-Feb-2023	1	Initial release.
20-Jul-2023	2	Added Table 1. Applicable products. Updated Section 2 SFDP basic properties. Minor text edits across the whole document.

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